

# NTD5806N, NVD5806N

## Power MOSFET

40 V, 33 A, Single N-Channel, DPAK/IPAK

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable – NVD5806N
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- CCFL Backlight
- DC Motor Control
- Power Supply Secondary Side Synchronous Rectification

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DS}$	40	V	
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V	
Gate-to-Source Voltage – Non-Repetitive ( $t_p < 10 \mu\text{s}$ )	$V_{GS}$	$\pm 30$	V	
Continuous Drain Current ( $R_{\theta JC}$ ) (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$ 33	A
		$T_C = 100^\circ\text{C}$	23	
Power Dissipation ( $R_{\theta JC}$ ) (Note 1)		$T_C = 25^\circ\text{C}$	$P_D$ 40	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$ 67	A	
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	33	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega, I_{L(pk)} = 28 \text{ A}, L = 0.1 \text{ mH}, V_{DS} = 40 \text{ V}$ )	$E_{AS}$	39	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.7	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	57.5	

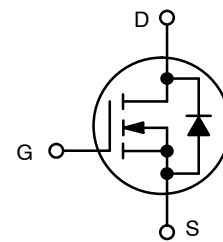
1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).



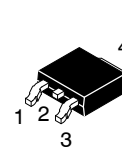
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<http://onsemi.com>

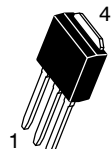
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
40 V	26 m $\Omega$ @ 4.5 V	33 A
	19 m $\Omega$ @ 10 V	



N-CHANNEL MOSFET

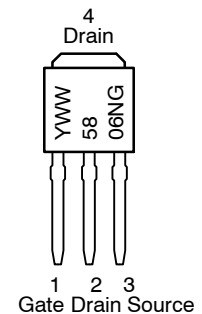
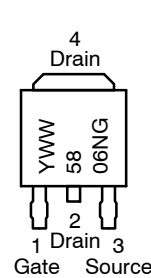


DPAK  
CASE 369C  
(Surface Mount)  
STYLE 2



IPAK  
CASE 369D  
(Straight Lead  
DPAK)

### MARKING DIAGRAMS & PIN ASSIGNMENT



Y = Year  
WW = Work Week  
5806N = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTD5806N, NVD5806N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40	45.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			29.5		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 150^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.4		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.8		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		12.7	19	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		17.8	26	

### CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		860		pF
Output Capacitance	$C_{oss}$			130		
Reverse Transfer Capacitance	$C_{rss}$			100		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 30\text{ A}$		17	38	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.95		
Gate-to-Source Charge	$Q_{GS}$			3.4		
Gate-to-Drain Charge	$Q_{GD}$			4.5		

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 20\text{ V}, I_D = 30\text{ A}, R_G = 2.5\ \Omega$		10.6		ns
Rise Time	$t_r$			93.7		
Turn-Off Delay Time	$t_{d(off)}$			14.2		
Fall Time	$t_f$			4.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}, I_D = 30\text{ A}, R_G = 2.5\ \Omega$		8.0		ns
Rise Time	$t_r$			49		
Turn-Off Delay Time	$t_{d(off)}$			19.8		
Fall Time	$t_f$			2.6		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.86	1.2	V
			$T_J = 150^\circ\text{C}$		0.69		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, \text{d}I_S/\text{d}t = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		18.8		ns	
Charge Time	$t_a$			11.8			
Discharge Time	$t_b$			7.0			
Reverse Recovery Charge	$Q_{RR}$			10.9			nC

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS

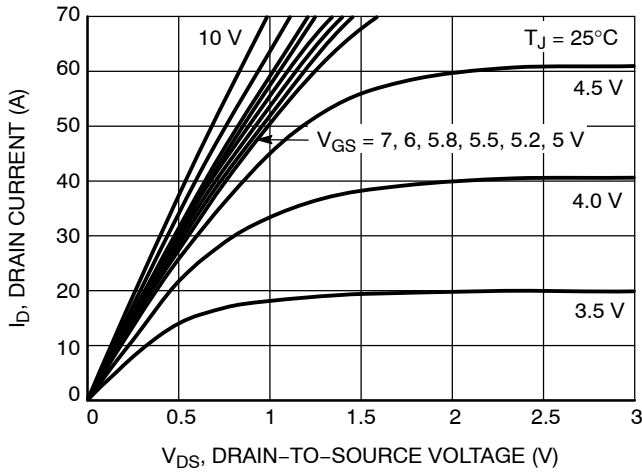


Figure 1. On-Region Characteristics

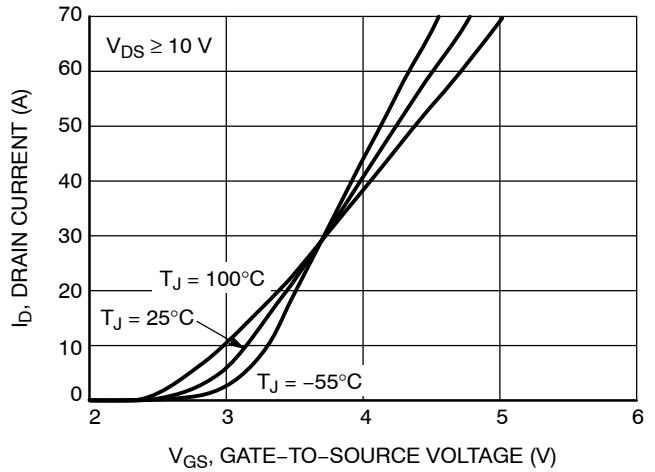


Figure 2. Transfer Characteristics

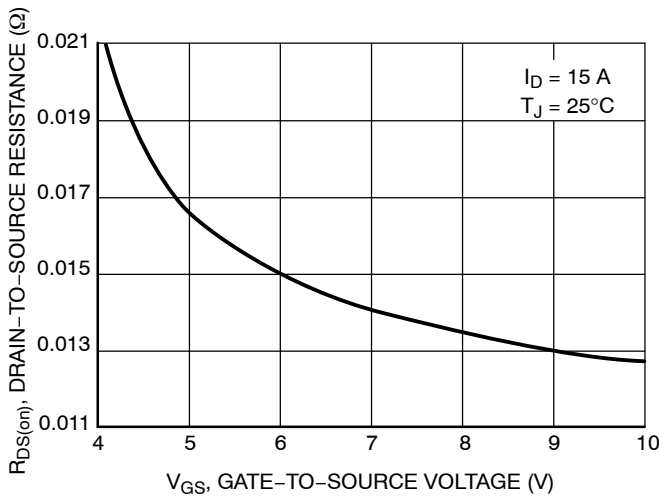


Figure 3. On-Resistance vs. Drain Current

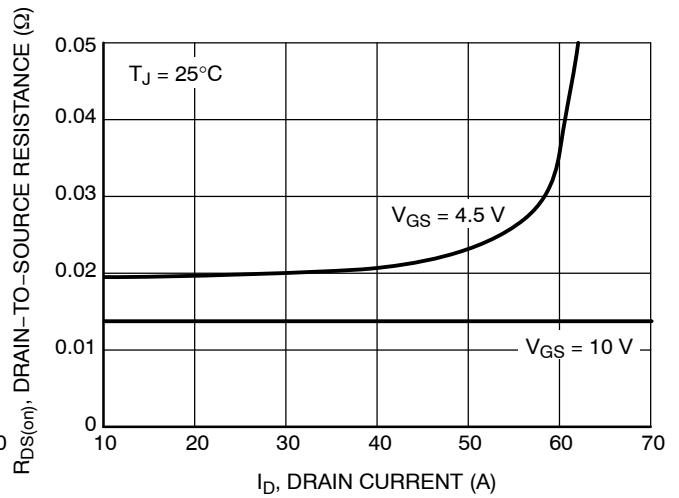


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

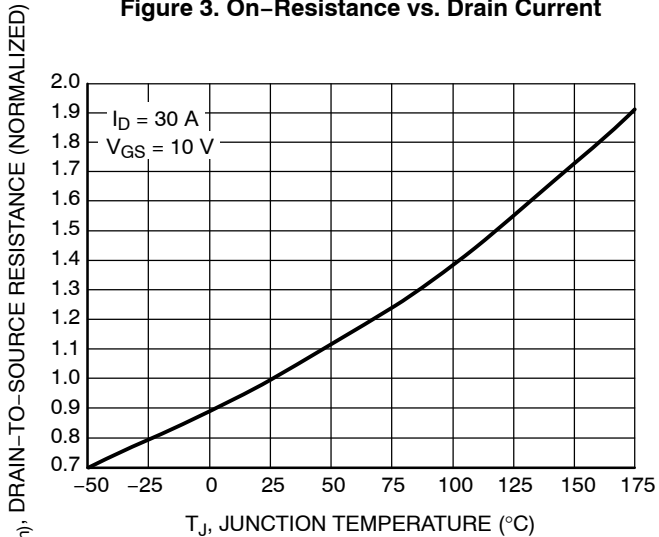


Figure 5. On-Resistance Variation with Temperature

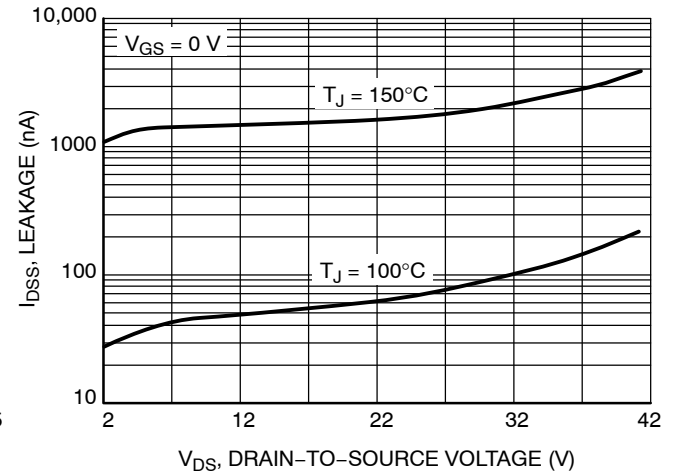


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

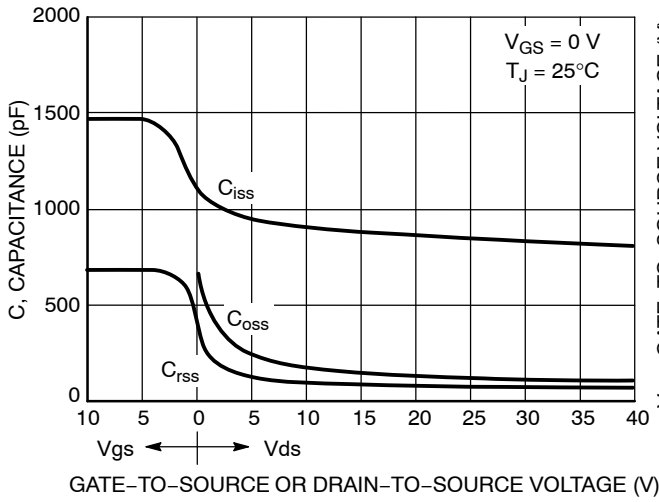


Figure 7. Capacitance Variation

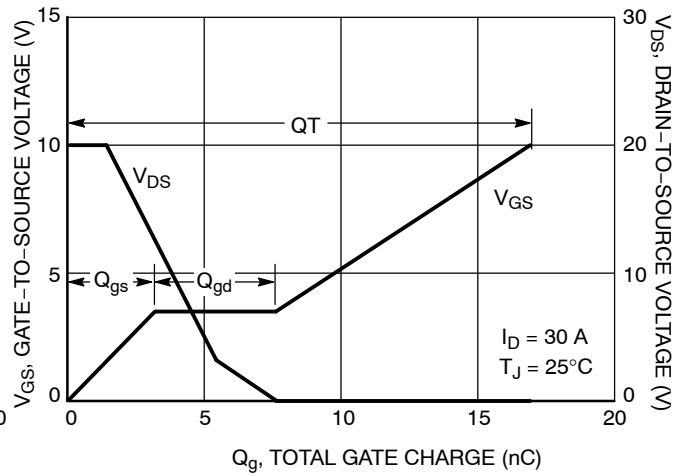


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

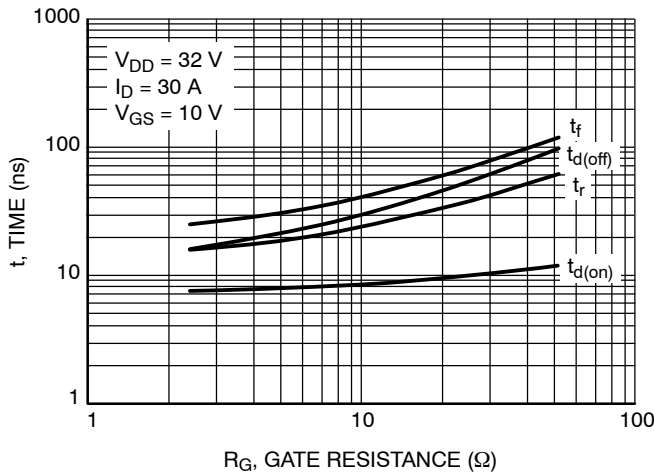


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

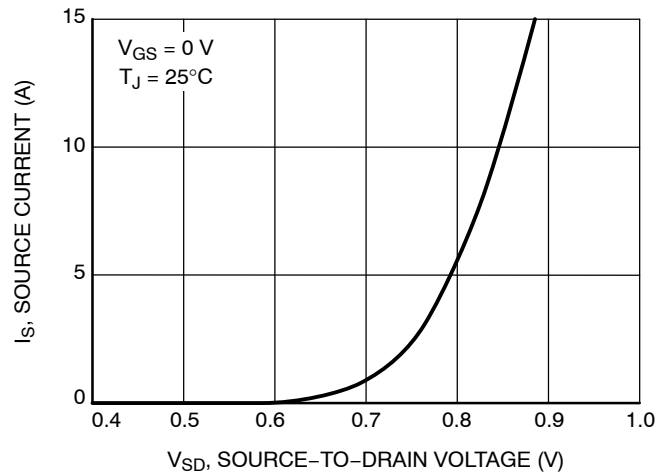


Figure 10. Diode Forward Voltage vs. Current

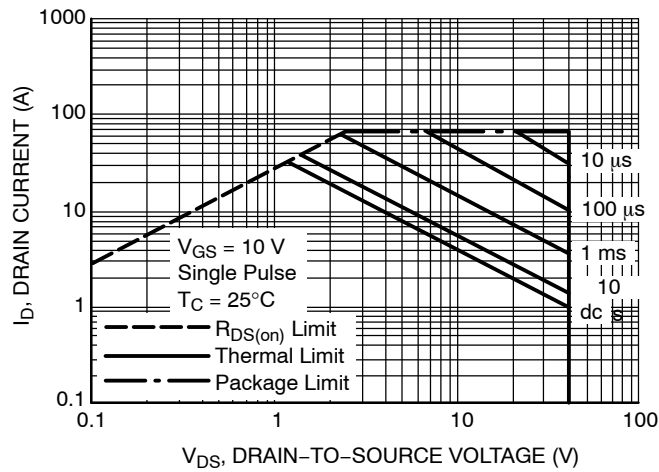


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTD5806N, NVD5806N

## TYPICAL PERFORMANCE CHARACTERISTICS

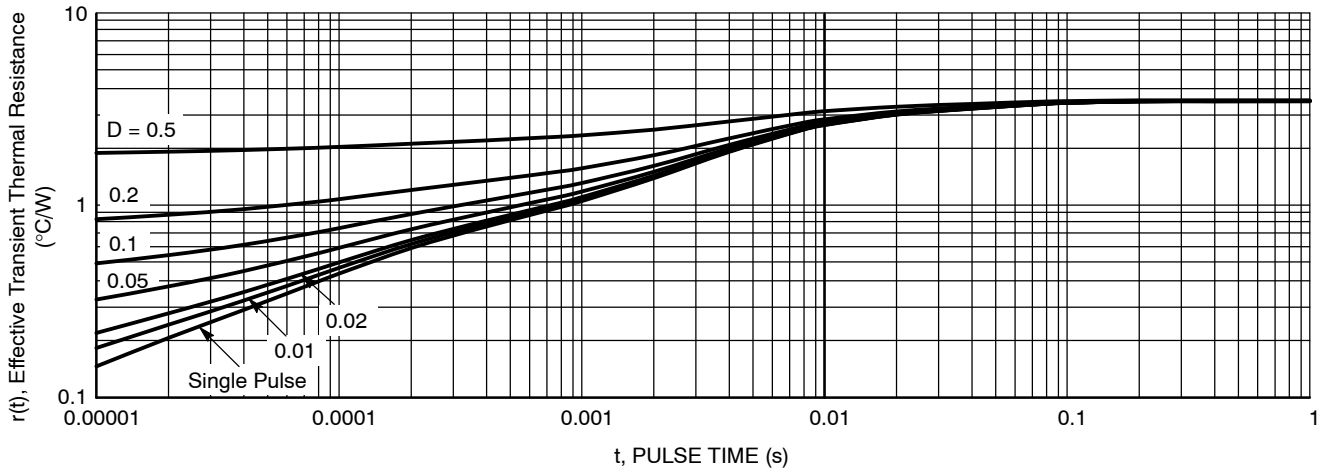


Figure 12. Thermal Response

### ORDERING INFORMATION

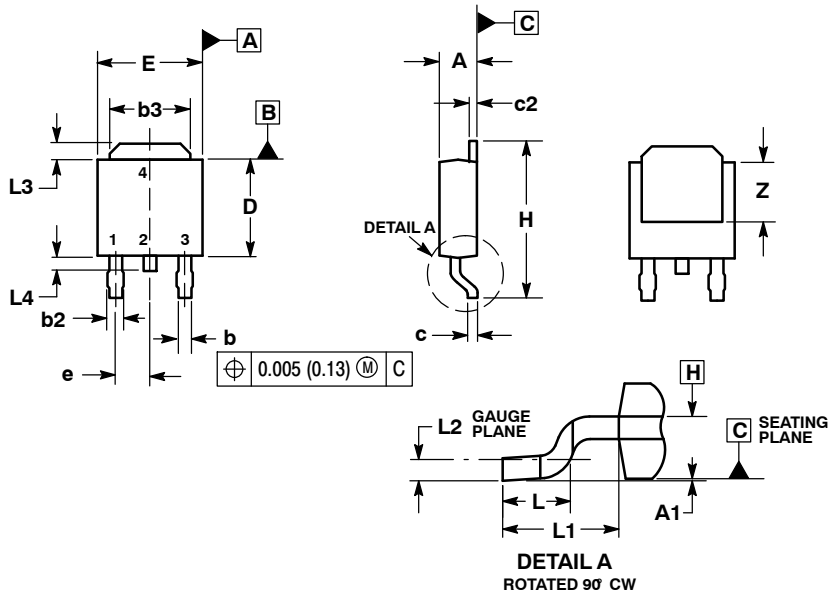
Order Number	Package	Shipping <sup>†</sup>
NTD5806NG	IPAK (Straight Lead DPAK) (Pb-Free)	75 Units / Rail
NTD5806NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5806NT4G	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTD5806N, NVD5806N

## PACKAGE DIMENSIONS

DPAK  
CASE 369C-01  
ISSUE D

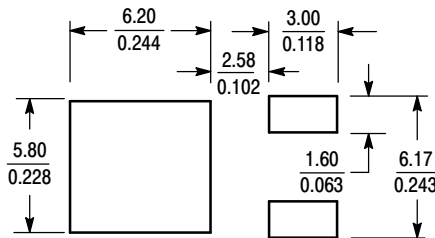


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### SOLDERING FOOTPRINT\*



SCALE 3:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

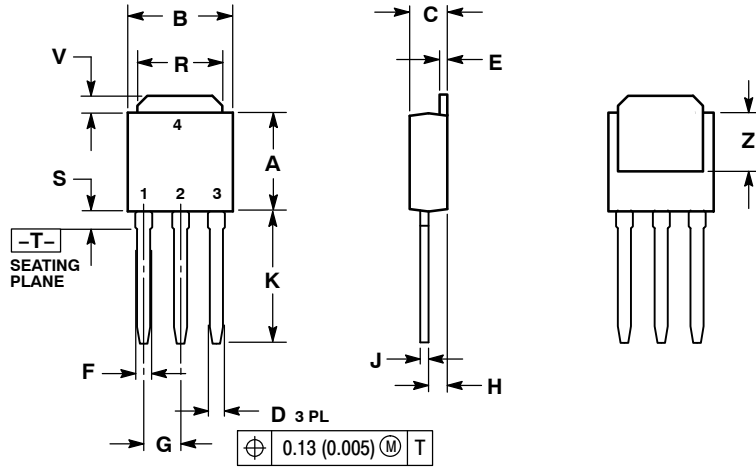
- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTD5806N, NVD5806N

## PACKAGE DIMENSIONS

### IPAK CASE 369D-01 ISSUE C



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

**STYLE 2:**

- PIN 1: GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

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