8-BIT MICROCONTROLLER

Table of Contents-

1 GENERAL DESCRIPTION

The W78E516D/W78E058D series is an 8-bit microcontroller which has an in-system programmable Flash EPROM for on-chip firmware updating.

The instruction sets of the W78E516D/W78E058D are fully compatible with the standard 8052. The W78E516D/W78E058D series contains a 64K/32K bytes of main Flash EPROM and a 4K bytes of auxiliary Flash EPROM which allows the contents of the 64K/32K bytes main Flash EPROM to be up-dated by the loader program located in the 4K bytes Flash EPROM; a 256 bytes of SRAM; 256 bytes of AUXRAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by an 8 sources 2-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E516D/W78E058D series allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E516D/W78E058D series microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4 to 5.5V
- Temperature grade is (-40°C~85°C)
- 64K/32K bytes of in-system programmable FLASH EPROM for Application Program (APROM)
- 4K bytes of auxiliary FLASH EPROM for Loader Program (LDROM)
- Low standby current at full supply voltage
- 512 bytes of on-chip RAM. (include 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space
- One 4-bit multipurpose programmable port, additional $\overline{INT2}$ / $\overline{INT3}$
- Support Watch Dog Timer
- Three 16-bit timer/counters
- One full duplex serial port
- 8-sources, 2-level interrupt capability
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78E516DDG
  - Lead Free (RoHS) PLCC 44: W78E516DPG
  - Lead Free (RoHS) PQFP 44: W78E516DFG
  - Lead Free (RoHS) LQFP 48: W78E516DLG
  - Lead Free (RoHS) DIP 40: W78E058DDG
  - Lead Free (RoHS) PLCC 44: W78E058DPG
  - Lead Free (RoHS) PQFP 44: W78E058DFG
  - Lead Free (RoHS) LQFP 48: W78E058DLG

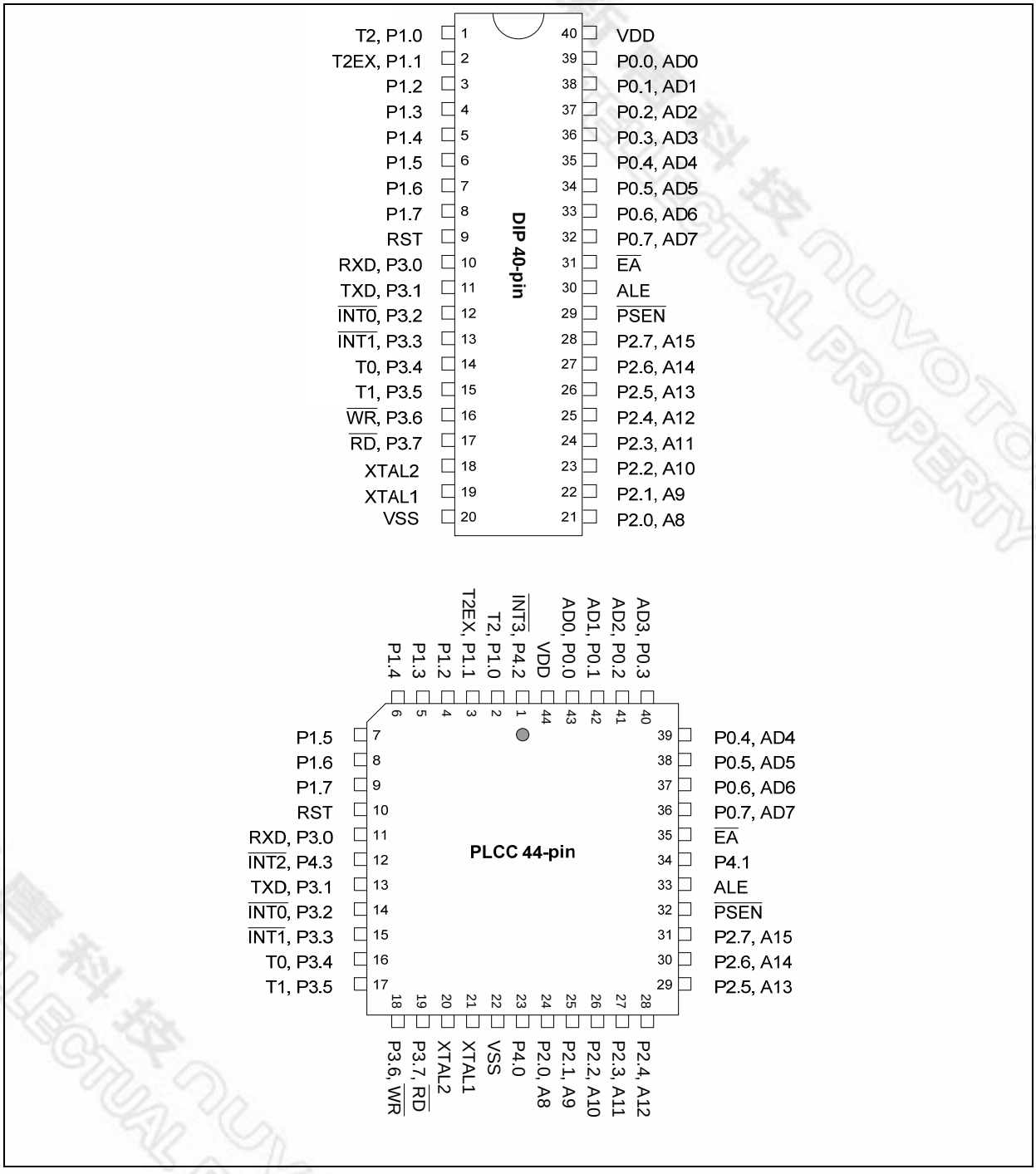
3 PARTS INFORMATION LIST

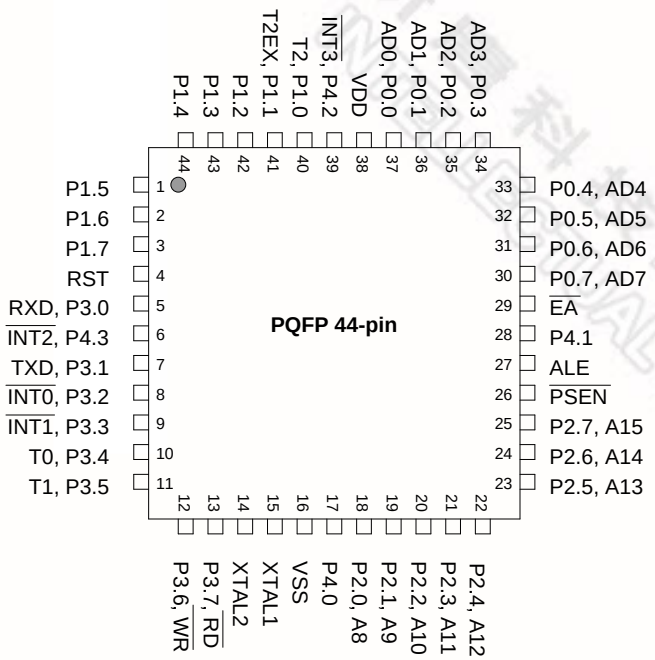
3.1 Lead Free (RoHS) Parts information list

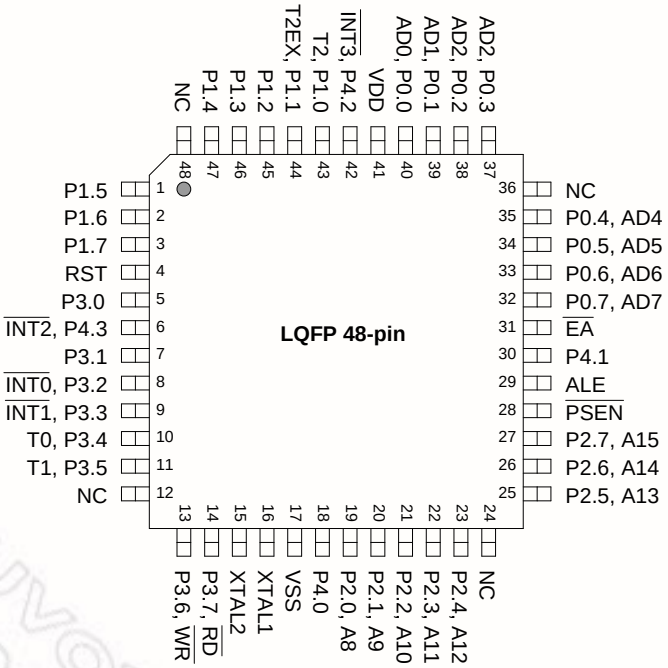
Table 3-1: Lead Free (RoHS) Parts information list

PART NO.	APROM FLASH SIZE	LDROM FLASH SIZE	RAM	PACKAGE	Temperature grade
W78E516DDG	64K Bytes	4K Bytes	512 Bytes	DIP-40 Pin	-40°C~85°C
W78E516DPG			512 Bytes	PLCC-44 Pin	
W78E516DFG			512 Bytes	PQFP-44 Pin	
W78E516DLG			512 Bytes	LQFP-48 Pin	
W78E058DDG	32K Bytes	4K Bytes	512 Bytes	DIP-40 Pin	-40°C~85°C
W78E058DPG			512 Bytes	PLCC-44 Pin	
W78E058DFG			512 Bytes	PQFP-44 Pin	
W78E058DLG			512 Bytes	LQFP-48 Pin	

4 PIN CONFIGURATIONS




P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD3, P0.3
P1.5
P1.6
P1.7
RST
RXD, P3.0
INT2, P4.3
TXD, P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
PQFP 44-pin


NC
P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD2, P0.3
P1.5
P1.6
P1.7
RST
P3.0
INT2, P4.3
P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
NC
NC
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
NC
LQFP 48-pin

5 PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the internal ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I L	**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	**CRYSTAL 1:** This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	**CRYSTAL 2:** This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	I	**GROUND:** ground potential.
VDD	I	**POWER SUPPLY:** Supply voltage for operation.
P0.0–P0.7	I/O D	**PORT 0:** Port 0 is an **open-drain bi-directional I/O port**. This port also provides a multiplexed low order address/data bus during accesses to external memory.
P1.0–P1.7	I/O H	**PORT 1**: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	I/O H	**PORT 2:** Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	I/O H	**PORT 3:** Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port 0 input TXD(P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$ (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) : External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	I/O H	**PORT 4:** Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

* Note : **TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

6 BLOCK DIAGRAM

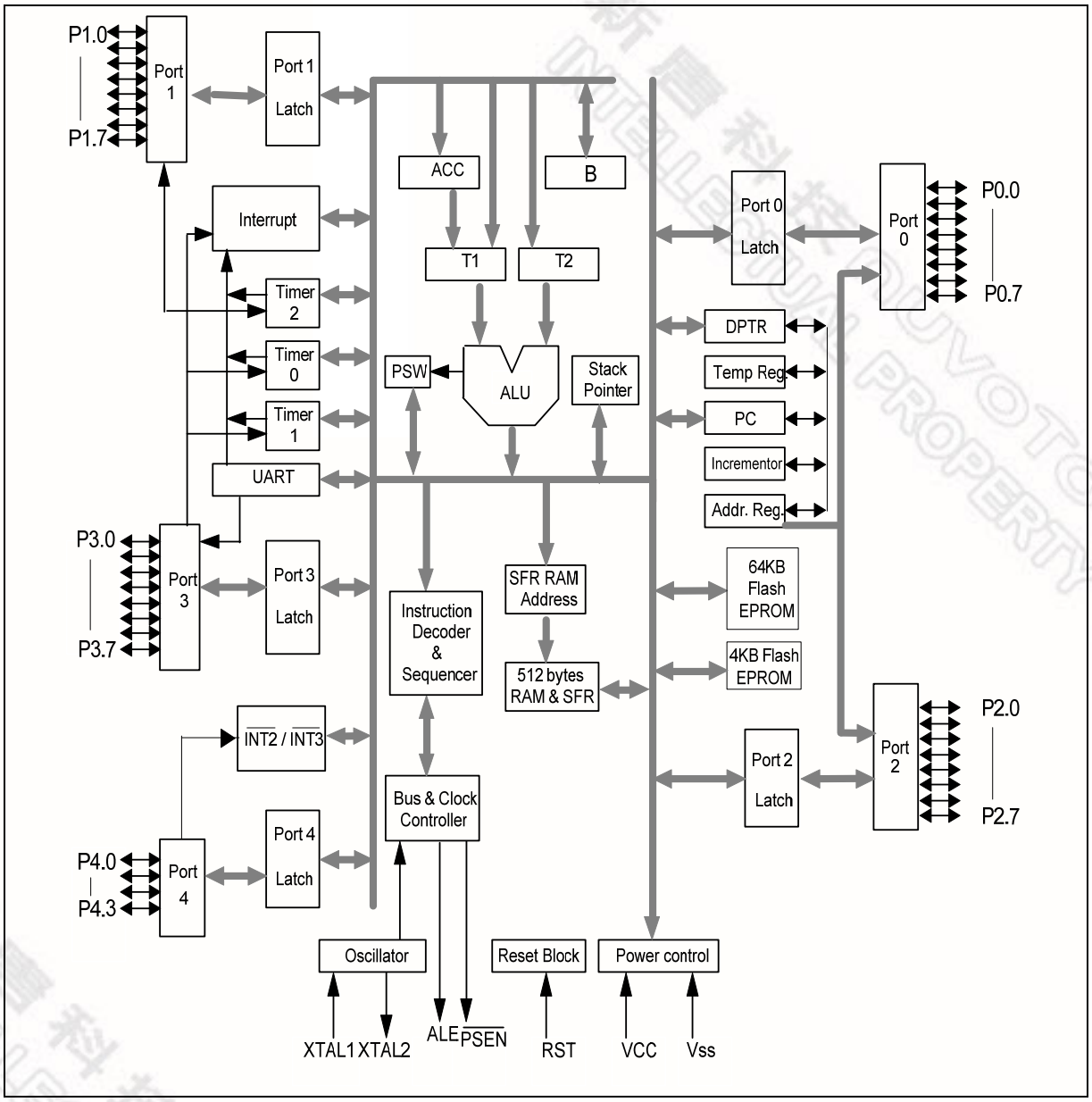


Figure 6- 1 W78E516D/W78E058D Block Diagram

7 FUNCTIONAL DESCRIPTION

The W78E516D/W78E058D series architecture consists of a core controller surrounded by various registers, four general purpose I/O ports, one special purpose programmable 4-bits I/O port, 512 bytes of RAM, three timer/counters, a serial port. The processor supports 111 different op-codes and references both a 64K program address space and a 64 K data storage space.

7.1 On-Chip Flash EPROM

The W78E516D/W78E058D series includes one 64K/32K bytes of main FLASH EPROM for application program (APROM) and one 4K bytes of FLASH EPROM for loader program (LDROM) when operating the in-system programming feature. In normal operation, the microcontroller will execute the code from the 64K/32K bytes of main FLASH EPROM. By setting program registers, user can force microcontroller to switch to the programming mode which microcontroller will execute the code (loader program) from the 4K bytes of auxiliary FLASH EPROM, and this loader program is going to update the contents of the 64K/32K bytes of main FLASH EPROM. After reset, the microcontroller executes the new application program in the main FLASH EPROM. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible that the end-user is able to easily update the system firmware by the them without opening the chassis.

7.2 I/O Ports

The W78E516D/W78E058D series has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port1 and 3 act as I/O ports with alternate functions. Port 4 is only available on PLCC/QFP/LQFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

7.3 Serial I/O

The W78E516D/W78E058D series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W78E516D/W78E058D series can operate in different modes in order to obtain timing similarity as well.

7.4 Timers

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the 8051 CPU. Timer 2 is a special feature of the W78E516D/W78E058D series: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or

as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

7.4.1 Clock

The W78E516D/W78E058D series are designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516D/W78E058D series relatively insensitive to duty cycle variations in the clock.

7.5 Interrupts

The Interrupt structure in the W78E516D/W78E058D series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W78E516D/W78E058D series provides 8 interrupt resources with two priority level, including four external interrupt sources, three timer interrupts, serial I/O interrupts.

7.6 Data Pointers

The data pointer of W78E516D/W78E058D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78E516D/W78E058D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78E516D/W78E058D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E516D/W78E058D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

7.7.5 Stack Pointer

The W78E516D/W78E058D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E516D/W78E058D series. Hence the size of the stack is limited by the size of this RAM.

7.7.6 Scratch-pad RAM

The W78E516D/W78E058D series has a 256 bytes on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit address-able, and can be directly addressed for this purpose.

7.7.7 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. The data memory region is from 0000H to 00FFH. Memory MAP shows the mem-ory map for this product series. W78E516D/W78E058D series can read/write 256 bytes AUX RAM by the MOVX instruction.

8 MEMORY ORGANIZATION

The W78E516D/W78E058D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

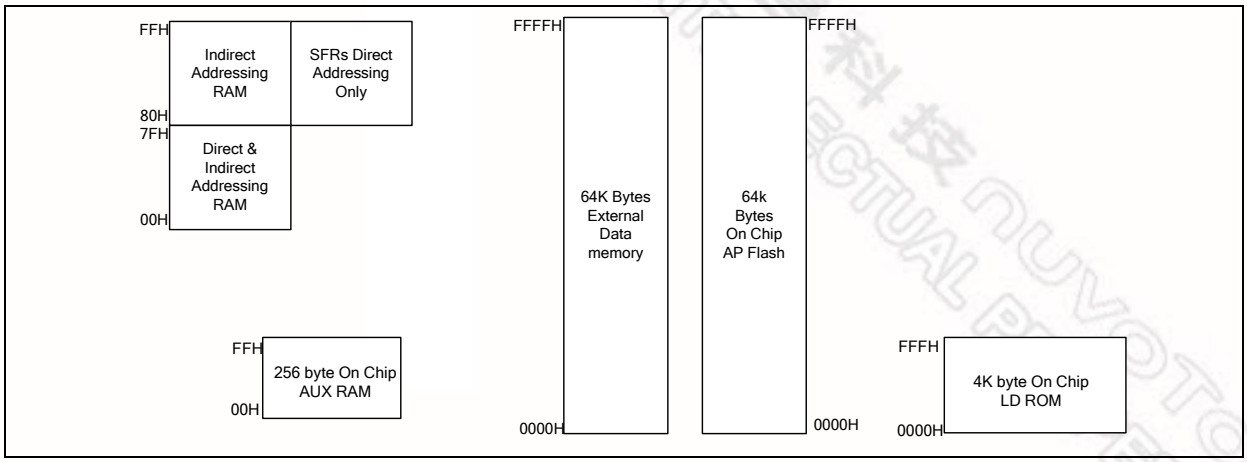


Figure 8- 1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E516D/W78E058D series can be up to 64K/32K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E516D/W78E058D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

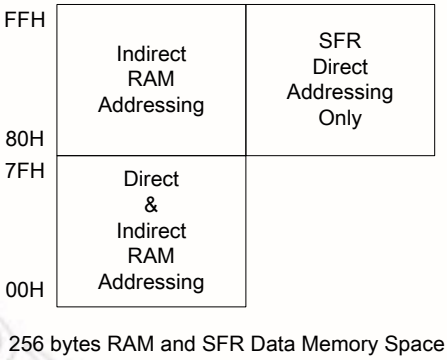


Figure 8- 2 W78E516D/W78E058D RAM and SFR Memory Map

Since the scratch-pad RAM is only 256bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

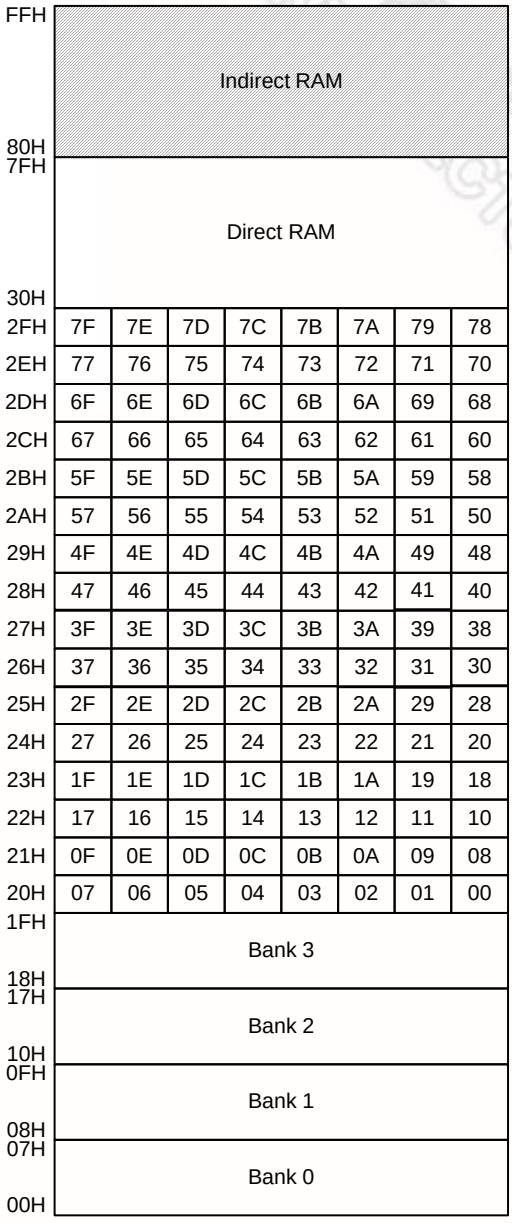


Figure 8- 3 Scratch-pad RAM

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78E516D/W78E058D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

8.2.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

8.2.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8.2.4 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. A access to external data memory locations higher than 255 will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disabled after power-on reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM.

9 SPECIAL FUNCTION REGISTERS

The W78E516D/W78E058D series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W78E516D/W78E058D series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

W78E516D/W78E058D Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B						CHPENR		F7
E8									EF
E0	+ACC								E7
D8	+P4								DF
D0	+PSW								D7
C8	+T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	+XICON		P4CONA	P4CONB	**SFRAL**	**SFRAH**	SFRFD	SFRCN	C7
B8	+IP							CHPCON	BF
B0	+P3				**P43AL**	**P43AH**			B7
A8	+IE				**P42AL**	**P42AH**	P2ECON		AF
A0	+P2								A7
98	+SCON	SBUF							9F
90	+P1				**P41AL**	**P41AH**			97
88	+TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	WDTC	8F
80	+P0	SP	DPL	DPH	**P40AL**	**P40AH**	P0UPR	PCON	87

Figure 9-1: Special Function Register Location Table

Note: 1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
CHPENR	Chip enable register	F6H									1111 0110B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
P4	Port 4	D8H					P43	P42	P41	P40	0000 1111B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B
TH2	T2 reg. high	CDH									0000 0000B
TL2	T2 reg. low	CCH									0000 0000B
RCAP2H	T2 capture low	CBH									0000 0000B
RCAP2L	T2 capture high	CAH									0000 0000B
T2CON	Timer 2 control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
SFRCN	SFR for program control	C7H									0000 0000B
SFRFD	SFR for program data	C6H									0000 0000B
SFRAH	Port4 base address high register	C5H									0000 0000B
SFRAL	Port4 base address low register	C4H									0000 0000B
P4CONB	Port 4 control B	C3H	P43FUN1	P43FUN0	P43CMP1	P43COM0	P42FUN1	P42FUN0	P42CMP1	P42CMP2	0000 0000B
P4CONA	Port 4 control A	C2H	P41UN1	P41FUN0	P41CMP1	P41COM0	P40FUN1	P40FUN0	P40CMP1	P40CMP2	0000 0000B
XICON	External interrupt control	C0H	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2	0000 0000B
CHPCON	Chip Control	BFH	SWRESET			ENAUXRAM			FBOOTSL	FPROGEN	XXX0 0000B[1]
IP	Interrupt priority	B8H	(BF) -	(BE) -	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x000 0000B
P43AH	Port 4.3 comparator high address	B5H									0000 0000B
P43AL	Port 4.3 comparator low address	B4H									0000 0000B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
P2ECON	Port 2 expanded control	AEH	P43CSINV	P42CSINV	P41CSINV	P40CSINV	-	-			0000 0000B
P42AH	Port 4.2 comparator high address	ADH									0000 0000B
P42AL	Port 4.3 comparator low address	ACH									0000 0000B
IE	Interrupt enable	A8H	(AF) EA	(AE) -	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111B
SBUF	Serial buffer	99H									xxxx xxxxB
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P41AH	Port 4.1 comparator high address	95H									0000 0000B
P41AL	Port 4.1 comparator low address	94H									0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91) T2EX	(90) T2	1111 1111B
WDTC	Watchdog control	8FH	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0	0000 0000B
AUXR	Auxiliary	8EH								ALE_OFF	0000 0110B
TH1	Timer high 1	8DH									0000 0000B
TH0	Timer high 0	8CH									0000 0000B
TL1	Timer low 1	8BH									0000 0000B
TL0	Timer low 0	8AH									0000 0000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B

TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power control	87H	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL	00x1 0000B
P0UPR	Port 0 pull up option register	86H								P0UP	0000 0000B
P40AH	HI address comparator of P4.0	85H									0000 0000B
P40AL	LO address comparator of P4.0	84H									0000 0000B
DPH	Data pointer high	83H									0000 0000B
DPL	Data pointer low	82H									0000 0000B
SP	Stack pointer	81H									0000 0111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	1111 1111B

[1]: When CPU in F04KBOOT mode (Ref. P65), CHPCON=1xx0 0000B, other mode the CHPCON=0xx0 0000B

9.1 SFR Detail Bit Descriptions

Port 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

BIT	NAME	FUNCTION
7-0	P0.[7:0]	Port 0 is an open-drain bi-directional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

P4.0 Base Address Low Byte Register

Bit:

7	6	5	4	3	2	1	0
P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

BIT	NAME	FUNCTION
7-0	P40AL.[7:0]	The Base address register for comparator of P4.0. P40AL contains the low-order byte of address.

P4.0 Base Address High Byte Register

Bit:

7	6	5	4	3	2	1	0
P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic:P40AH Address: 85h

BIT	NAME	FUNCTION
7-0	P40AH.[7:0]	The Base address register for comparator of P4.0. P40AH contains the High-order byte of address.

Port 0 Pull up Option Register

Bit:

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P0UP

Mnemonic: P0UPR Address: 86h

BIT	NAME	FUNCTION
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:

7	6	5	4	3	2	1	0
SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.
6	SMOD 0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as

		Frame Error (FE) status flag.
5	-	Reserved
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

Timer Control

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

Timer Mode Control

Bit:	7	6	5	4	3	2	1	0

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

AUXR

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALE_OFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
0	ALE_OFF	1: Disable ALE output 0: Enable ALE output

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog if set.
6	CLRW	Clear watch-dog timer and Pre-scalar if set. This flag will be cleared automatically.
5	WIDL	If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is

		disabled under IDLE mode. Default is cleared.
2-0	PS2-0	Watch-dog Pre-scalar timer select. Pre-scalar is selected when set PS2–0 as follows: **PS2 PS1 PS0 — PRE-SCALAR SELECT** 0 0 0 — 2 0 0 1 — 4 0 1 0 — 8 0 1 1 — 16 1 0 0 — 32 1 0 1 — 64 1 1 0 — 128 1 1 1 — 256

Port 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

BIT	NAME	FUNCTION
7-0	P1.[7:0]	General purpose I/O port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read.

P4.1 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	P41AL.7	P41AL.6	P41AL.5	P41AL.4	P41AL.3	P41AL.2	P41AL.1	P41AL.0

Mnemonic: P41AL Address: 94h

BIT	NAME	FUNCTION
7-0	P41AL.[7:0]	The Base address register for comparator of P4.1. P41AL contains the low-order byte of address.

P4.1 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P41AH.7	P41AH.6	P41AH.5	P41AH.4	P41AH.3	P41AH.2	P41AH.1	P41AH.0

Mnemonic: P41AH Address: 95h

BIT	NAME	FUNCTION
7-0	P41AH.[7:0]	The Base address register for comparator of P4.1. P41AH contains the High-order byte of address.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiprocessor communication mode enable. The function of this bit is dependent on the serial port mode. Mode 0: No effect. Mode 1: Checking valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

Port 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7-0	P2.[7:0]	Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	-	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	-	Reserved
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

P4.2 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	P42AL.7	P42AL.6	P42AL.5	P42AL.4	P42AL.3	P42AL.2	P42AL.1	P42AL.0

Mnemonic: P42AL Address: ACh

BIT	NAME	FUNCTION
7-0	P42AL.[7:0]	The Base address register for comparator of P4.2. P42AL contains the low-order byte of address.

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic:P42AH Address: ADh

BIT	NAME	FUNCTION
7-0	P42AH.[7:0]	The Base address register for comparator of P4.2. P42AH contains the High-order byte of address.

Port 2 Expanded Control

Bit:	7	6	5	4	3	2	1	0
	P43CSIN	P42CSIN	P41CSIN	P40CSIN	-	-	-	-

Mnemonic: P2ECON Address:AEh

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. 1 : P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. 0 : P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$
6	P3.6	$\overline{WR}$
5	P3.5	T1
4	P3.4	T0

3	P3.3	$\overline{INT1}$
2	P3.2	$\overline{INT0}$
1	P3.1	TX
0	P3.0	RX

P4.3 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	P43AL.7	P43AL.6	P43AL.5	P43AL.4	P43AL.3	P43AL.2	P43AL.1	P43AL.0

Mnemonic: P43AL Address: B4h

BIT	NAME	FUNCTION
7-0	P43AL.[7:0]	The Base address register for comparator of P4.3. P43AL contains the low-order byte of address.

P4.3 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P43AH.7	P43AH.6	P43AH.5	P43AH.4	P43AH.3	P43AH.2	P43AH.1	P43AH.0

Mnemonic: P43AH Address: B5h

BIT	NAME	FUNCTION
7-0	P43AH.[7:0]	The Base address register for comparator of P4.3. P43AH contains the High-order byte of address.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	-	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
5	PT2	1: To set interrupt priority of Timer 2 is higher priority level.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

Chip Control

Bit:	7	6	5	4	3	2	1	0
	SWRESET	-	-	ENAUXRAM	0	0	FBOOTSL	FPRGEN

(F04KMODE)				(MUST SET 0)	(MUST SET 0)		

Mnemonic: CHPCON Address: BFh

BIT	NAME	FUNCTION
7	SWRESET(F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit can determine that the F04KBOOT mode is running.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
1	FBOOTSL	The Loader Program Location Select. 0: The Loader Program locates at the 64K/32K Byte flash memory bank. 1: The Loader Program locates at the 4KB flash memory bank.
0	FPROGEN	Flash EPROM Programming Enable 1: Enable. The microcontroller switches to the programming flash mode after entering the idle mode and waken up from interrupt. The microcontroller will execute the loader program while in on-chip programming mode. 0: Disable. The on-chip flash memory is read-only. In-system programmability is disabled.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	External interrupt 3 priority high if set
6	EX3	External interrupt 3 enable if set
5	IE3	If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
4	IT3	External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
3	PX2	External interrupt 2 priority high if set
2	EX2	External interrupt 2 enable if set
1	IE2	If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
0	IT2	External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Port 4 control A

Bit:	7	6	5	4	3	2	1	0
	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0

Mnemonic: P4CONA Address: C2h

BIT	NAME	FUNCTION
7,6	P41FUN1 P41FUN0	00: Mode 0. P4.1 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.1is a Read Strobe signal for chip select purpose. The address range depends on the SFR P41AH, P41AL, P41CMP1 and P41CMP0. 10: Mode 2. P4.1 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P41AH,P41AL,P41CMP1 and P41CMP0. 11: Mode 3. P4.1 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P41AH, P41AL, P41CMP1, and P41CMP0.
5,4	P41CMP1 P41CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P41AH, P41AL. 01: Compare the 15 high bits (A15-A1) of address bus with the base address register P41AH, P41AL. 10: Compare the 14 high bits (A15-A2) of address bus with the base address register P41AH, P41AL. 11: Compare the 8 high bits (A15-A8) of address bus with the base address register P41AH, P41AL.
3,2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P40FUN1, P40FUN0. .
1,0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P40CMP, P40CMP0.

Port 4 control B

Bit:	7	6	5	4	3	2	1	0
	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0

Mnemonic: P4CONB Address: C3h

BIT	NAME	FUNCTION
7,6	P43FUN1 P43FUN0	The P4.3 function control bits which are the similar definition as P43FUN1, P43FUN0. .
5,4	P43CMP1 P43CMP0	The P4.3 address comparator length control bits which are the similar definition as P43CMP1,P43CMP0.
3,2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P42FUN1, P42FUN0. .
1,0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P42CMP1,P42CMP0.

SFR program of address low

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Mnemonic: SFRAL Address: C4h

BIT	NAME	FUNCTION
7-0	SFRAL.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAL contains the low-order byte of address.

SFR program of address high

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH Address: C5h

BIT	NAME	FUNCTION
7-0	SFRAH.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAH contains the high-order byte of address.

SFR program For Data

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

SFRFD Address: C6h

BIT	NAME	FUNCTION
7-0	SFRFD.[7:0]	The programming data for on-chip flash memory in programming mode.

SFR for Program Control

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

SFRCN Address: C7h

BIT	NAME	FUNCTION
6	WFWIN	On-chip FLASH EPROM bank select for in-system programming. 0: 64K bytes FLASH EPROM bank is selected as destination for re-programming. 1: 4K bytes FLASH EPROM bank is selected as destination for re-programming.
5	OEN	FLASH EPROM output enable.
4	CEN	FLASH EPROM chip enable.
3-0	CTRL[3:0]	CTRL[3:0]: The flash control signals

Mode	CTRL<3:0>	WFWIN	OEN	CEN	SFRAH,SFRAL	SFRFD
Erase APROM	0010	0	1	0	X	X
Program APROM	0001	0	1	0	Address in	Data in

Read APROM	0000	0	0	0	Address in	Data out	

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: This bit is set when Timer 2 overflows. It can be set only if RCLK and TCLK are both 0. It is cleared only by software. Software can also set or clear this bit.
6	EXF2	Timer 2 External Flag: A negative transition on the T2EX pin (P1.1) or timer 2 overflow will cause this flag to set based on the CP / $\overline{RL2}$, EXEN2 bits. If set by a negative transition, this flag must be cleared by software. Setting this bit in software or detection of a negative transition on T2EX pin will force a timer interrupt if enabled.
5	RCLK	Receive Clock Flag: This bit determines the serial port 0 time-base when receiving data in serial modes 1 or 3. If it is 0, then timer 1 overflow is used for baud rate generation, otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.
4	TCLK	Transmit Clock Flag: This bit determines the serial port 0 time-base when transmitting data in modes 1 and 3. If it is set to 0, the timer 1 overflow is used to generate the baud rate clock otherwise timer 2 overflow is used. Setting this bit forces timer 2 in baud rate generator mode.
3	EXEN2	Timer 2 External Enable. This bit enables the capture/reload function on the T2EX pin if Timer 2 is not generating baud clocks for the serial port. If this bit is 0, then the T2EX pin will be ignored, otherwise a negative transition detected on the T2EX pin will result in capture or reload.
2	TR2	Timer 2 Run Control. This bit enables/disables the operation of timer 2. Clearing this bit will halt the timer 2 and preserve the current count in TH2, TL2.
1	C / $\overline{T2}$	Counter/Timer Select. This bit determines whether timer 2 will function as a timer or a counter. Independent of this bit, the timer will run at 2 clocks per tick when used in baud rate generator mode.
0	CP / $\overline{RL2}$	Capture/Reload Select. This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will be ignored and the timer will function in an auto-reload mode following each overflow. If the bit is 0 then auto-reload will occur when timer 2 overflows or a falling edge is detected on T2EX pin if EXEN2 = 1. If this bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX pin if EXEN2 = 1.

Timer 2 Capture LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

BIT	NAME	FUNCTION
7-0	RCAP2L.[7:0]	This register is used to capture the TL2 value when a timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 Capture MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2h.7	RCAP2h.6	RCAP2h.5	RCAP2h.4	RCAP2h.3	RCAP2h.2	RCAP2h.1	RCAP2h.0

Mnemonic: RCAP2H Address: CBh

BIT	NAME	FUNCTION
7-0	RCAP2H.[7:0]	This register is used to capture the TH2 value when a timer 2 is configured in capture mode. RCAP2H is also used as the MSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

BIT	NAME	FUNCTION
7-0	TL2.[7:0]	Timer 2 LSB

Timer 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

BIT	NAME	FUNCTION
7-0	TH2.[7:0]	Timer 2 MSB

Program Status Word PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION

7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register bank selection bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

Port 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: D8h

Port 4, SFR P4 at address D8H, is a 4-bit multipurpose programmable I/O port. Each bit can be configured individually by software. The Port 4 has four different operation mode:

In mode 0, P4.0–P4.3 is a bi-directional I/O port which is same as port 1. P4.2 and P4.3 also serve as external interrupt $\overline{INT3}$ and $\overline{INT2}$ if enabled.

In mode 1, P4.0–P4.3 are read data strobe signals which are synchronized with $\overline{RD}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

In mode 2 , P4.0–P4.3 are write data strobe signals which are synchronized with $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

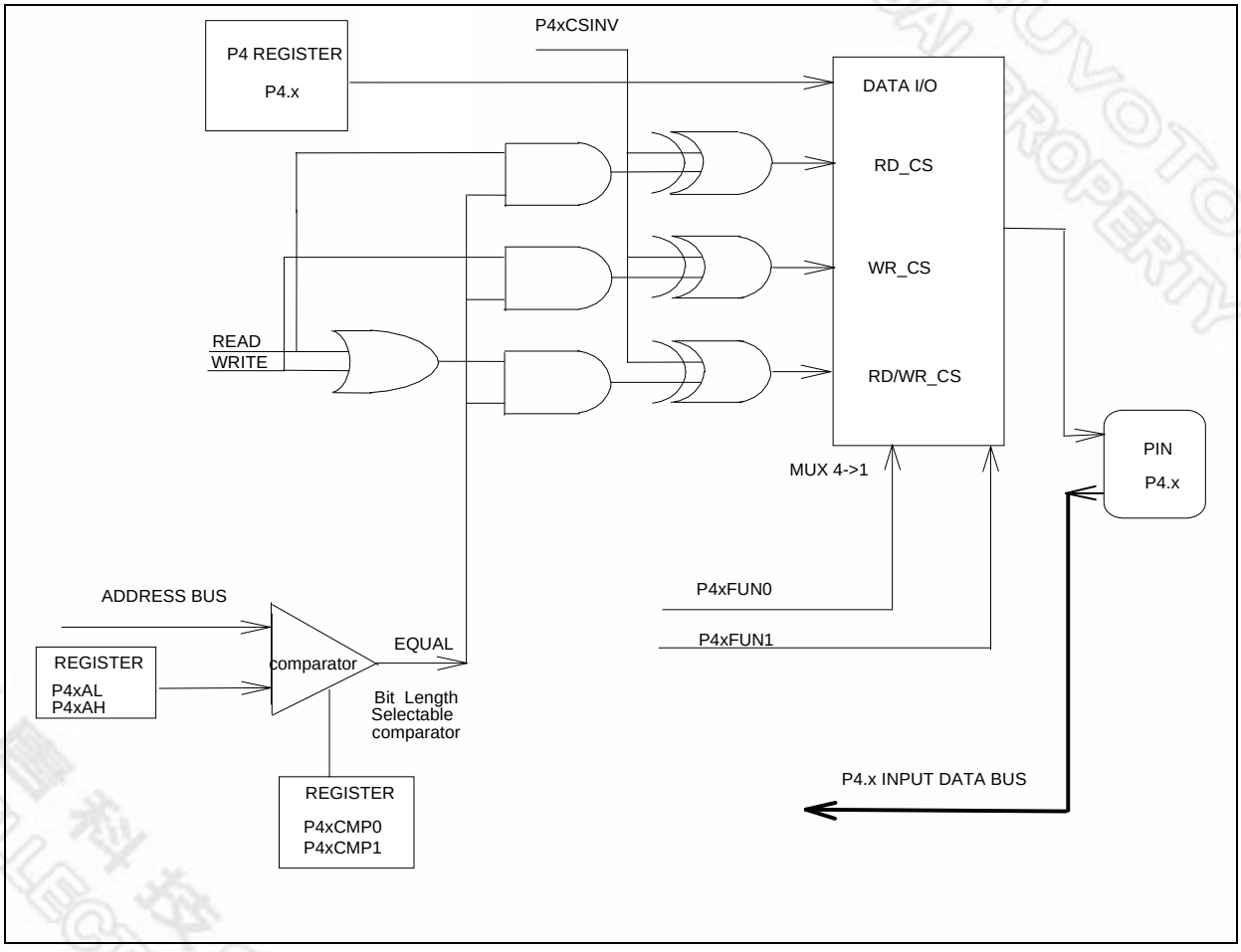
In mode 3, P4.0–P4.3 are read data strobe signals which are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These signals can be used as chip-select signals for external peripherals.

When Port 4 is configured with the feature of chip-select signals, the chip-select signal address range depends on the contents of the SFR P4xAH, P4xAL, P4CONA and P4CONB. The registers P4xAH and P4xAL contain the 16-bit base address of P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H ~1237H and positive polarity, and P4.1~P4.3 are used as general I/O ports.

```
MOV  P40AH,#12H
MOV  P40AL,#34H              ;Define the base I/O address 1234H for P4.0 as an special function
MOV  P4CONA,#00001010B       ;Define the P4.0 as a write strobe signal pin and the comparator
MOV  P4CONB,#00H             ;P4.1~P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON,#10H             ;Write the P40SINV =1 to inverse the P4.0 write strobe polarity
                             ;default is negative.
```

Then any instruction MOVX @DPTR,A (with DPTR=1234H~1237H) will generate the positive polarity write strobe signal at pin P4.0 . And the instruction MOV P4,#XX will output the bit3 to bit1 of data #XX to pin P4.3~ P4.1.



The Port 4 Structure Diagram

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

Bit	Name	Function
7-0	ACC	The A or ACC register is the standard 8052 accumulator.

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

Bit	Name	Function
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

Chip Enable Register

Bit:	7	6	5	4	3	2	1	0
	CHPENR.7	CHPENR.6	CHPENR.5	CHPENR.4	CHPENR.3	CHPENR.2	CHPENR.1	CHPENR.0

Mnemonic: CHPENR Address: F6h

The CHPCON is read only by default .You must write #87,#59H sequentially to this special register CHPENR to enable the CHPCON write attribute, and write other value to disable CHPCON write attribute. This register protects from writing to the CHPCON register carelessly.

10 INSTRUCTION

The W78E516D/W78E058D series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly the same.

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
NOP	00	1	12
ADD A, R0	28	1	12
ADD A, R1	29	1	12
ADD A, R2	2A	1	12
ADD A, R3	2B	1	12
ADD A, R4	2C	1	12
ADD A, R5	2D	1	12
ADD A, R6	2E	1	12
ADD A, R7	2F	1	12
ADD A, @R0	26	1	12
ADD A, @R1	27	1	12
ADD A, direct	25	2	12
ADD A, #data	24	2	12
ADDC A, R0	38	1	12
ADDC A, R1	39	1	12
ADDC A, R2	3A	1	12
ADDC A, R3	3B	1	12
ADDC A, R4	3C	1	12
ADDC A, R5	3D	1	12
ADDC A, R6	3E	1	12
ADDC A, R7	3F	1	12
ADDC A, @R0	36	1	12
ADDC A, @R1	37	1	12
ADDC A, direct	35	2	12
ADDC A, #data	34	2	12
SUBB A, R0	98	1	12
SUBB A, R1	99	1	12
SUBB A, R2	9A	1	12
SUBB A, R3	9B	1	12
SUBB A, R4	9C	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
SUBB A, R5	9D	1	12
SUBB A, R6	9E	1	12
SUBB A, R7	9F	1	12
SUBB A, @R0	96	1	12
SUBB A, @R1	97	1	12
SUBB A, direct	95	2	12
SUBB A, #data	94	2	12
INC A	04	1	12
INC R0	08	1	12
INC R1	09	1	12
INC R2	0A	1	12
INC R3	0B	1	12
INC R4	0C	1	12
INC R5	0D	1	12
INC R6	0E	1	12
INC R7	0F	1	12
INC @R0	06	1	12
INC @R1	07	1	12
INC direct	05	2	12
INC DPTR	A3	1	24
DEC A	14	1	12
DEC R0	18	1	12
DEC R1	19	1	12
DEC R2	1A	1	12
DEC R3	1B	1	12
DEC R4	1C	1	12
DEC R5	1D	1	12
DEC R6	1E	1	12
DEC R7	1F	1	12
DEC @R0	16	1	12
DEC @R1	17	1	12
DEC direct	15	2	12
MUL AB	A4	1	48
DIV AB	84	1	48

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
DA A	D4	1	12
ANL A, R0	58	1	12
ANL A, R1	59	1	12
ANL A, R2	5A	1	12
ANL A, R3	5B	1	12
ANL A, R4	5C	1	12
ANL A, R5	5D	1	12
ANL A, R6	5E	1	12
ANL A, R7	5F	1	12
ANL A, @R0	56	1	12
ANL A, @R1	57	1	12
ANL A, direct	55	2	12
ANL A, #data	54	2	12
ANL direct, A	52	2	12
ANL direct, #data	53	3	24
ORL A, R0	48	1	12
ORL A, R1	49	1	12
ORL A, R2	4A	1	12
ORL A, R3	4B	1	12
ORL A, R4	4C	1	12
ORL A, R5	4D	1	12
ORL A, R6	4E	1	12
ORL A, R7	4F	1	12
ORL A, @R0	46	1	12
ORL A, @R1	47	1	12
ORL A, direct	45	2	12
ORL A, #data	44	2	12
ORL direct, A	42	2	12
ORL direct, #data	43	3	24
XRL A, R0	68	1	12
XRL A, R1	69	1	12
XRL A, R2	6A	1	12
XRL A, R3	6B	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
XRL A, R4	6C	1	12
XRL A, R5	6D	1	12
XRL A, R6	6E	1	12
XRL A, R7	6F	1	12
XRL A, @R0	66	1	12
XRL A, @R1	67	1	12
XRL A, direct	65	2	12
XRL A, #data	64	2	12
XRL direct, A	62	2	12
XRL direct, #data	63	3	24
CLR A	E4	1	12
CPL A	F4	1	12
RL A	23	1	12
RLC A	33	1	12
RR A	03	1	12
RRC A	13	1	12
SWAP A	C4	1	12
MOV A, R0	E8	1	12
MOV A, R1	E9	1	12
MOV A, R2	EA	1	12
MOV A, R3	EB	1	12
MOV A, R4	EC	1	12
MOV A, R5	ED	1	12
MOV A, R6	EE	1	12
MOV A, R7	EF	1	12
MOV A, @R0	E6	1	12
MOV A, @R1	E7	1	12
MOV A, direct	E5	2	12
MOV A, #data	74	2	12
MOV R0, A	F8	1	12
MOV R1, A	F9	1	12
MOV R2, A	FA	1	12
MOV R3, A	FB	1	12
MOV R4, A	FC	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
MOV R5, A	FD	1	12
MOV R6, A	FE	1	12
MOV R7, A	FF	1	12
MOV R0, direct	A8	2	24
MOV R1, direct	A9	2	24
MOV R2, direct	AA	2	24
MOV R3, direct	AB	2	24
MOV R4, direct	AC	2	24
MOV R5, direct	AD	2	24
MOV R6, direct	AE	2	24
MOV R7, direct	AF	2	24
MOV R0, #data	78	2	12
MOV R1, #data	79	2	12
MOV R2, #data	7A	2	12
MOV R3, #data	7B	2	12
MOV R4, #data	7C	2	12
MOV R5, #data	7D	2	12
MOV R6, #data	7E	2	12
MOV R7, #data	7F	2	12
MOV @R0, A	F6	1	12
MOV @R1, A	F7	1	12
MOV @R0, direct	A6	2	24
MOV @R1, direct	A7	2	24
MOV @R0, #data	76	2	12
MOV @R1, #data	77	2	12
MOV direct, A	F5	2	12
MOV direct, R0	88	2	24
MOV direct, R1	89	2	24
MOV direct, R2	8A	2	24
MOV direct, R3	8B	2	24
MOV direct, R4	8C	2	24
MOV direct, R5	8D	2	24
MOV direct, R6	8E	2	24

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
MOV direct, R7	8F	2	24
MOV direct, @R0	86	2	24
MOV direct, @R1	87	2	24
MOV direct, direct	85	3	24
MOV direct, #data	75	3	24
MOV DPTR, #data 16	90	3	24
MOVC A, @A+DPTR	93	1	24
MOVC A, @A+PC	83	1	24
MOVX A, @R0	E2	1	24
MOVX A, @R1	E3	1	24
MOVX A, @DPTR	E0	1	24
MOVX @R0, A	F2	1	24
MOVX @R1, A	F3	1	24
MOVX @DPTR, A	F0	1	24
PUSH direct	C0	2	24
POP direct	D0	2	24
XCH A, R0	C8	1	12
XCH A, R1	C9	1	12
XCH A, R2	CA	1	12
XCH A, R3	CB	1	12
XCH A, R4	CC	1	12
XCH A, R5	CD	1	12
XCH A, R6	CE	1	12
XCH A, R7	CF	1	12
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24
JB bit, rel	20	3	24
JNB bit, rel	30	3	24
JBC bit, rel	10	3	24
CJNE A, direct, rel	B5	3	24
CJNE A, #data, rel	B4	3	24
CJNE @R0, #data, rel	B6	3	24
CJNE @R1, #data, rel	B7	3	24
CJNE R0, #data, rel	B8	3	24
CJNE R1, #data, rel	B9	3	24
CJNE R2, #data, rel	BA	3	24
CJNE R3, #data, rel	BB	3	24
CJNE R4, #data, rel	BC	3	24
CJNE R5, #data, rel	BD	3	24

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
CJNE R6, #data, rel	BE	3	24
CJNE R7, #data, rel	BF	3	24
DJNZ R0, rel	D8	2	24
DJNZ R1, rel	D9	2	24
DJNZ R5, rel	DD	2	24
DJNZ R2, rel	DA	2	24
DJNZ R3, rel	DB	2	24
DJNZ R4, rel	DC	2	24
DJNZ R6, rel	DE	2	24
DJNZ R7, rel	DF	2	24
DJNZ direct, rel	D5	3	24

Table 10-1: Instruction Set for W78E516D/W78E058D

11 INSTRUCTION TIMING

A machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods or 1us if the oscillator frequency is 12MHz.

Each state is divided into a Phase 1 half and a Phase 2 half. The fetch/execute sequences in states and phases for various kinds of instructions. Normally two program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the Program Counter is not incremented. Execution of a one-cycle instruction begins during State 1 of the machine cycle, when the op-codes is latched into the Instruction Register. A second fetch occurs during S4 of the same machine cycle. Execution is complete at the end of State 6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions.

The fetch/execute sequences are the same whether the Program Memory is internal or external to the chip. Execution times do not depend on whether the Program Memory is internal or external.

the signals and timing involved in program fetches when the Program Memory is external. If Program Memory is external, then the Program Memory read strobe PSEN is normally activated twice per machine cycle. If an access to external Data Memory occurs, two PSENs pulse are skipped, because the address and data bus are being used for the Data Memory access. Note that a Data Memory bus cycle takes twice as much time as a Program Memory bus cycle.

12 POWER MANAGEMENT

The W78E516D/W78E058D has several features that help the user to control the power consumption of the device. The power saved features have basically the POWER DOWN mode and the IDLE mode of operation.

12.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 24 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately.

12.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W78E516D/W78E058D will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detects. An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode.

The W78E516D/W78E058D can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the high level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there.

13 RESET CONDITIONS

The user has several hardware related options for placing the W78E516D/W78E058D into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

13.1 Sources of reset

13.1.1 External Reset

The device continuously samples the RST pin at state S5P2 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles (24 clock cycles) to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset. For more timing descript, please reference the character 21.4.5 (Page 79).

Once the device is in reset condition, it will remain so as long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition.

13.1.2 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

13.1.3 Software Reset

The W78E516D/W78E058D offers a software reset to switch back to the AP Flash EPROM. Setting CHPCON bits 0, 1 and 7 to logic-1 creates a software reset to reset the CPU.

13.1.4 RESET STATE

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the VDD falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have 0FFh written into them which puts the port pins in a high state.

Interrupts

The W78E516D/W78E058D has a 2 priority level interrupt structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

13.2 Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts $\overline{INT2}$ and $\overline{INT3}$. By default, the individual interrupt flag corresponding to external interrupt 2 to 3 must be cleared manually by software.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts, at once.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Timer 2 Overflow	002Bh
External Interrupt 2	0033h	External Interrupt 3	003Bh

Table 13- 1 W78E516D/W78E058D interrupt vector table

13.3 Priority Level Structure

There are two priority levels for the interrupts high, low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being executed.
3. The current instruction does not involve a write to IE, IP, XICON registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on below table. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of 2 priority levels by setting or clearing bits in the IP registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and external interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Flag cleared by	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	Hardware, software	1(highest)	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	Hardware, software	2	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, software	3	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, software	4	No
Serial Port	RI + TI	0023H	ES (IE.4)	Software	5	No
Timer 2 Over-flow/Match	TF2	002BH	ET2 (IE.5)	Software	6	No
External Interrupt 2	XICON	0033H	EX2 (XICON.2)	Hardware, software	7	Yes
External Interrupt 3	XICON	003BH	EX3 (XICON.6)	Hardware, software	8(lowest)	Yes

Table 13- 2 Summary of interrupt sources

13.4 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ and $\overline{INT1}$, they are sampled at S5P2 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, IP and then executes a MUL or DIV instruction.

13.5 Interrupt Inputs

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is high for at least

one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the W78E516D/W78E058D is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

14 PROGRAMMABLE TIMERS/COUNTERS

The W78E516D/W78E058D series have Three 16-bit programmable timer/counters, a machine cycle equals 12 or 6 oscillator periods, and it depends on 12T mode or 6T mode that the user configured this device.

14.1 Timer/Counters 0 & 1

W78E516D/W78E058D has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

14.2 Time-Base Selection

W78E516D/W78E058D provides users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on W78E516D/W78E058D and the standard 8051 can be matched. This is the default mode of operation of the W78E516D/W78E058D timers.

14.2.1 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (Timer 0) or T1 (Timer 1). For clock cycles, the time base be 1/12 speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated in next figure below.

14.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of 0FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if

enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

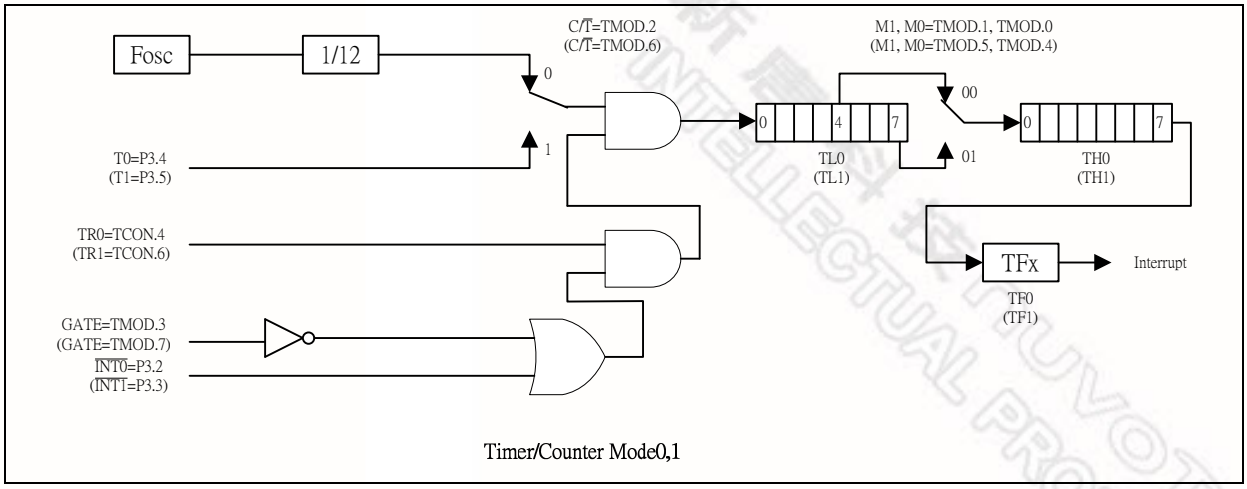


Figure 14- 1 Timer/Counters 0 & 1 in Mode 0,1

14.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$. As in the other two modes 0 and 1 mode 2 allows counting of clock/12 or pulses on pin Tn.

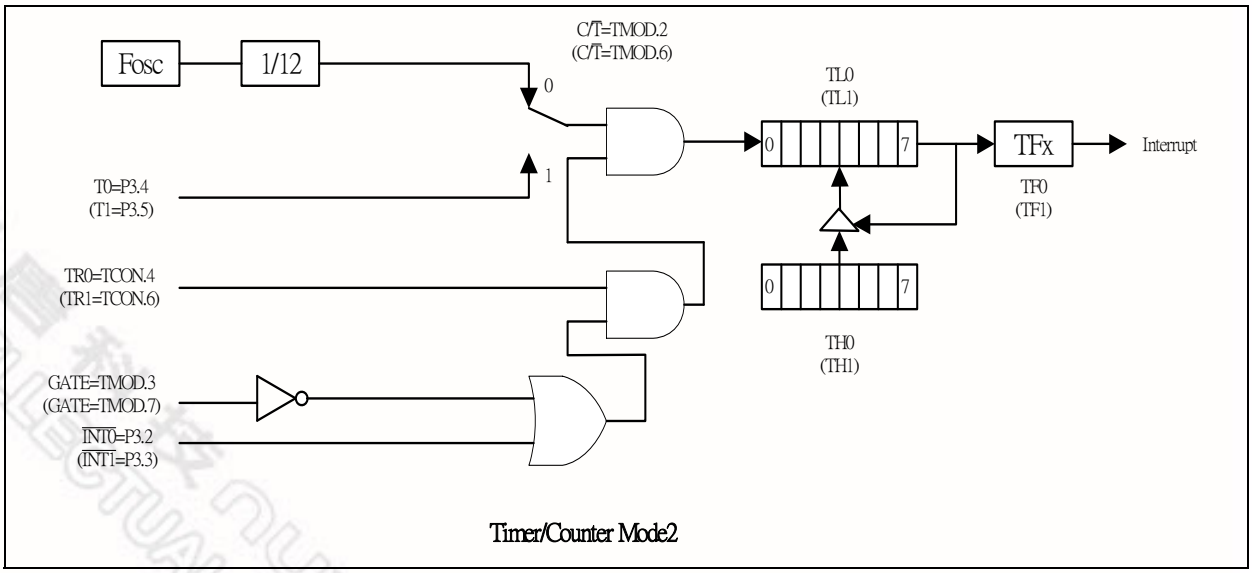


Figure 14- 2 Timer/Counter 0 & 1 in Mode 2

14.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

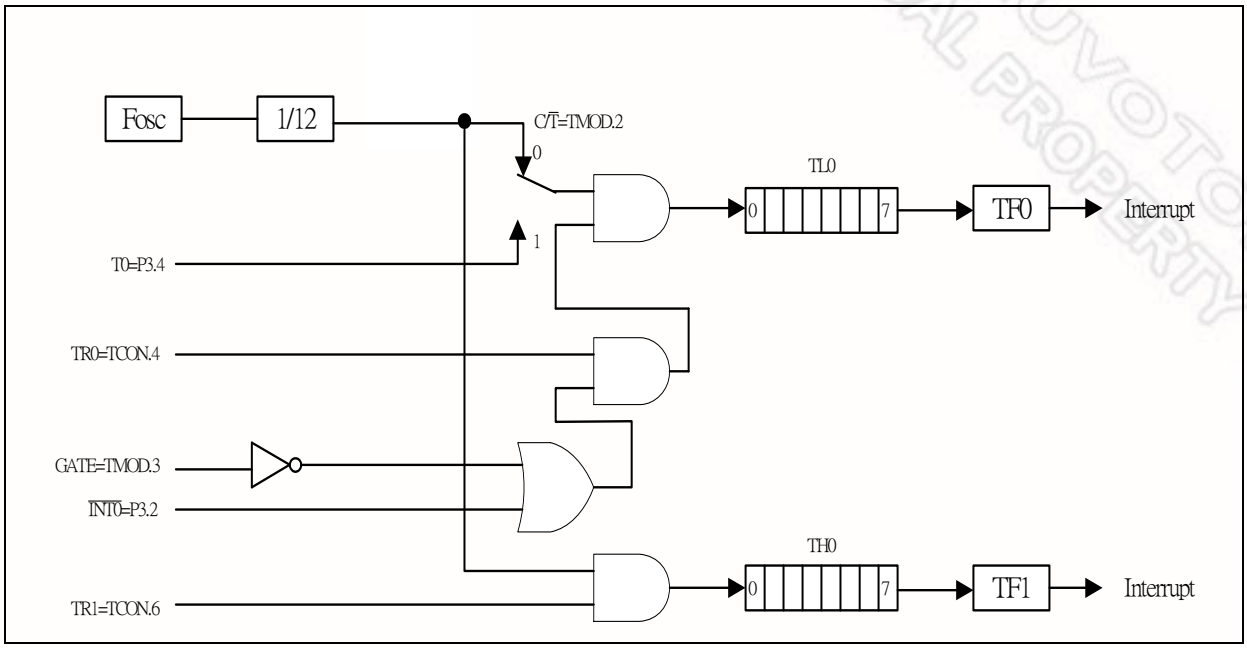


Figure 14-3 Timer/Counter Mode 3

14.3 Timer/Counter 2

Timer/Counter 2 is a 16 bit counter. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/T2 = 1) or the crystal oscillator, which is divided by 12 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

14.3.1 Capture Mode

The capture mode is enabled by setting the $CP/\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from 0FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will

also generate an interrupt.

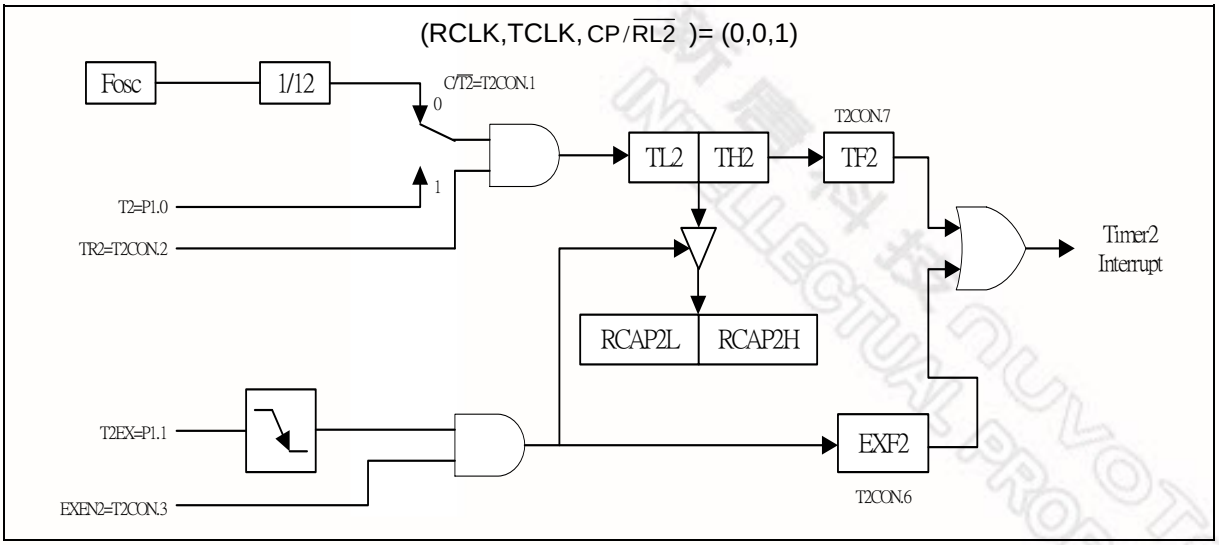


Figure 14-4 16-Bit Capture Mode

14.3.2 Auto-Reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the CP / RL2 bit in the T2CON register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from 0FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

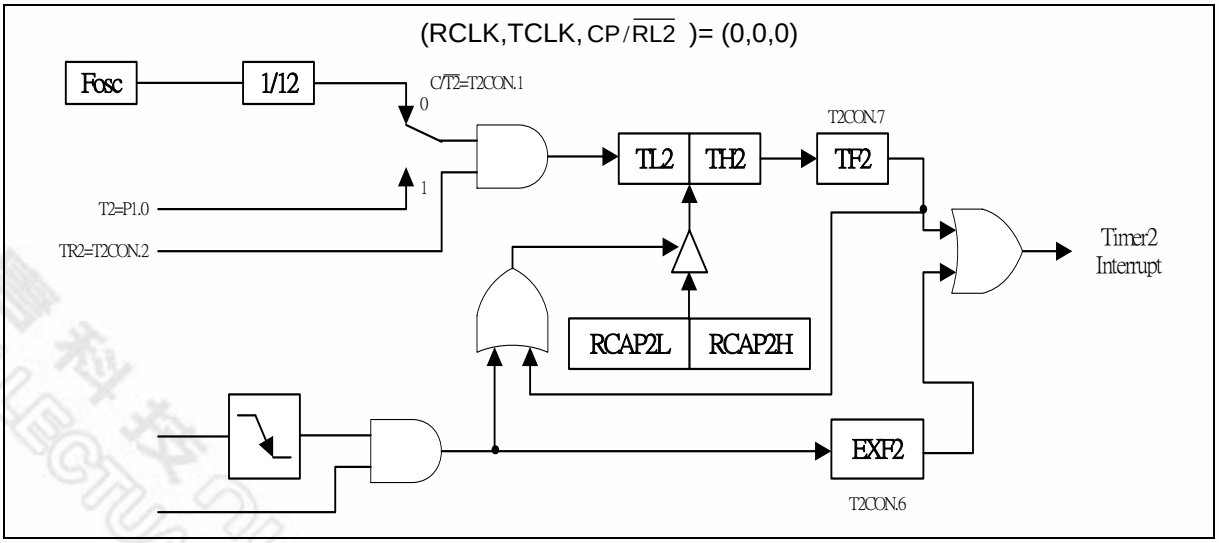


Figure 14- 5 16-Bit Auto-reload Mode, Counting Up

14.3.3 Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from 0FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

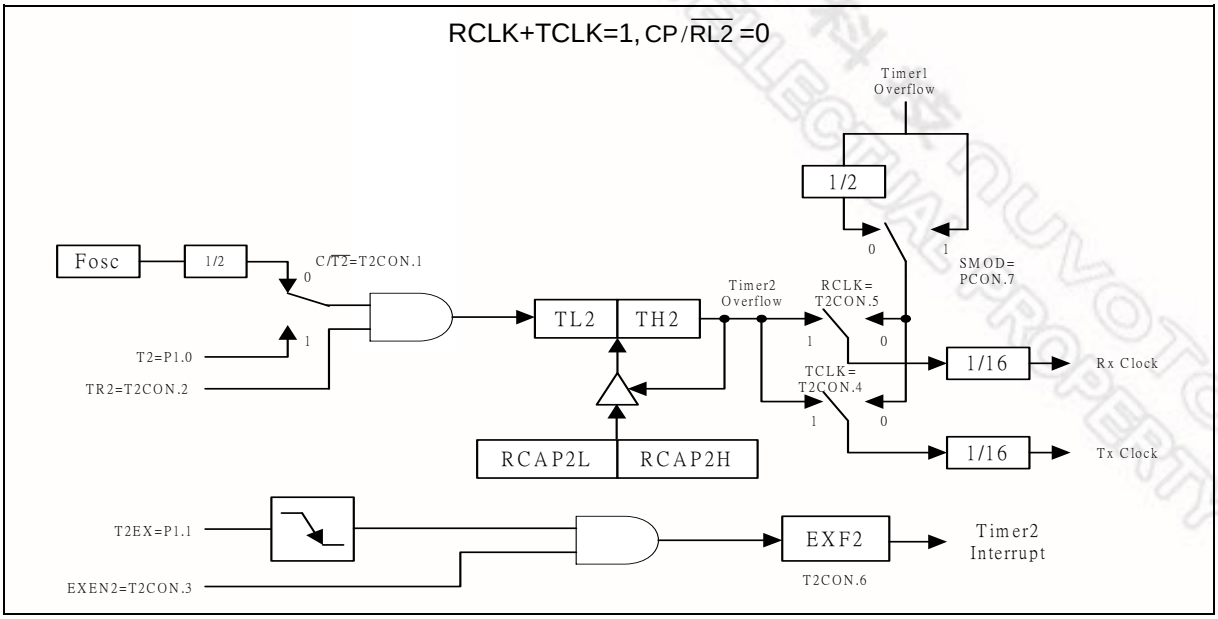


Figure 14- 6 Baud Rate Generator Mode

15 WATCHDOG TIMER

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

ENW : Enable watchdog if set.

CLRW : Clear watchdog timer and Pre-scalar if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watchdog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watchdog Pre-scalar timer select. Pre-scalar is selected when set PS2–0 as follows:

PS2	PS1	PS0	Pre-scalar select
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

The time-out period is obtained using the following equation:

$$\frac{1}{OSC} \times 2^{14} \times \Pr e - scalar \times 1000 \times 12ms \quad \text{(12T mode)}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, Pre-scalar and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.

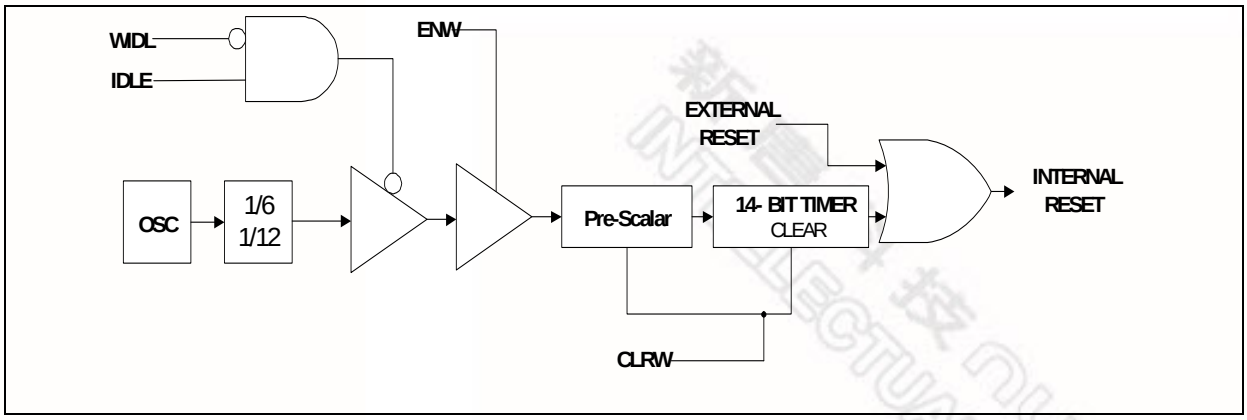


Figure 15- 1 Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	Watchdog time-out period
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

Table 15- 1 Watch-Dog time-out period

16 SERIAL PORT

Serial port in this device is a full duplex port. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W78E516D/W78E058D.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

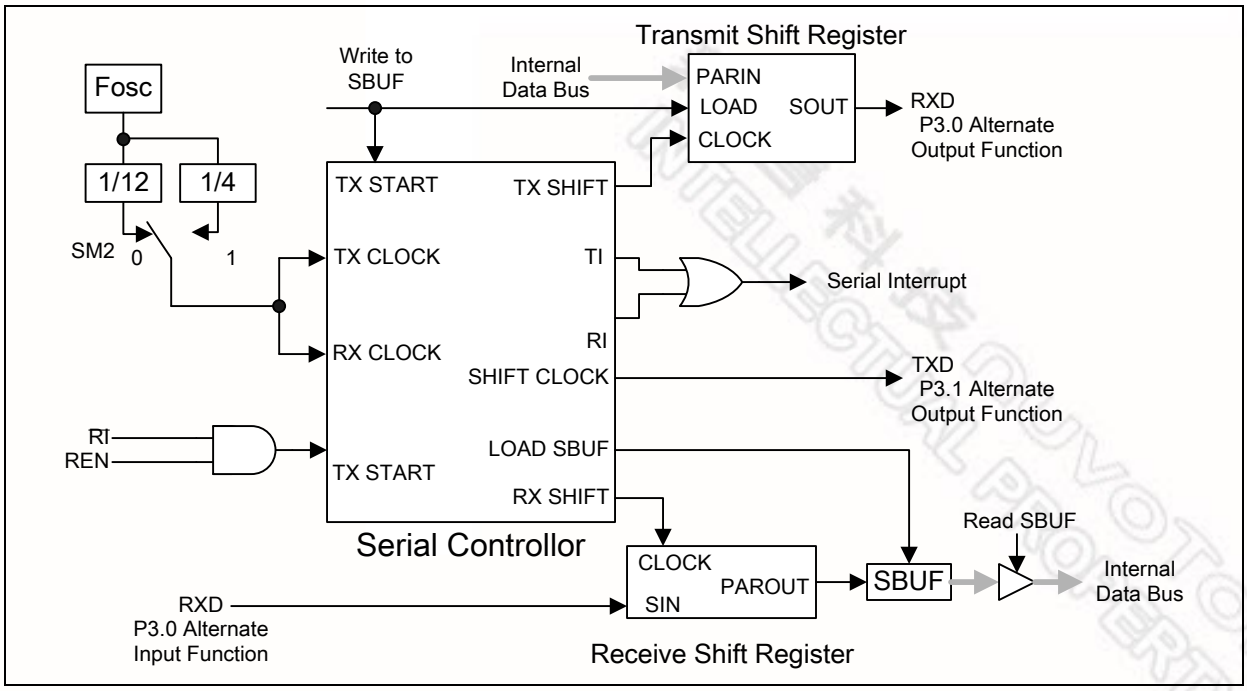


Figure 16- 1 Serial port mode 0

The TI flag is set high in S6P2 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in S6P2 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive mode, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basie. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

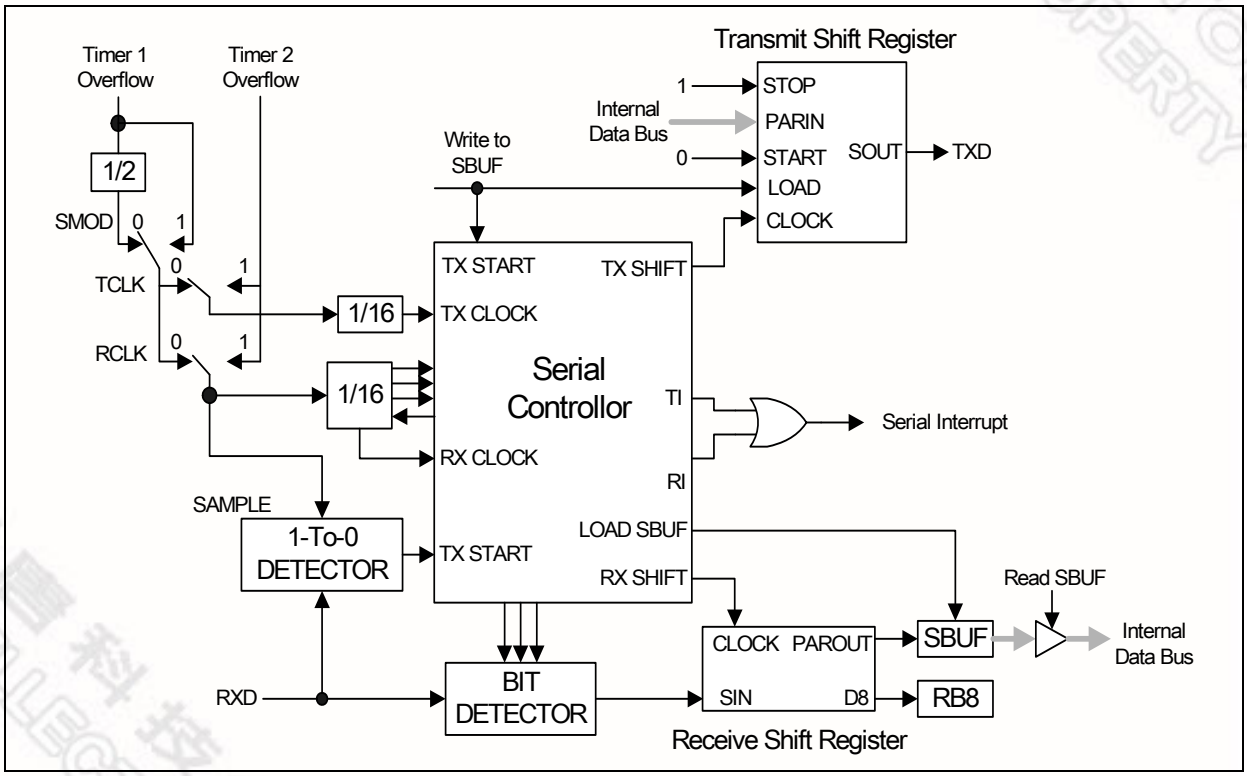


Figure 16- 2 Serial port mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a pro-

grammable 9th bit (TB8) and a stop bit (1). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

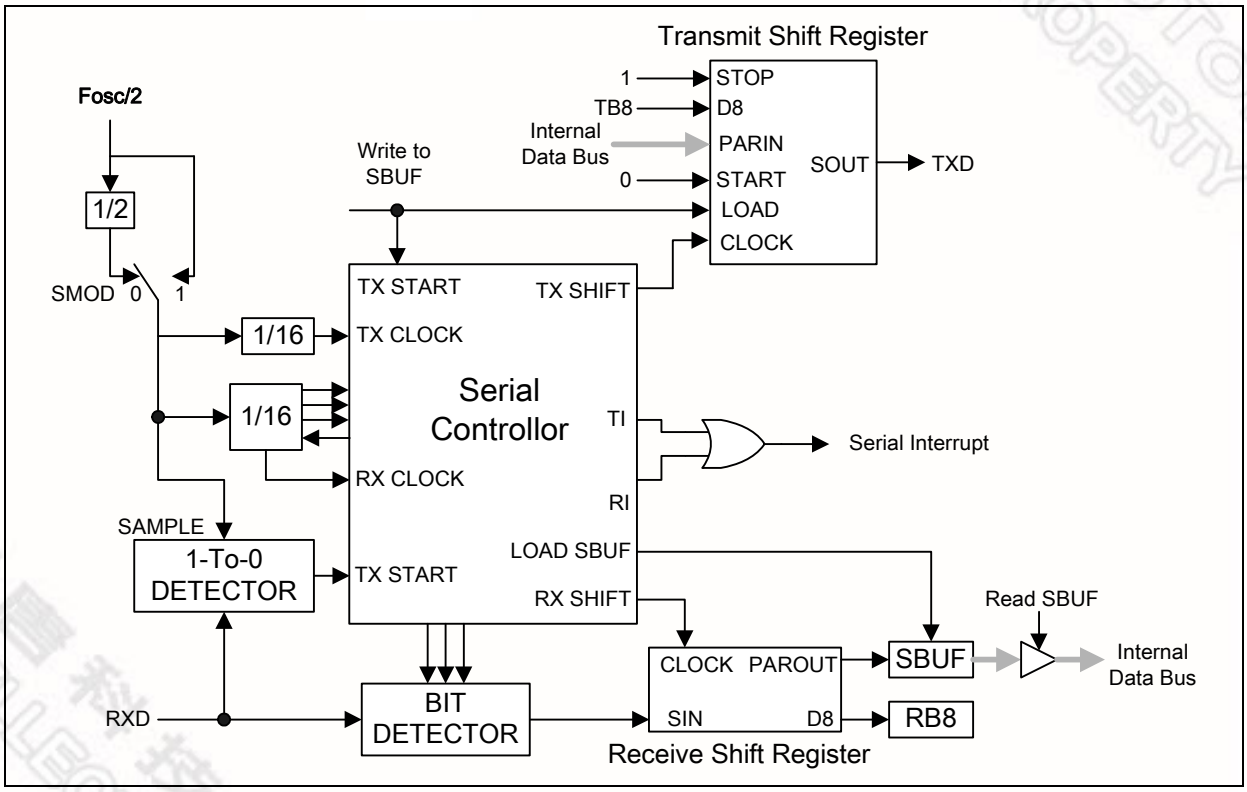


Figure 16- 3 Serial port mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

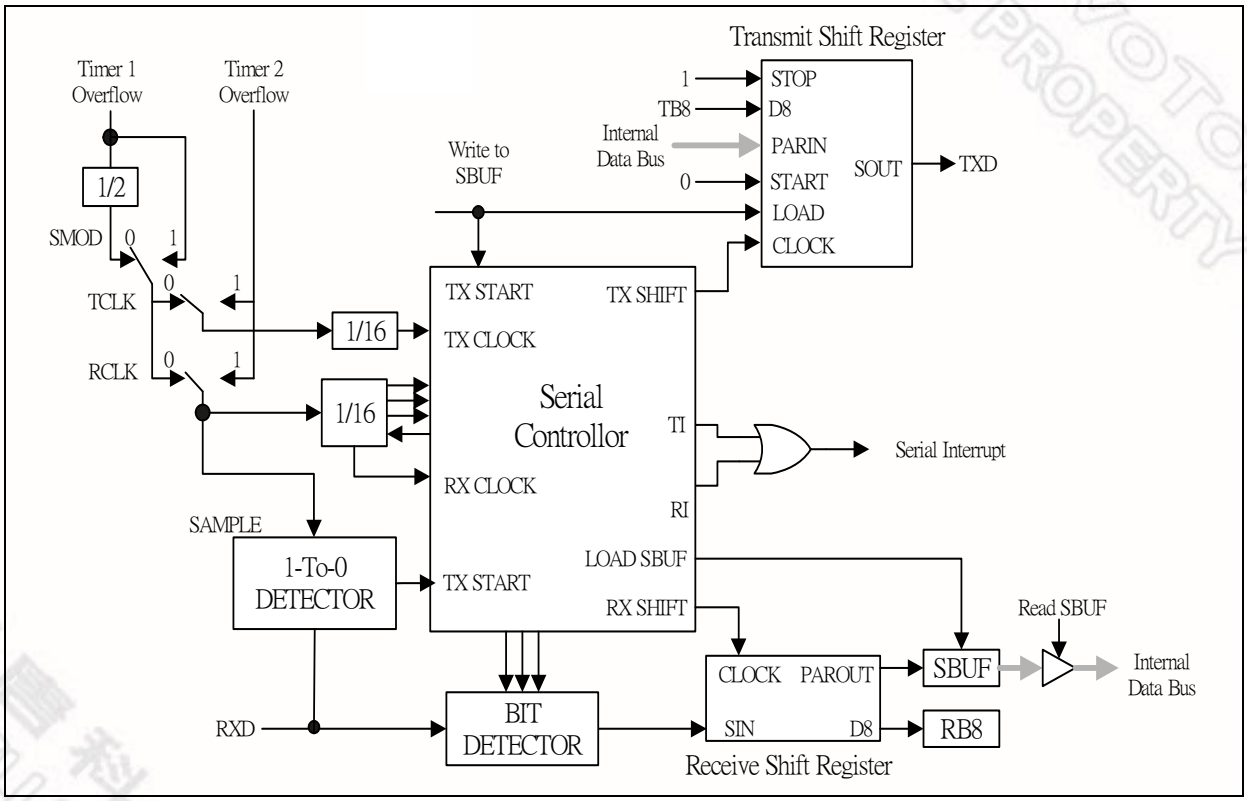


Figure 15- 4 Serial port mode 3

SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit Function
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None

1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

Table 16- 1 Serial Ports Modes

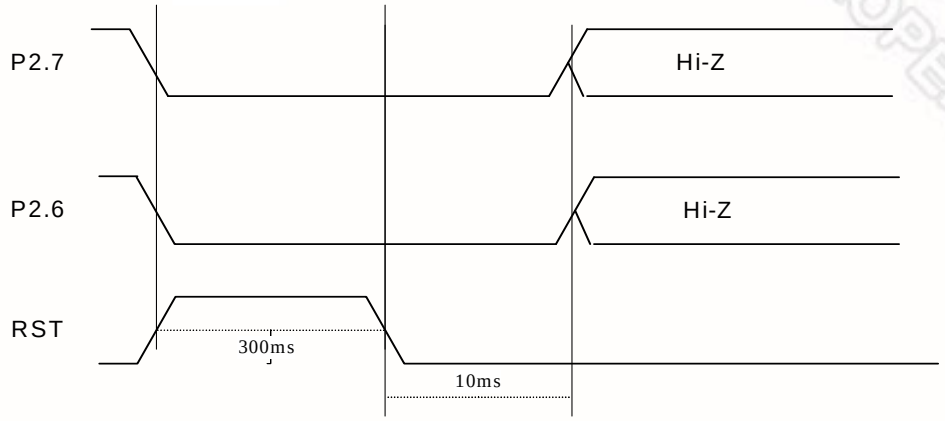
17 F04KBOOT MODE (BOOT FROM 4K BYTES OF LDROM)

The W78E516D/W78E058D boots from APROM program memory(64K/32K bytes) by default at power on reset or reset-pin reset. On some occasions, user can force the W78E516D/W78E058D booting from the LDROM program memory (4K bytes) at power on reset or external reset. The settings for this special mode as follow.

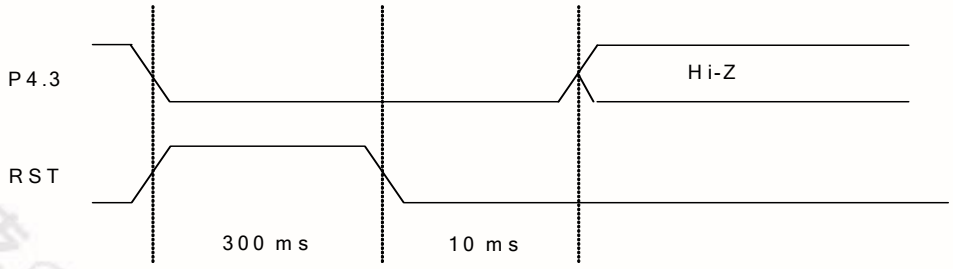
F04KBOOT MODE

P4.3	P2.7	P2.6	Mode
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

The Reset Timing For Entering F04KBOOT Mode



The Reset Timing For Entering F04KBOOT Mode



NOTE1: The possible situation that you need to enter F04KBOOT mode is when the APROM program can not run normally and W78E516D/W78E058D can not jump to LDROM to execute on chip pro-

gramming function. Then you can use this F04KBOOT mode to force the W78E516D/W78E058D jump to LDROM and run on chip programming procedure. When you design your system, you can connect the pins P26, P27 to switches or jumpers. For example in a CD ROM system, you can connect the P26 and P27 to PLAY and EJECT buttons on the panel. When the APROM program is fail to execute the normal application program. User can press both two buttons at the same time and then switch on the power of the personal computer to force the W78E516D/W78E058D to enter the F04KBOOT mode. After power on of personal computer, you can release both PLAY and EJECT button.

NOTE2: In application system design, user must take care the P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W78E516D/W78E058D entering the programming mode or F04KBOOT mode in normal operation.

18 ISP(IN-SYSTEM PROGRAMMING)

ISP is the ability of programmable MCU to be programmed while F/W code in AP-ROM or LD-ROM (ISP work voltage 3.3-5.5V).

The W78E058D/516D equips one 32K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E058D/516D allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E058D/516D achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

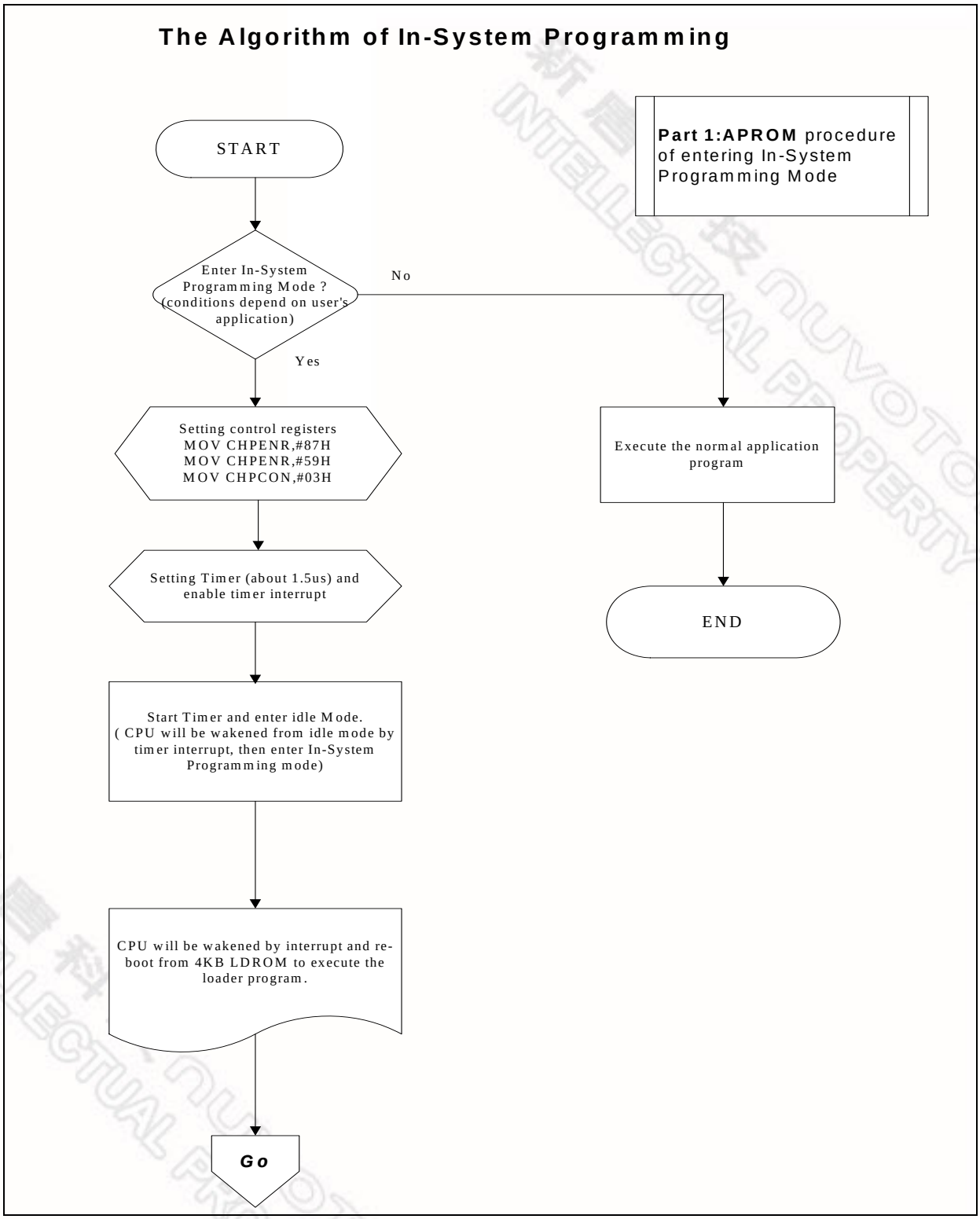
SFRCN: The control byte of on-chip ROM programming mode.

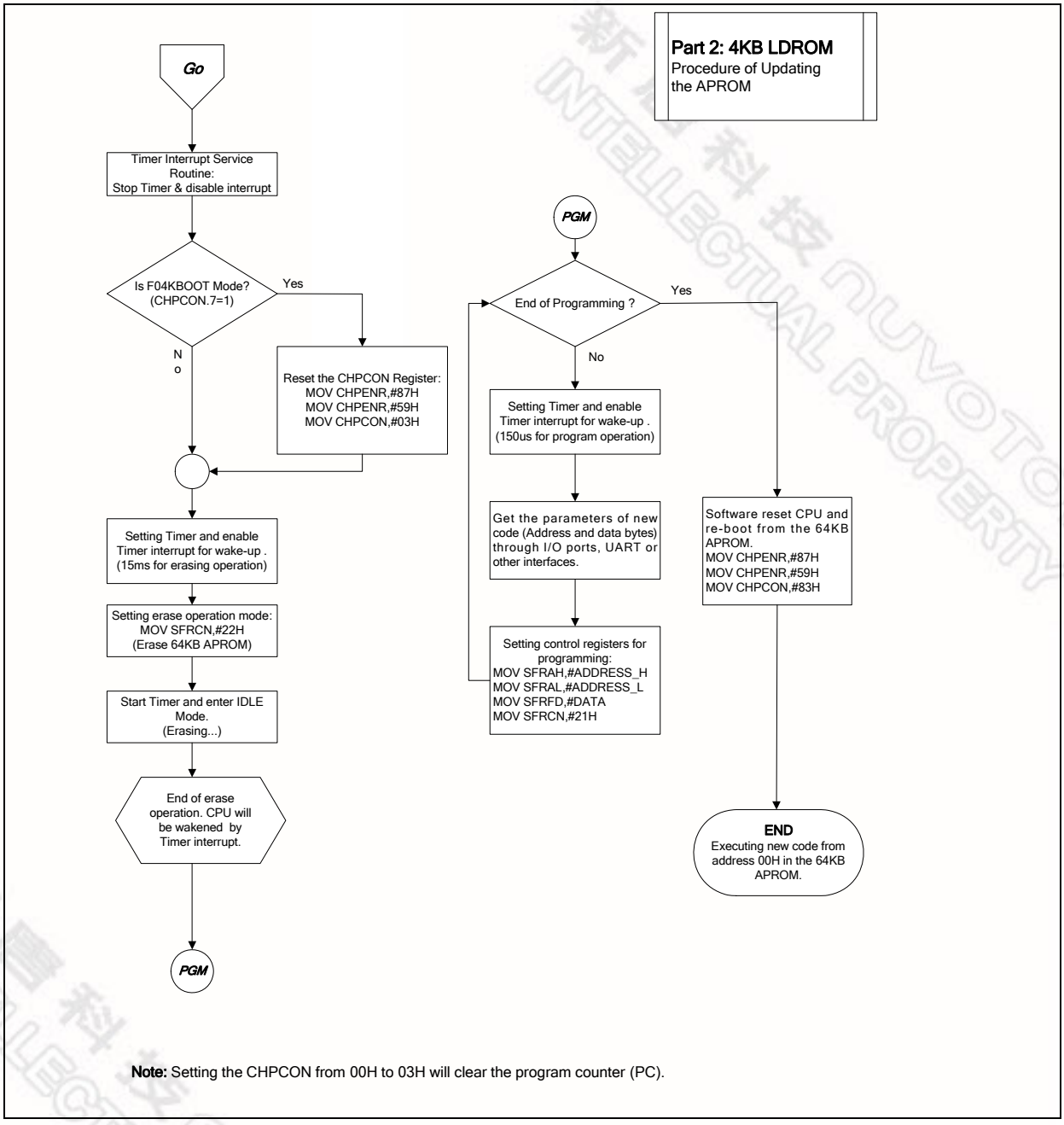
SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. 0: 32K/64K bytes ROM bank is selected as destination for re-programming. 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL [3:0]	The flash control signals

MODE	WFWIN	OEN	CEN	CTRL<3:0>	SFRAH, SFRAL	SFRFD
Erase 32KB/64KB APROM	0	1	0	0010	X	X
Program 32KB/64KB APROM	0	1	0	0001	Address in	Data in
Read 32KB/64KB APROM	0	0	0	0000	Address in	Data out
Erase 4KB LDROM	1	1	0	0010	X	X
Program 4KB LDROM	1	1	0	0001	Address in	Data in
Read 4KB LDROM	1	0	0	0000	Address in	Data out

The Algorithm of In-System Programming





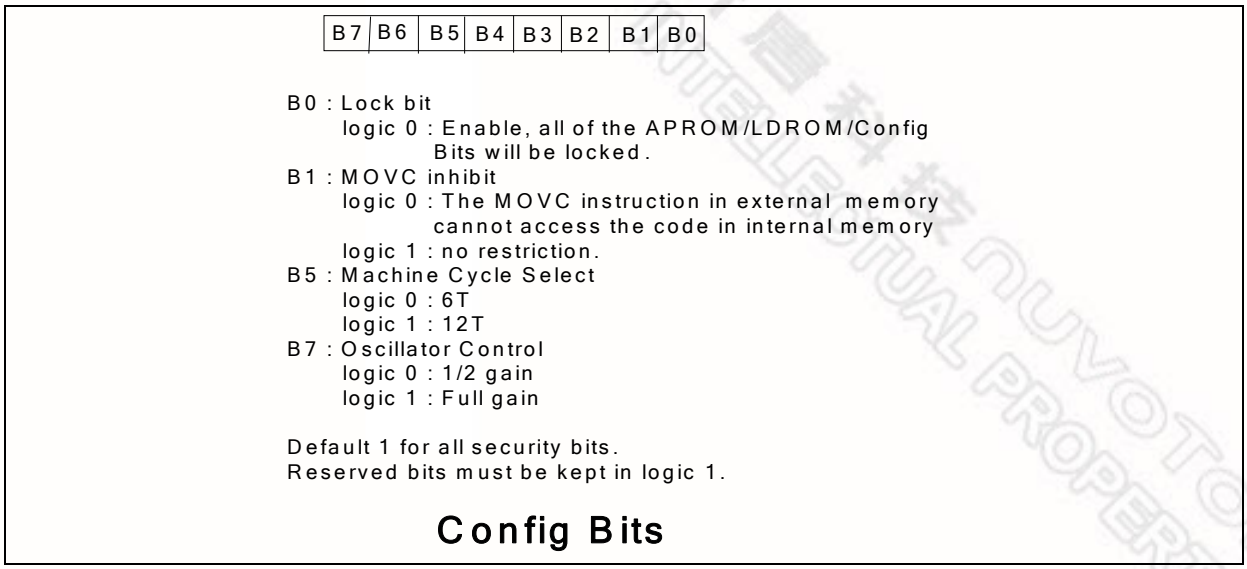
Note: Setting the CHPCON from 00H to 03H will clear the program counter (PC).

19 CONFIG BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E516D/W78E058D has several Special Setting Registers, including the Security Register and Company/Device ID Registers, which can not be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They

can only be reset through erase-all operation. The contents of the Company ID and Device ID registers have been set in factory.



Bit 0: Lock bits

This bit is used to protect the customer's program code in the W78E516D/W78E058D. It may be set after the programmer finishes the programming and verifies sequence. Once these bits are set to logic 0, both the FLASH data and Special Setting Registers can not be accessed again.

Bit 1: Movc inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Bit 5: Machine Cycle Select

This bit is select MCU core, default value is logic 1(12T). Once these bits are set to logic 0, the MCU core is 6T.

Bit 7: Crystal Select

If this bit is set to logic 0 (24 MHz), the EMI effect will be reduce. If this bit is set to logic 1 (40 MHz), the W78E516D/W78E058D could to use 40MHz crystal, but the EMI effect is major. So we provide the option bit which could be chose by customer.

20 TYPICAL APPLICATION CIRCUITS

External Program Memory and Crystal

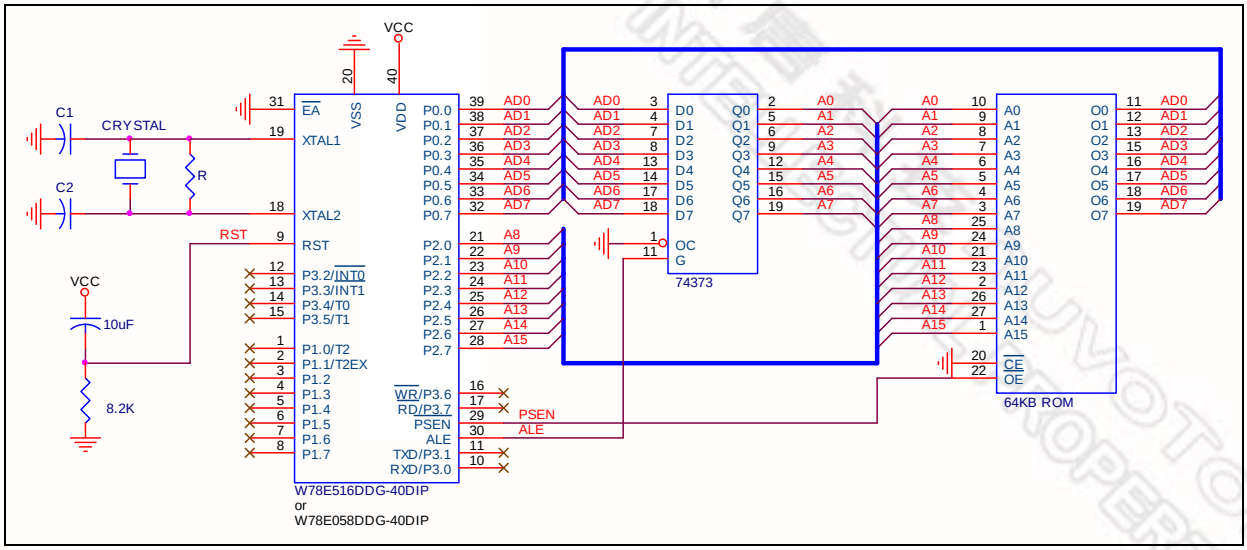


Figure A

Expanded External Data Memory and Oscillator

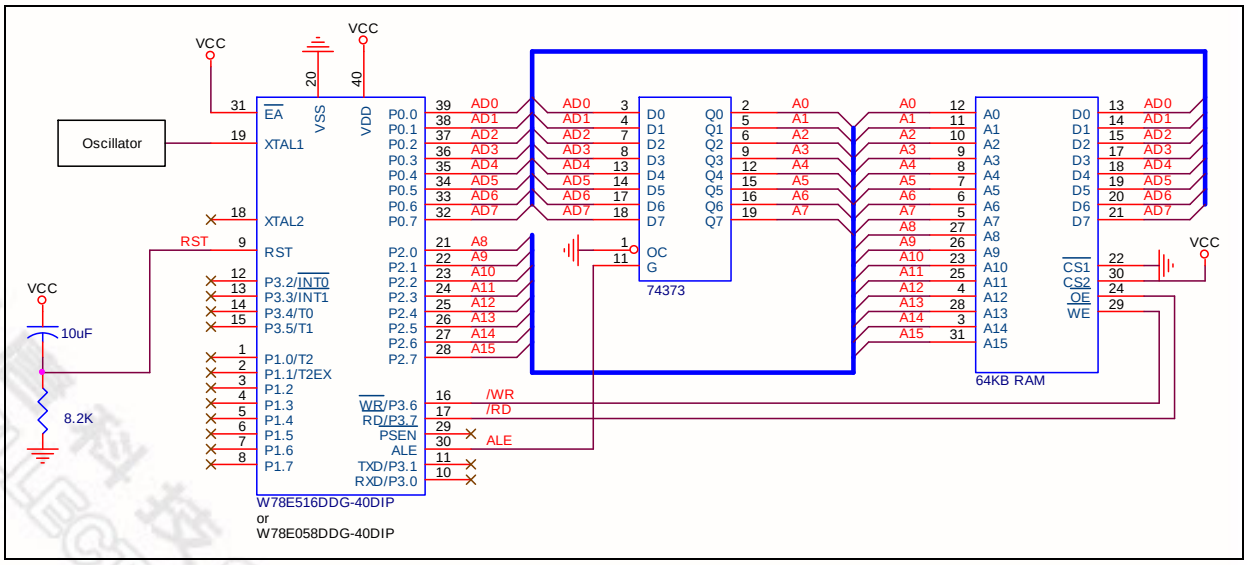


Figure B

21 ELECTRICAL CHARACTERISTICS

21.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	2.4	5.5	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_A	-40	+85	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

21.2 D.C. ELECTRICAL CHARACTERISTICS

T_A=-40℃~+85℃, V_{DD}=2.4V~5.5V, V_{SS}=0V

Sym	Parameter	Test Condition	Min	Typ[*1]	Max	Unit
V_{IL}	Input Low Voltage (Ports 0~4, /EA, XTAL1, RST)	2.4 < V_{DD} < 5.5V	-0.5		0.2V_{DD}-0.1	V
V_{IH}	Input High Voltage (Ports 0~4, /EA)	2.4 < V_{DD} < 5.5V	0.2V_{DD} +0.9		V_{DD}+ 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.4 < V_{DD} < 5.5V	0.7V_{DD}		V_{DD}+ 0.5	V
V_{OL}	Output Low Voltage (Ports 0~4, ALE, /PSEN)	V_{DD}=4.5V, I_{OL}= 12.0mA[*3,*4] V_{DD}=2.4V, I_{OL}= 8.0mA[*3,*4]			0.4	V
V_{OH1}	Output High Voltage (Ports 1~4)	V_{DD}=4.5V, I_{OH}= -300μA[*4] V_{DD}=2.4V, I_{OH}= -20μA[*4]	2.4 2.0			V
V_{OH2}	Output High Voltage (Ports 0 & 2 in external bus mode, ALE, /PSEN)	V_{DD}=4.5V, I_{OH}= -8.0mA[*4] V_{DD}=2.4V, I_{OH}= -2.0mA[*4]	2.4 2.0			V
I_{IL}	Logical 0 Input Current (Ports 1~4)	V_{DD}=5.5V, V_{IN}=0.4V		-45	-50	μA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1~4)	V_{DD}=5.5V, V_{IN}=2.0V[*2]		-510	-650	μA
I_{LI}	Input Leakage Current (Port 0)	0 < V_{IN} < V_{DD}+0.5		±1.0	±10	μA
I_{DD}	Power Supply Current	Active mode[*5] @12MHz, V_{DD}=5.0V @40MHz, V_{DD}=5.0V @12MHz, V_{DD}=3.3V @20MHz, V_{DD}=3.3V		 10.4 18.2 3.6 4.4		mA
		Idle mode @12MHz, V_{DD}=5.0V @40MHz, V_{DD}=5.0V @12MHz, V_{DD}=3.3V @20MHz, V_{DD}=3.3V		 3.4 10.3 1.3 1.9		mA
		Power-down mode		<1	50	μA

R_{RST}	RST-pin Internal Pull-down Resistor	2.4 < V_{DD} < 5.5V	30		350	KΩ

Note:

*1: Typical values are not guaranteed. The values listed are tested at room temperature and based on a limited number of samples.

*2: Pins of ports 1~4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

*3: Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20mA
Maximum I_{OL} per 8-bit port: 40mA
Maximum total I_{OL} for all outputs: 100mA

*4: If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification.
If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

*5: Tested while CPU is kept in reset state and EA=H, Port0=H.

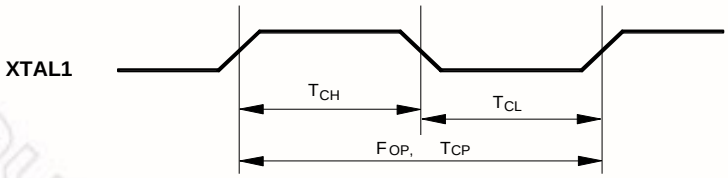
Voltage	**Max.** Frequency	6T/12T mode	Note
4.5-5.5V	40MHz	12T	
4.5-5.5V	20MHz	6T	
2.4V	20MHz	12T	
2.4V	10MHz	6T	

Frequency VS Voltage Table

21.3 AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	4	-	40	MHz	1

Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	TDAR	3 TCP-Δ	-	3 TCP+Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{\text{RD}}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{\text{RD}}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	TDRD	6 TCP-Δ	6 TCP	-	nS	2

Notes:
1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{\text{WR}}$ Low	TDAW	3 TCP-Δ	-	3 TCP+Δ	nS
Data Valid to $\overline{\text{WR}}$ Low	TDAD	1 TCP-Δ	-	-	nS
Data Hold from $\overline{\text{WR}}$ High	TDWD	1 TCP-Δ	-	-	nS
$\overline{\text{WR}}$ Pulse Width	TDWR	6 TCP-Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

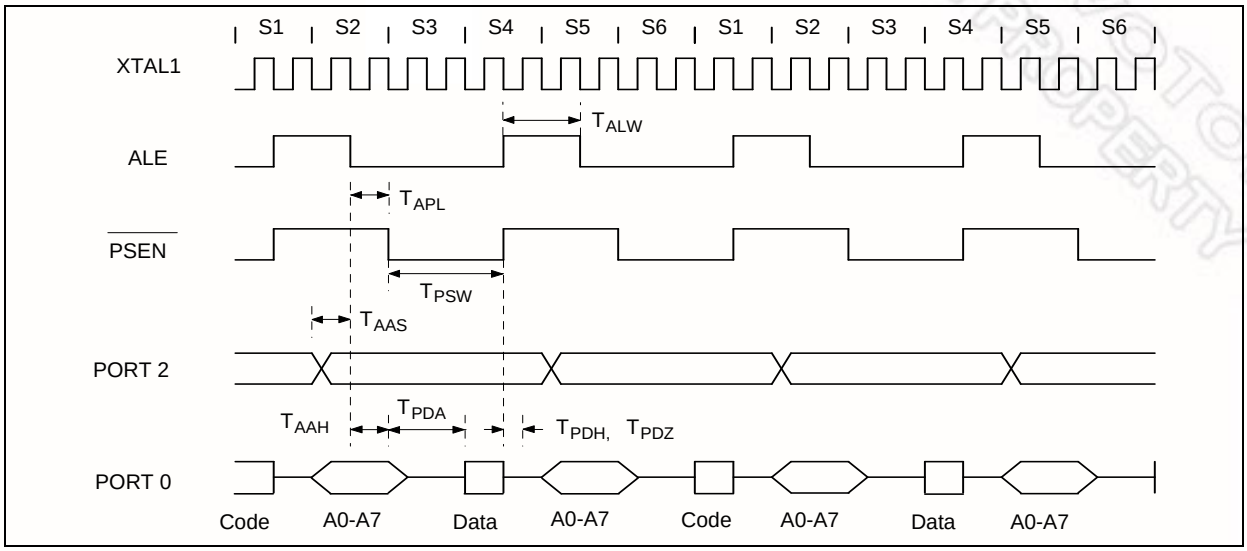
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

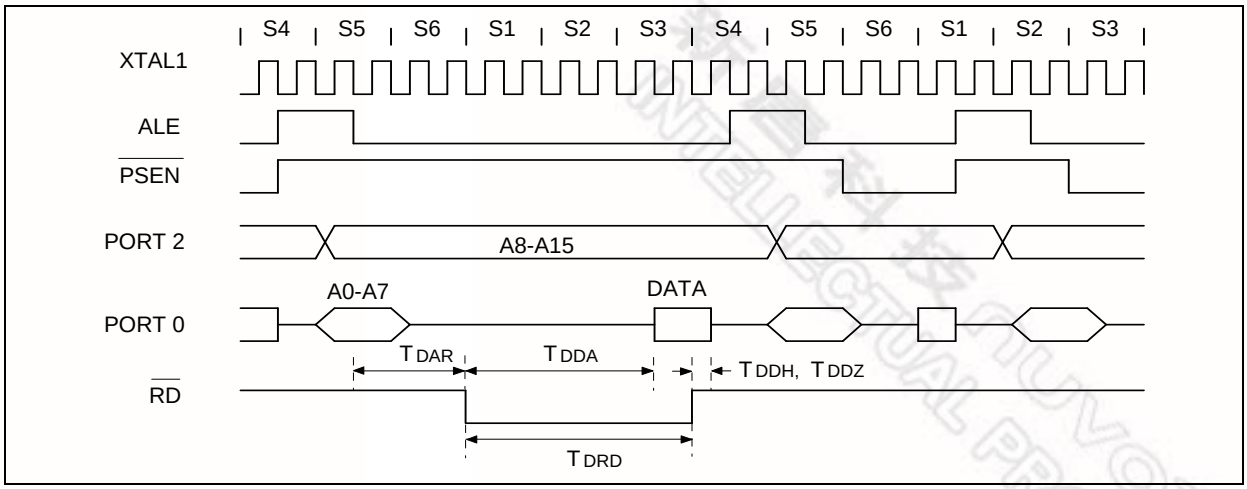
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

21.4 TIMING waveforms

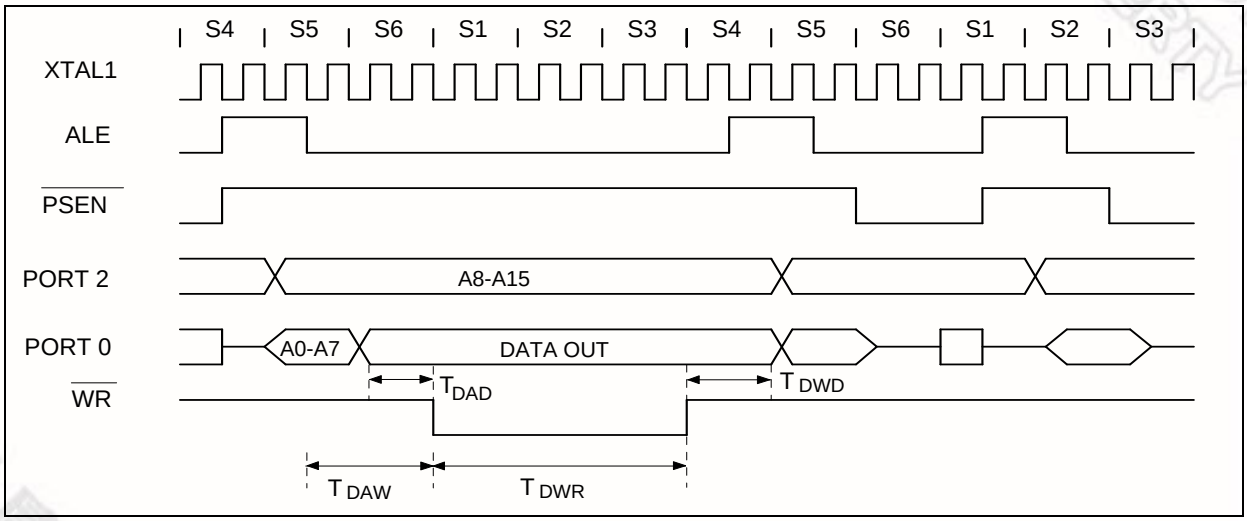
21.4.1 Program Fetch Cycle



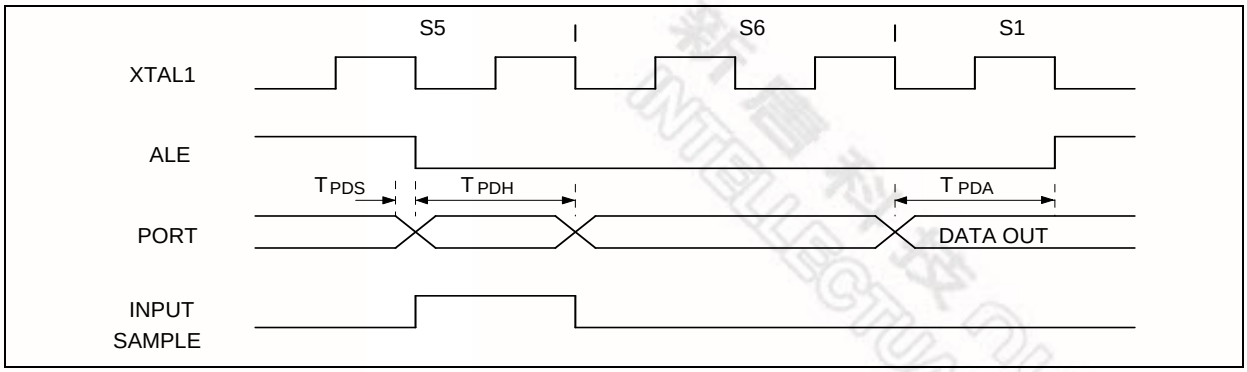
21.4.2 Data Read Cycle



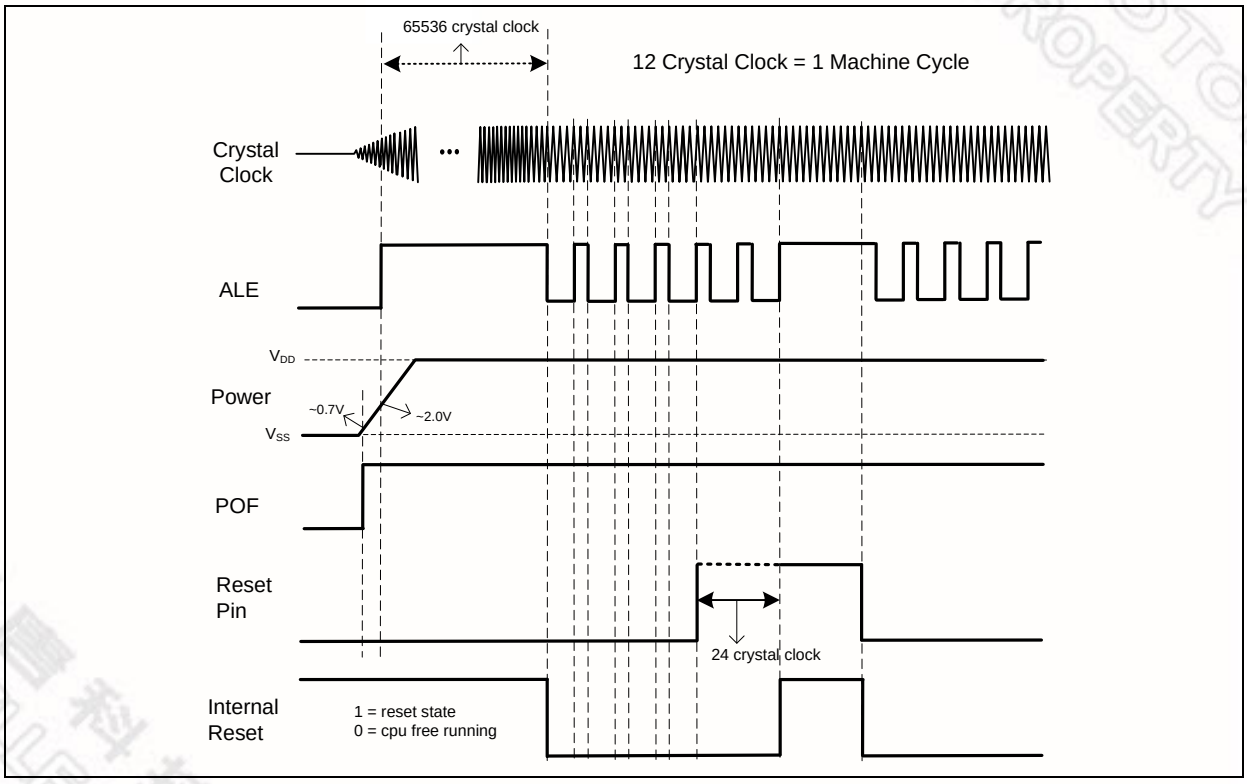
21.4.3 Data Write Cycle



21.4.4 Port Access Cycle

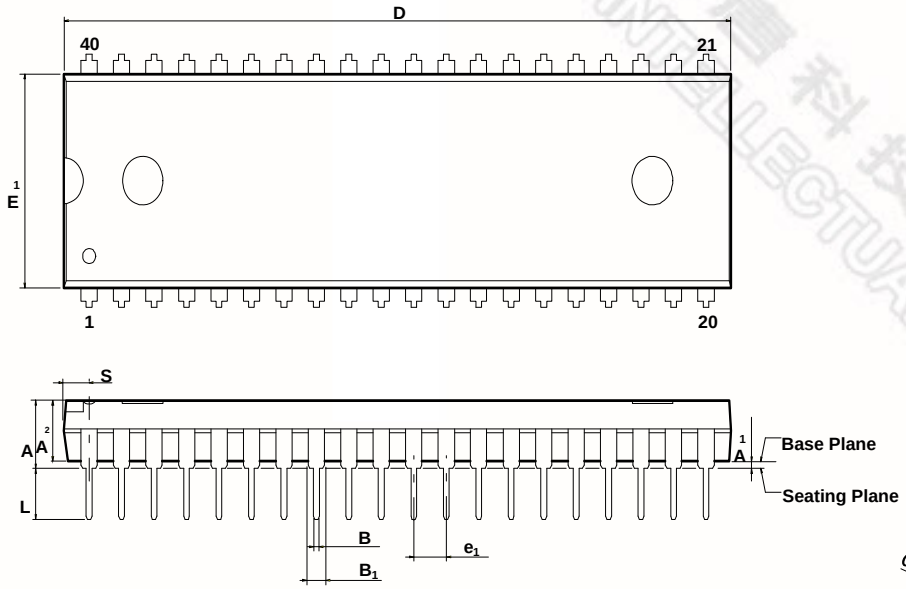


21.4.5 Reset Pin Access Cycle



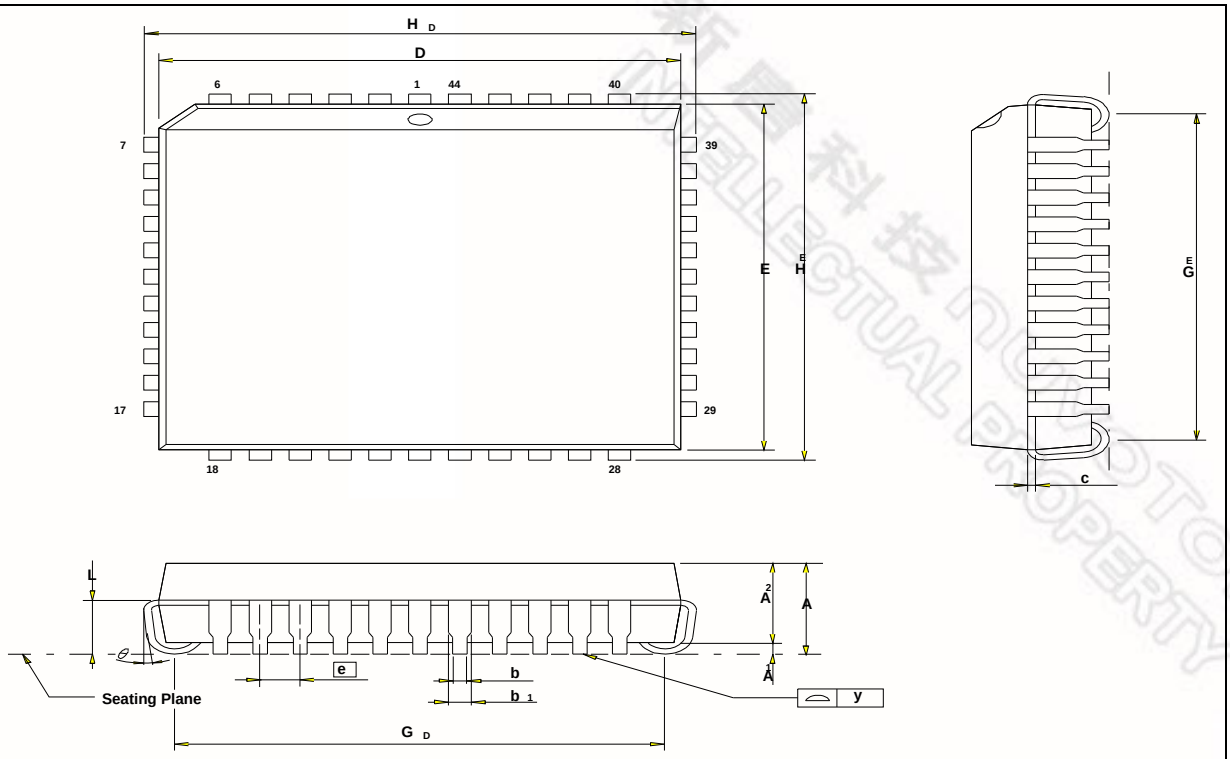
22 PACKAGE DIMENSIONS

22.1 40-pin DIP



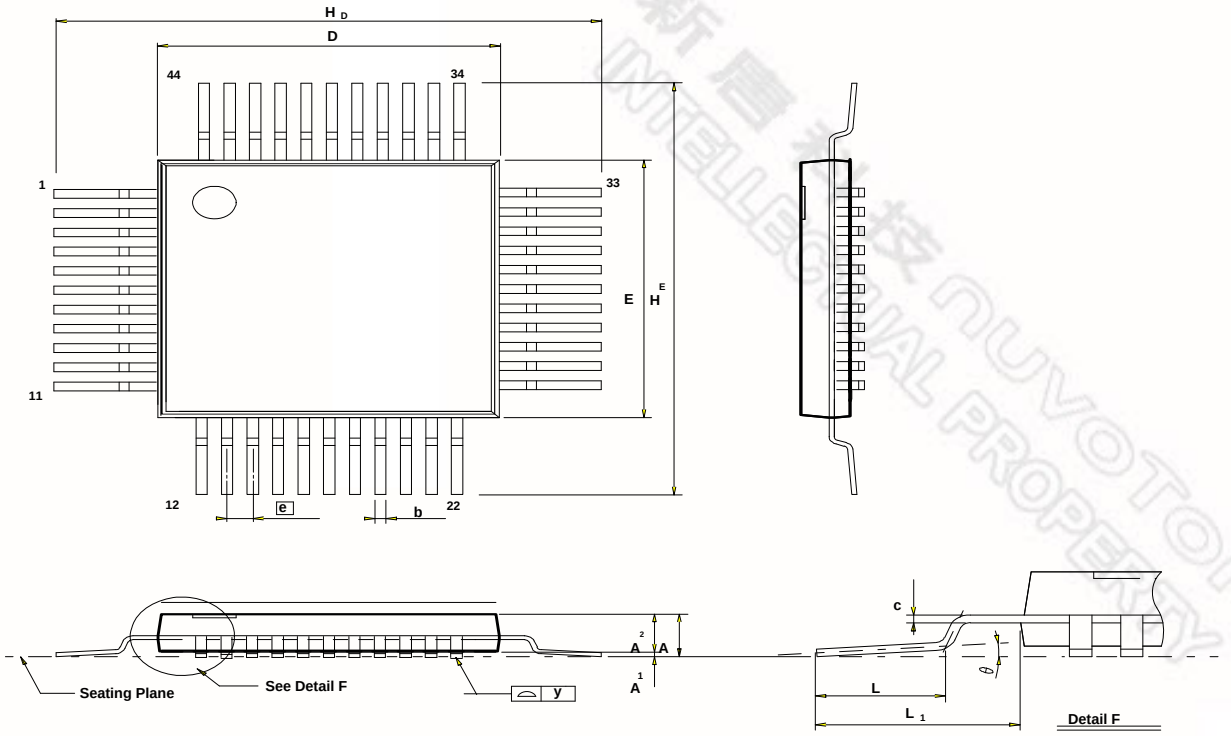
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

22.2 44-pin PLCC



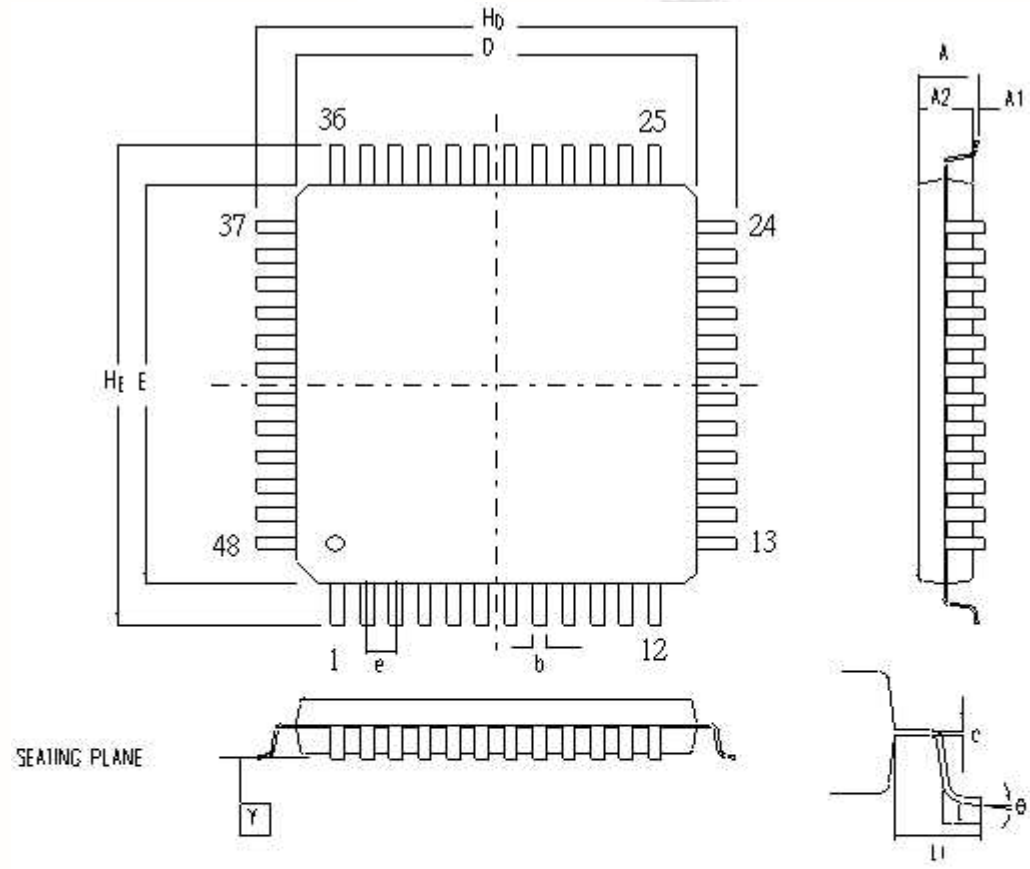
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	——	——	0.185	——	——	4.70
A 1	0.020	——	——	0.51	——	——
A 2	0.145	0.150	0.155	3.68	3.81	3.94
b 1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G D	0.590	0.610	0.630	14.99	15.49	16.00
G E	0.590	0.610	0.630	14.99	15.49	16.00
H D	0.680	0.690	0.700	17.27	17.53	17.78
H E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	——	——	0.004	——	——	0.10

22.3 44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	-	—	—	-
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	—	.0315	—	—	0.80	—
H_D	0.510	0.520	0.530	12.95	13.20	13.45
H_E	0.510	0.520	0.530	12.95	13.20	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	—	0.063	—	—	1.60	—
y	—	—	0.004	—	—	0.10
θ	0 °	—	10 °	0 °	—	10 °

22.4 48-pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

Application Note: In-system Programming Software Examples

This application note illustrates the in-system programmability of the microcontroller. In this example, microcontroller will boot from APROM bank and waiting for a key to enter in-system programming mode for re-programming the contents of APROM. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDROM bank. The loader program erases the APROM then reads the new code data from external SRAM buffer (or through other interfaces) to update the APROM.

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of APROM program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the contents of APROM code else executes the current ROM code.
;* XTAL = 40 MHz
;*****************************************************************************************************************

    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON          EQU         BFH
    CHPENR          EQU         F6H
    SFRAL           EQU         C4H
    SFRAH           EQU         C5H
    SFRFD           EQU         C6H
    SFRCN           EQU         C7H

            ORG         0H
            LJMP        100H                        ;JUMP TO MAIN PROGRAM
  ;*************************************************************************
  ;*  TIMER0 SERVICE VECTOR ORG=000BH
  ;*************************************************************************
            ORG         00BH
            CLR         TR0                         ;TR0=0,STOP TIMER0
            MOV         TL0,R6
            MOV         TH0,R7
            RETI
  ;*************************************************************************
  ;*   APROM MAIN PROGRAM
  ;*************************************************************************
            ORG         100H

MAIN_:

           MOV          A,P1                        ;SCAN P1.0
           ANL          A,#01H
           CJNE         A,#01H,PROGRAM_             ;IF P1.0=0, ENTER IN-SYSTEM
                                                    ;PROGRAMMING MODE
           JMP          NORMAL_MODE

PROGRAM_:
            MOV         CHPENR,#87H                 ; CHPENR=87H, CHPCON
                                                    ; REGISTER WRTE ENABLE
            MOV         CHPENR,#59H                  ; CHPENR=59H, CHPCON
                                                    ; REGISTER WRITE ENABLE
            MOV         CHPCON,#03H                  ;CHPCON=03H, ENTER IN-SYSTEM
                                                    ; PROGRAMMING MODE
```

```
            MOV     TCON,#00H               ;TR=0 TIMER0 STOP
            MOV      IP,#00H                ;IP=00H
            MOV      IE,#82H                ;TIMER0 INTERRUPT ENABLE FOR
                                            ;WAKE-UP FROM IDLE MODE
            MOV     R6,#FEH                 ;TL0=FEH
            MOV     R7,#FFH                 ;TH0=FFH
            MOV     TL0,R6
            MOV     TH0,R7
            MOV     TMOD,#01H               ;TMOD=01H,SET TIMER0 A 16-BIT TIMER
            MOV      TCON,#10H              ;TCON=10H,TR0=1,GO
            MOV      PCON,#01H              ;ENTER IDLE MODE FOR LAUNCHING
                                            ;THE IN-SYSTEM PROGRAMMABILITY
;*****************************************************************************
;* Normal mode APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
                                .
                                    ;User's application program
                                .
                                .
                                .
                                .
```

EXAMPLE 2:

```
;*************************************************************************************************************************  ;*
Example of 4KB LDROM program: This lorder program will erase the APROM first, then reads the new ;* code from external SRAM and program them into APROM bank. XTAL = 40 MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON          EQU         BFH
    CHPENR          EQU         F6H
    SFRAL           EQU         C4H
    SFRAH           EQU         C5H
    SFRFD           EQU         C6H
    SFRCN           EQU         C7H

            ORG     000H
            LJMP    100H                    ;JUMP TO MAIN PROGRAM
  ;*****************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG=0BH
  ;*****************************************************************************
            ORG     000BH
            CLR     TR0                      ;TR0=0,STOP TIMER0
            MOV     TL0,R6
            MOV     TH0,R7
            RETI

  ;*****************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
```

```
;*********************************************************************
            ORG 100H

MAIN_4K:

            MOV         CHPENR,#87H             ;CHPENR=87H, CHPCON WRITE ENABLE.
            MOV         CHPENR,#59H             ;CHPENR=59H, CHPCON WRITE ENABLE.
            MOV         7FH,#01H                ;SET F04KBOOT MODE FLAG.

            MOV         A,CHPCON
            ANL         A,#01H
            CJNE        A,#00H,UPDATE_          ;CHECK CHPCON BIT 0
            MOV         7FH,#00H                ;FLAG=0, NOT IN THE F04KBOOT MODE.

            MOV         CHPCON,#01H             ;CHPCON=01H, ENABLE IN-SYSTEM PROGRAMMING.
            MOV         CHPENR,#00H             ;DISABLE CHPCON WRITE ATTRIBUTE

            MOV         TCON,#00H               ;TCON=00H ,TR=0 TIMER0 STOP
            MOV         TMOD,#01H               ;TMOD=01H ,SET TIMER0 A 16BIT TIMER
            MOV         IP,#00H                 ;IP=00H
            MOV         IE,#82H                 ;IE=82H,TIMER0 INTERRUPT ENABLED
            MOV         R6,#FEH
            MOV         R7,#FFH
            MOV         TL0,R6
            MOV         TH0,R7
            MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
            MOV         PCON,#01H               ;ENTER IDLE MODE


UPDATE_:

            MOV         CHPENR,#00H             ;DISABLE CHPCON WRITE-ATTRIBUTE
            MOV         TCON,#00H               ;TCON=00H ,TR=0 TIM0 STOP
            MOV         IP,#00H                 ;IP=00H
            MOV         IE,#82H                 ;IE=82H,TIMER0 INTERRUPT ENABLED
            MOV         TMOD,#01H               ;TMOD=01H ,MODE1

            MOV         R6,#3CH                 ;SET WAKE-UP TIME FOR ERASE OPERATION,
                                                ;ABOUT 15ms.   DEPENDING ON USER'S
                                                ;SYSTEM CLOCK RATE.
            MOV         R7,#B0H
            MOV         TL0,R6
            MOV         TH0,R7

ERASE_P_4K:
            MOV         SFRCN,#22H              ;SFRCN(C7H)=22H  ERASE
            MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
            MOV         PCON,#01H               ;ENTER IDLE MODE( FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************

            MOV         SFRCN,#0H               ;READ APROM MODE
            MOV         SFRAH,#0H               ;START ADDRESS = 0H
            MOV         SFRAL,#0H
            MOV         R6,#FBH                 ;SET TIMER FOR READ OPERATION, ABOUT 1.5us.
            MOV         R7,#FFH
```

```
                MOV         TL0,R6
                MOV         TH0,R7

BLANK_CHECK_LOOP:

                SETB        TR0                     ;ENABLE TIMER 0
                MOV         PCON,#01H               ;ENTER IDLE MODE
                MOV         A,SFRFD                 ;READ ONE BYTE

                CJNE        A,#FFH,BLANK_CHECK_ERROR
                INC         SFRAL                   ;NEXT ADDRESS
                MOV         A,SFRAL
                JNZ         BLANK_CHECK_LOOP
                INC         SFRAH
                MOV         A,SFRAH
                CJNE        A,#C0H,BLANK_CHECK_LOOP   ;END ADDRESS=BFFFH
               JMP          PROGRAM_ROM

BLANK_CHECK_ERROR:

                MOV         P1,#F0H
                MOV         P3,#F0H
                JMP         $

;*******************************************************************************
;* RE-PROGRAMMING APROM BANK
;*******************************************************************************
PROGRAM_ROM:

                MOV         DPTR,#0H                ;THE ADDRESS OF NEW ROM CODE
                MOV         R2,#00H                 ;TARGET LOW BYTE ADDRESS
                MOV         R1,#00H                 ;TARGET HIGH BYTE ADDRESS
                MOV         DPTR,#0H                ;EXTERNAL SRAM BUFFER ADDRESS
                MOV         SFRAH,R1                ;SFRAH, TARGET  HIGH ADDRESS
                 MOV        SFRCN,#21H              ;SFRCN(C7H)=21  (PROGRAM )
                MOV         R6,#0CH                 ;SET TIMER FOR PROGRAMMING, ABOUT 150us.
                MOV         R7,#FEH
                MOV         TL0,R6
                MOV         TH0,R7
PROG_D_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW BYTE ADDRESS
                MOVX        A,@DPTR                 ;READ DATA FROM EXTERNAL SRAM BUFFER
                MOV         SFRFD,A                 ;SFRFD(C6H)=DATA IN
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H               ;ENTER IDLE MODE( PRORGAMMING)
                INC         DPTR
                INC         R2
                CJNE        R2,#0H,PROG_D_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,PROG_D_
;*******************************************************************************
; * VERIFY APROM BANK
;*******************************************************************************
                MOV         R4,#03H                 ;ERROR COUNTER
                MOV         R6,#FBH                 ;SET TIMER FOR READ VERIFY, ABOUT 1.5us.
                MOV         R7,#FFH
```

```
                MOV         TL0,R6
                MOV         TH0,R7
                MOV         DPTR,#0H                ;The start address of sample code
                MOV         R2,#0H                  ;Target  low byte address
                MOV         R1,#0H                  ;Target  high byte address
                MOV         SFRAH,R1                ;SFRAH, Target high address
                MOV         SFRCN,#00H              ;SFRCN=00 (Read ROM CODE)
READ_VERIFY_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW ADDRESS
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H
                INC         R2
                MOVX        A,@DPTR
                INC         DPTR
                CJNE        A,SFRFD,ERROR_
                CJNE        R2,#0H,READ_VERIFY_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,READ_VERIFY_

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
                MOV         CHPENR,#87H             ;CHPENR=87H
                MOV         CHPENR,#59H             ;CHPENR=59H
                MOV         CHPCON,#83H             ;CHPCON=83H, SOFTWARE RESET.


ERROR_:
                DJNZ        R4,UPDATE_              ;IF ERROR OCCURS, REPEAT 3 TIMES.
        .                                           ;IN-SYSTEM PROGRAMMING FAIL, USER'S
                                                   ;PROCESS TO DEAL WITH IT.
```

23 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	June 24, 2008	-	Initial Issued
A02	August 21,2008	7,8	Update pin assignment.
A03	September 1,2008	-	Update W78I516D/W78I058D parts
A04	November 3,2008		Update DC table typo error
A05	January 7,2009	74	Update V_{IL} and V_{IH} .
A06	April 2, 2009	- - -	Update DC table Revise some typing errors Rename SFR 86H POR register to P0UPR
A07	April 22,2009	70	Revise the Application Circuit
A08	June 30,2009	6 65 70 71	1. Revise the Table 3-1 2. Add the picture for “F04KBOOT Mode” of P4.3 3. Revise the ISP Flow Chart 4. Revise the CONFIG BITS 5. Remove the “Preliminary” character each page
A09	Feb 15,2011	18 65 70 79	1. Revise the default reset value for CHPCON 2. Add the reset-pin reset can entry the F04KBOOT mode. 3. Revise the flow chart of ISP programming 4. Revise the CONFIG BITS 5. Add the external reset pin timing

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.