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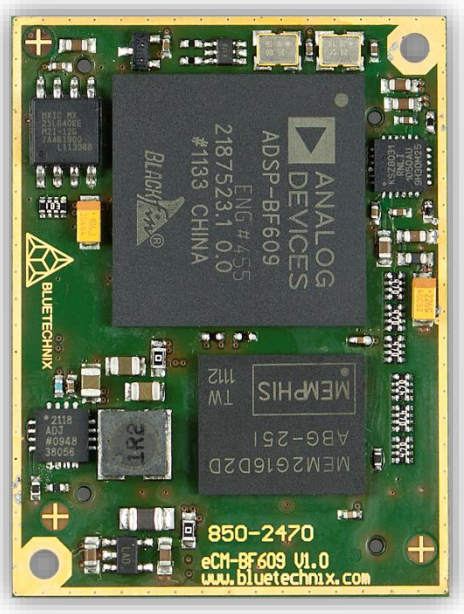
Embedding Ideas

eCM-BF609



Hardware User Manual

Version 1.4

Contact

Bluetechnix Mechatronische Systeme GmbH

Waidhausenstraße 3/19

A-1140 Vienna

AUSTRIA

office@bluetechnix.com

http://www.bluetechnix.com

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Warning

Due to technical requirements components may contain dangerous substances.

1 Introduction

The Core Module eCM-BF609 is optimized for performance and parallel data processing. The module integrates processor, DDR2 RAM, NOR flash, Ethernet PHY and power supply at a size of 44x33mm! It is based on the high performance dual-core ADSP-BF609 from Analog Devices.

The ADSP-BF609 integrates a co-processor unit to process signal and image algorithms (i.e. for pre- and co-processing of video frames in ADAS applications). The eCM-BF609 is designed for industrial and commercial applications. It addresses 256MByte DDR2 SDRAM via its dedicated DDR2 interface and has an onboard SPI flash of 8MByte.

1.1 Overview

Figure 1.1 shows the main components of the Core Module eCM-BF609.

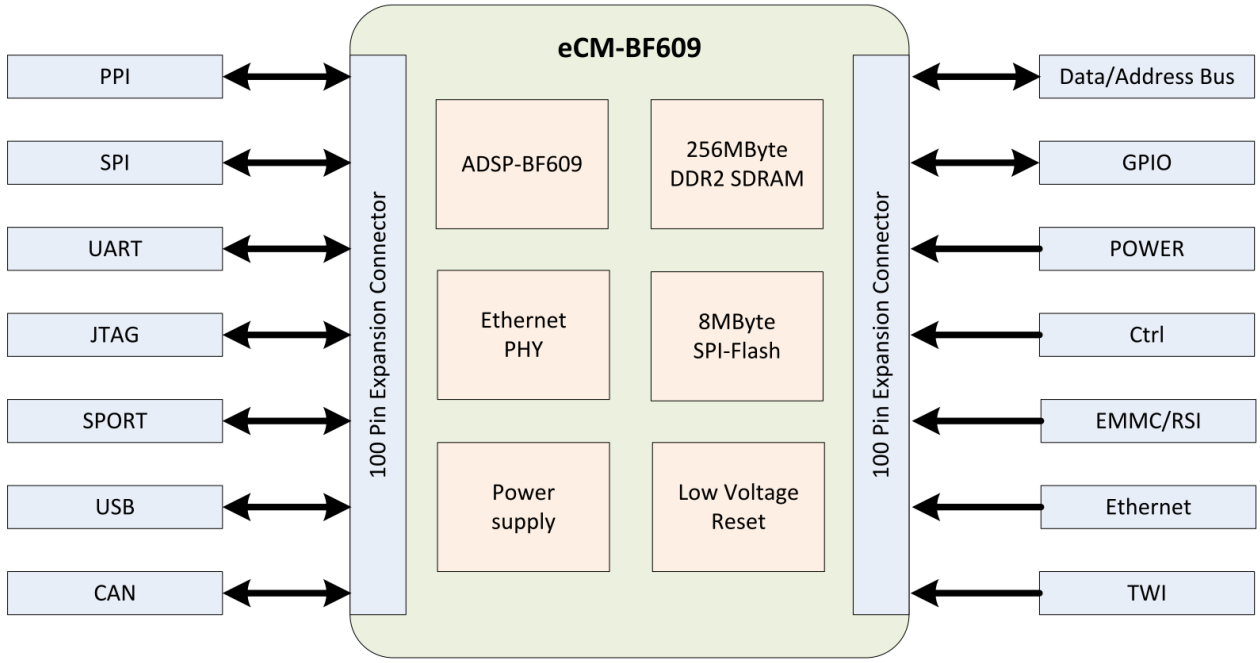


Figure 1.1: Main components of the eCM-BF609 module

1.2 Key Features

- **Analog Devices Blackfin Processor ADSP-BF609**
  - ADSP-BF609BBCZ-5X (Temperature range: - 40°C – 85°C)
- **256MB DDR2 SDRAM**
  - MEM2G16D2DABG-25I
  - DDR2-SDRAM Clock up to 400MHz
  - 128Mx16, 1Gbit at 1.8V

- **8MB SPI-Flash**
  - MX25L6406EM2I-12G
  - 64Mbit at 3.3V
- **Power supply**
  - Core voltage regulator
    - ADP2118ACPZ-R7
    - 1.25V at 2.5A
  - DDR2 SDRAM
    - ADP2108AUJZ-1.8-R7
    - 1.8V at 600mA
- **Low voltage Reset**
  - Module resets if power supply goes below 2.93V for at least 140ms
- **Ethernet PHY**
  - KSZ8031RNLI
  - Integrated terminal resistors
  - Can be disabled by analog switch to preserve the EPPI1 interface (see chapter 2.4)
- **Connectors**
  - 2x UART
  - 1x Up/Down/Rotary Counters
  - 8x Timer/Counters with PWM
  - 2x 3-Phase PWM Units (4-pair)
  - 3x SPORT
  - 2x SPI
  - 1x USB OTG
  - 3x Parallel Peripheral Interface
  - 1x Removable Storage Interface
  - 1x CAN
  - 2x TWI
  - 2x UART
  - 1x ADC Control Module (ACM)
  - 4x Link Ports
  - 1x Ethernet MAC (IEEE 1588)
  - 1x Ethernet MAC+PHY (IEEE 1588)
  - Data/Address Bus
  - GPIOs
  - Boot mode
  - JTAG
  - Power Supply
  - nRESET

- Buffered clocks (25MHz, SYS_CLKOUT)
- Various control signals (see chapter 4)

1.3 Applications

- Parallel digital signal processing
- Automotive vision systems
- Imaging and consumer multimedia
- Stereo vision systems
- Portable media players
- Video conference applications
- Digital video camera systems

2 General Description

2.1 Functional Description

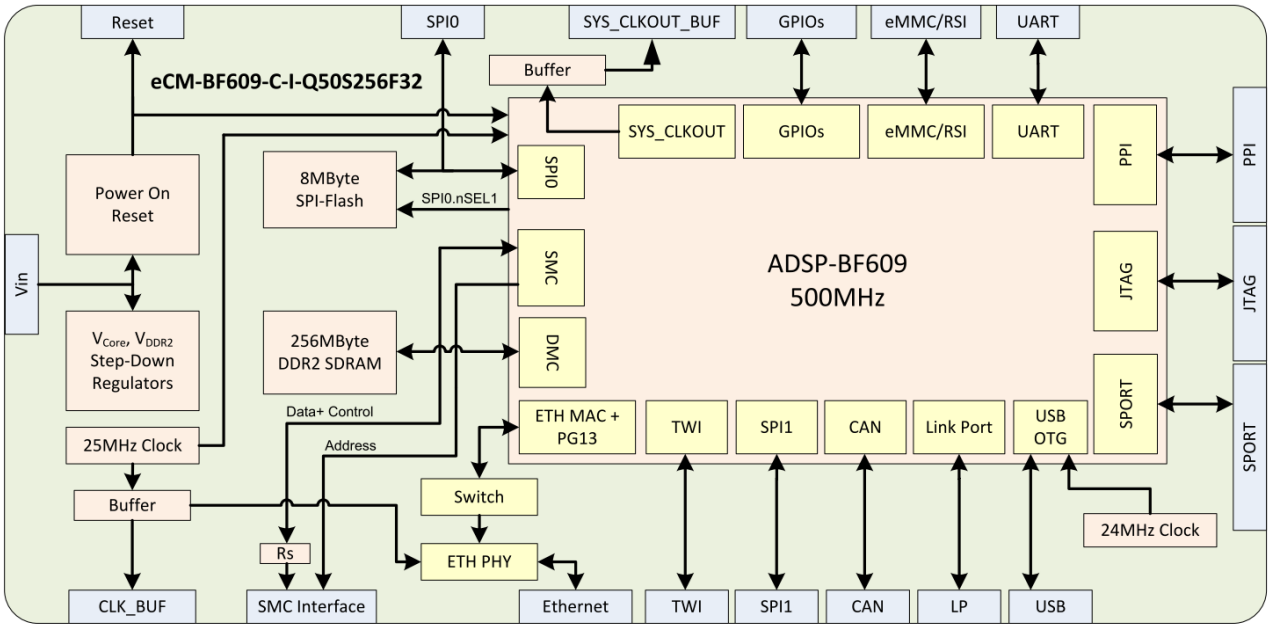


Figure 2.1: Functional overview

2.2 Boot Mode

By default the Boot Mode is set to “No Boot – idle”. The boot mode pins are available on the connectors.

BMODE[2:0]	Boot Source	Description
000	No Boot – idle	The processor does not boot. Rather the boot kernel executes and IDLE instruction.
001	Memory boot	Boot from an address in memory, by default this is the start address of flash memory
010	RSI master boot	Boot through the Removable Storage Interface(RSI) peripheral configure as a slave
011	SPI0 master boot	Boot through the Serial Port Interface (SPI0) peripheral configured as a slave
100	SPI0 slave boot	Boot through the SPI0 peripheral configured as a master
110	LP0 slave boot	Boot through the Link Port (LP0) peripheral configured as a master
111	UART0 slave boot	Boot through the UART0 peripheral configured as a master

Table 2.1: Boot modes

2.2.1 Boot from onboard SPI Flash

The onboard SPI Flash supports double throughput of Serial Flash in read mode (DREAD) therefore the boot time can be shortened using `SPIMCODE = 0x8` (DOR FAST_MODE) at the boot sequence. In this mode the

SPI clock is set to SCLK/2 and the DREAD command is used to read the boot stream from flash. To use this feature the firmware must be linked with the option `-bcode 0x8`.

2.3 Memory Map

2.3.1 Core Module Memory

Memory Type	Access	Size	Comment
SPI FLASH [1)]	SPI0 and SPI0.nSEL1 1-Bit or 2-Bit access	8MByte	MX25L6406EM2I-12G
DDR2 SDRAM	DMC Range: 0x00000000 – 0x0FFFFFFF	256MByte	MEM2G16D2DABG-25I, 128M x 16

Table 2.2: Memory Map

1) The SPI flash is connected to the SPI0 interface. SPI0.nSEL1 is used as chip select signal. See also chapter 2.2.1.

2.3.2 Externally Addressable Memory (on connector)

The Static Memory Controller can be programmed to control up to four banks of memory-mapped devices. Each bank occupies a 64MByte segment regardless of the size of the device used.

AMS Line	Start Address	End Address	Max. Size
nAMS0	0xB0000000	0xB3FFFFFF	64MByte
nAMS1	0xB4000000	0xB7FFFFFF	64MByte
nAMS2	0xB8000000	0xBBFFFFFF	64MByte
nAMS3	0xBC000000	0xBFFFFFFF	64MByte

Table 2.3: External addressable memory

2.4 KSZ5031RNLI Ethernet PHY

The ETH0 interface is connected through an analog switch with the Ethernet PHY KSZ5031RNLI. The connection is controlled by PG_13:

PG_13 Level	Ethernet PHY
LOW	Connected
HIGH	Disconnected

Table 2.4: Connect/Disconnect Ethernet interface

The Ethernet PHY is controlled in RMII mode and the 50MHz reference clock is generated by the PHY itself. No termination resistors are needed for the Ethernet interface since they are integrated in the PHY.

3 Specifications

3.1 Electrical Specifications

3.1.1 Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
V_{IN}	Input supply voltage	3.15	3.3	3.45	V
I_{3V3}	3.3V current	-	1100	-	mA
V_{OH}	High level output voltage	2.4	-	-	V
V_{OL}	Low level output voltage	-	-	0.4	V
I_{IH}	IO input current	-	-	10	µA
I_{OZ}	Three state leakage current	-	-	10	µA
f_{CCLK}	Core clock frequency	-	-	500	MHz

Table 3.1: Electrical characteristics

3.1.2 Maximum Ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions greater than those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{IO}	Input or output voltage	-0.5	3.6	V
V_{IN}	Input supply voltage	-0.5	4.0	V
I_{OH} /I_{OL}	Current per pin	0	10	mA
T_{AMB}	Ambient temperature	-40	85	°C
T_{STO}	Storage temperature	-55	150	°C
T_{SLD}	Solder temperature for 10 seconds		260	°C
φ_{AMB}	Relative ambient humidity (no condensing)		90	%

Table 3.2: Absolute maximum ratings

3.1.3 ESD Sensitivity

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

4 Connector Description

4.1 Connector X1

Pin No.	Signal Name	Type	Function
1	PF_00/PWM0_AL/EPPI0_D00/LP2_D0	I/O	PF Position 0/PWM0 Channel A Low Side/EPPI0 Data 0/LP2 Data 0
2	PF_01/PWM0_AH/EPPI0_D01/LP2_D1	I/O	PF Position 1/PWM0 Channel A High Side/EPPI0 Data 1/LP2 Data 1
3	PF_02/PWM0_BL/EPPI0_D02/LP2_D2	I/O	PF Position 2/PWM0 Channel B Low Side/EPPI0 Data 2/LP2 Data 2
4	PF_03/PWM0_BH/EPPI0_D03/LP2_D3	I/O	PF Position 3/PWM0 Channel B High Side/EPPI0 Data 3/LP2 Data 3
5	PF_04/PWM0_CL/EPPI0_D04/LP2_D4	I/O	PF Position 4/PWM0 Channel C Low Side/EPPI0 Data 4/LP2 Data 4
6	PF_05/PWM0_CH/EPPI0_D05/LP2_D5	I/O	PF Position 5/PWM0 Channel C High Side/EPPI0 Data 5/LP2 Data 5
7	PF_06/PWM0_DL/EPPI0_D06/LP2_D6	I/O	PF Position 6/PWM0 Channel D Low Side/EPPI0 Data 6/LP2 Data 6
8	PF_07/PWM0_DH/EPPI0_D07/LP2_D7	I/O	PF Position 7/PWM0 Channel D High Side/EPPI0 Data 7/LP2 Data 7
9	PE_06/SPORT1_ATDV/EPPI0_FS3/LP3_CLK	I/O	PE Position 6/SPORT1 Channel A Transmit Data Valid/EPPI0 Frame Sync 3 (FIELD)/LP3 Clock
10	PE_07/SPORT1_BTDV/EPPI0_FS2/LP3_ACK	I/O	PE Position 7/SPORT1 Channel B Transmit Data Valid/EPPI0 Frame Sync 2 (VSYNC)/LP3 Acknowledge
11	PE_08/PWM0_SYNC/EPPI0_FS1/LP2_ACK/ ACM0_T0	I/O	PE Position 8/PWM0 Sync/EPPI0 Frame Sync 1 (HSYNC)/LP2 Acknowledge/ACM0 External Trigger 0
12	PE_09/EPPI0_CLK/LP2_CLK/nPWM0_TRIP0	I/O	PE Position 9/EPPI0 Clock/LP2 Clock/PWM0 Shutdown Input 0
13	GND		
14	PC_00/ETH0_RXD0/EPPI1_D00	I/O *)	PC Position 0/ETH0 Receive Data 0/EPPI1 Data 0
15	PC_01/ETH0_RXD1/EPPI1_D01	I/O *)	PC Position 1/ETH0 Receive Data 1/EPPI1 Data 1
16	PC_02/ETH0_TXD0/EPPI1_D02	I/O	PC Position 2/ETH0 Transmit Data 0/EPPI1 Data 2
17	PC_03/ETH0_TXD1/EPPI1_D03	I/O *)	PC Position 3/ETH0 Transmit Data 1/EPPI1 Data 3
18	PC_04/ETH0_RXERR/EPPI1_D04	I/O *)	PC Position 4/ETH0 Receive Error/EPPI1 Data 4
19	PC_05/ETH0_CRS/EPPI1_D05	I/O *)	PC Position 5/ETH0 Carrier Sense/RMII Receive Data Valid/EPPI1 Data 5
20	PC_06/ETH0_MDC/EPPI1_D06	I/O	PC Position 6/ETH0 Management Channel Clock/EPPI1 Data 6
21	PC_07/ETH0_MDIO/EPPI1_D07	I/O *)	PC Position 7/ETH0 Management Channel Serial Data/EPPI1 Data 7
22	PC_08/EPPI1_D08	I/O	PC Position 8/EPPI1 Data 8
23	PC_09/ETH1_PTPPPS/EPPI1_D09	I/O	PC Position 9/ETH1 PTP Pulse-Per-Second Output/EPPI1 Data 9
24	PC_10/EPPI1_D10	I/O	PC Position 10/EPPI1 Data 10
25	PC_11/EPPI1_D11/ETH_PTPAUXIN	I/O	PC Position 11/EPPI1 Data 11/ETH PTP Auxiliary Trigger Input
26	PC_12/nSPI0_SEL7/EPPI1_D1	I/O	PC Position 12/SPI0 Slave Select Output 7/EPPI1

Pin No.	Signal Name	Type	Function
	2		Data 12
27	PC_13/nSPI0_SEL6/EPPI1_D13/ETH_PTPCLKIN	I/O	PC Position 13/SPI0 Slave Select Output 6/EPPI1 Data 13/ETH PTP Clock Input
28	PC_14/nSPI1_SEL7/EPPI1_D14	I/O	PC Position 14/SPI1 Slave Select Output 7/EPPI1 Data 14
29	PC_15/nSPI0_SEL4/EPPI1_D15	I/O	PC Position 15/SPI0 Slave Select Output 4/EPPI1 Data 15
30	PB_15/ETH0_PTPPPS/EPPI1_FS3	I/O	PB Position 15/ETH0 PTP Pulse-Per-Second Output/EPPI1 Frame Sync 3 (FIELD)
31	PD_06/nETH0_PHYINT/EPPI1_FS2/TIMER0_ACI5	I/O *)	PD Position 6/ETH0 RMII Management Data Interrupt/EPPI1 Frame Sync 2 (VSYNC)/TIMER0 Alternate Capture Input 5
32	PB_13/ETH0_TXEN/EPPI1_FS1/TIMER0_ACI6	I/O	PB Position 13/ETH0 Transmit Enable/EPPI1 Frame Sync 1 (HSYNC)/TIMER0 Alternate Capture Input 6
33	PB_14/ETH0_REFCLK/EPPI1_CLK	I/O *)	PB Position 14/ETH0 Reference Clock/EPPI1 Clock
34	3V3	Power	
35	3V3	Power	
36	3V3	Power	
37	GND	Power	
38	GND	Power	
39	GND	Power	
40	nSYS_NMI/nSYS_RESOUT	I/O – 10k pull-up	SYS Non-makeable Interrupt/SYS Reset Output
41	SYS_EXTWAKE	I	SYS External Wake Control
42	PD_08/nUART0_RX/TIMER0_ACI0	I/O	PD Position 8/UART0 Receive/TIMER0 Alternate Capture Input 0
43	PD_07/nUART0_TX/TIMER0_ACI3	I/O	PD Position 7/UART0 Transmit/TIMER0 Alternate Capture Input 3
44	GND	Power	
45	JTG_TCK	I	JTAG Clock
46	JTG_TDO	O	JTAG Data Out
47	JTG_TDI	I	JTAG Data In
48	JTG_TMS	I	JTAG Mode Select
49	nJTG_TRST	I – 4k7 pull-down	JTAG Reset
50	nJTG_EMU	O	JTG Emulation Output
51	PE_10/ETH1_MDC/PWM1_DL/RSI0_D6	I/O	PE Position 10/ETH1 Management Channel Clock/PWM1 Channel D Low Side/RSI0 Data 6
52	PE_11/ETH1_MDIO/PWM1_DH/RSI0_D7	I/O	PE Position 11/ETH1 Management Channel Serial Data/PWM1 Channel D High Side/RSI0 Data 7
53	PD_05/SPI1_CLK/TIMER0_ACLK7	I/O	PD Position 5/SPI1 Clock/TIMER0 Alternate Clock 7
54	PD_13/SPI1_MOSI/TIMER0_ACLK5	I/O	PD Position 13/SPI1 Master Out, Slave In/TIMER0 Alternate Clock 5
55	PD_14/SPI1_MISO/TIMER0_ACLK6	I/O	PD Position 14/SPI1 Master In, Slave Out/TIMER0 Alternate Clock 6
56	PD_12/nSPI1_SEL1/EPPI0_D20/SPORT1_AD1/nSPI1_SS	I/O	PD Position 12/SPI1 Slave Select Output 1/EPPI0 Data 20/SPORT1 Channel A Data 1/SPI1 Slave Select Input
57	PD_15/nSPI1_SEL2/EPPI0_D21/SPORT1_AD0	I/O	PD Position 15/SPI1 Slave Select Output 2/EPPI0 Data 21/SPORT1 Channel A Data 0
58	PE_05/EPPI0_D23/SPORT1_A	I/O	PE Position 5/EPPI0 Data 23/SPORT1 Channel A

Pin No.	Signal Name	Type	Function
	FS		Frame Sync
59	PE_02/SPI1_RDY/EPPI0_D22/ SPORT1_ACLK	I/O	PE Position 2/SPI1 Ready/EPPI0 Data 22/SPORT1 Channel A Clock
60	PE_00/SPI1_D3/EPPI0_D18/SP ORT1_BD1	I/O	PE Position 0/SPI1 Data 3/EPPI0 Data 18/SPORT1 Channel B Data 1
61	PE_01/SPI1_D2/EPPI0_D19/SP ORT1_BD0	I/O	PE Position 1/SPI1 Data 2/EPPI0 Data 19/SPORT1 Channel B Data 0
62	PE_03/EPPI0_D16/ACM0_FS/S PORT1_BFS	I/O	PE Position 3/EPPI0 Data 16/ACM0 Frame Sync/SPORT1 Channel B Frame Sync
63	PE_04/EPPI0_D17/ACM0_CLK/ SPORT1_BCLK	I/O	PE Position 4/EPPI0 Data 17/ACM0 Clock/SPORT1 Channel B Clock
64	GND	Power	
65	CLK_BUF	O	Buffered 25MHz
66	GND	Power	
67	PD_04/SPI0_CLK	I/O	PD Position 4/SPI0 Clock
68	PD_02/SPI0_MISO	I/O – 10k pull-up	PD Position 2/SPI0 Master In, Slave Out
69	PD_03/SPI0_MOSI	I/O	PD Position 3/SPI0 Master Out, Slave In
70	PD_00/SPI0_D2/EPPI1_D16/nS PI0_SEL3	I/O	PD Position 0/SPI0 Data 2/EPPI1 Data 16/SPI0 Slave Select Output 3
71	PD_01/SPI0_D3/EPPI1_D17/nS PI0_SEL2	I/O	PD Position 1/SPI0 Data 3/EPPI1 Data 17/SPI0 Slave Select Output 2
72	PG_08/SPORT2_AD1/TIMER0_ TMR3/nPWM1_TRIP1	I/O	PG Position 8/SPORT2 Channel A Data 1/TIMER0 Timer 3/PWM1 Shutdown Input
73	PG_09/SPORT2_AD0/TIMER0_ TMR4	I/O	PG Position 9/SPORT2 Channel A Data 0/TIMER0 Timer 4
74	PG_01/SPORT2_AFS/TIMER0_ TMR2/CAN0_TX	I/O	PG Position 1/SPORT2 Channel A Frame Sync/TIMER0 Timer 2/CAN0 Transmit
75	PG_04/SPORT2_ACLK/TIMER0 _TMR1/CAN0_RX/TIMER0_ACI 2	I/O	PG Position 4/SPORT2 Channel A Clock/TIMER0 Timer 1/CAN0 Receive/ TIMER0 Alternate Capture Input 2
76	PG_11/SPORT2_BD1/TIMER0_ TMR6/CNT0_UD	I/O	PG Position 11/SPORT2 Channel B Data 1/TIMER0 Timer 6/CNT0 Count Up and Direction
77	PG_12/SPORT2_BD0/TIMER0_ TMR7/CNT0_DG	I/O	PG Position 12/SPORT2 Channel B Data 0/TIMER0 Timer 7/CNT0 Count Down and Gate
78	PG_07/SPORT2_BFS/TIMER0_ TMR5/CNT0_ZM	I/O	PG Position 7/SPORT2 Channel B Frame Sync/ TIMER0 Timer 5/CNT0 Count Zero Marker
79	PG_10/nUART1_RTS/SPORT2 _BCLK	I/O	PG Position 10/UART1 Request to Send/SPORT2 Channel B Clock
80	GND	Power	
81	TWI0_SCL	I/O – Open drain, 5V compatibl e	TWI0 Serial Clock
82	TWI0_SDA	I/O – Open drain, 5V compatibl e	TWI0 Serial Data
83	PG_01/SPORT2_AFS/TIMER0_ TMR2/CAN0_TX	I/O	PG Position 1/SPORT2 Channel A Frame Sync/TIMER0 Timer 2/CAN0 Transmit
84	PG_04/SPORT2_ACLK/TIMER0 _TMR1/CAN0_RX/TIMER0_ACI 2	I/O	PG Position 4/SPORT2 Channel A Clock/TIMER0 Timer 1/CAN0 Receive/ TIMER0 Alternate Capture Input 2
85	TWI1_SDA	I/O –	TWI1 Serial Data

Pin No.	Signal Name	Type	Function
		Open drain, 5V compatible	
86	TWI1_SCL	O – Open drain, 5V compatible	TWI1 Serial Clock
87	PG_06/ETH1_REFCLK/RSI0_CLK/SPORT2_BTDV/nPWM1_TRIP0	I/O	PG Position 6/ETH1 Reference Clock/RSI0 Clock/SPORT2 Channel B Transmit Data Valid/ PWM1 Shutdown Input 0
88	PG_05/ETH1_TXEN/RSI0_CMD/PWM1_SYNC/ACM0_T1	I/O	PG Position 5/ETH1 Transmit Enable/RSI0 Command/PWM1 Sync/ACM0 External Trigger 1
89	PG_03/ETH1_TXD0/PWM1_AH/RSI0_D0	I/O	PG Position 3/ETH1 Transmit Data 0/PWM1 Channel A High Side/RSI0 Data 0
90	PG_02/ETH1_TXD1/PWM1_AL/RSI0_D1	I/O	PG Position 2/ETH1 Transmit Data 1/PWM1 Channel A Low Side/RSI0 Data 1
91	PG_00/ETH1_RXD0/PWM1_BH/RSI0_D2	I/O	PG Position 0/ETH1 Receive Data 0/PWM1 Channel B High Side/RSI0 Data 2
92	PE_15/ETH1_RXD1/PWM1_BL/RSI0_D3	I/O	PE Position 15/PWM1 Channel B Low Side/RSI0 Data 3/ETH1 Receive Data 1
93	PF_15/ACM0_A1/PPI0_D15/LP3_D7	I/O	PF Position 15/ACM0 Address 1/EPPI0 Data 15/LP3 Data 7
94	PF_14/ACM0_A0/PPI0_D14/LP3_D6	I/O	PF Position 14/EPPI0 Data 14/ACM0 Address 0/LP3 Data 6
95	PF_13/ACM0_A3/PPI0_D13/LP3_D5	I/O	PF Position 13/ACM0 Address 3/EPPI0 Data 13/LP3 Data 5
96	PF_12/ACM0_A2/PPI0_D12/LP3_D4	I/O	PF Position 12/ACM0 Address 2/EPPI0 Data 12/LP3 Data 4
97	PF_11/PPI0_D11/LP3_D3	I/O	PF Position 11/EPPI0 Data 11/LP3 Data 3/PWM0 Shutdown Input
98	PF_10/ACM0_A4/PPI0_D10/LP3_D2	I/O	PF Position 10/ACM0 Address 4/EPPI0 Data 10/LP3 Data 2
99	PF_09/nSPI1_SEL6/PPI0_D09/LP3_D1	I/O	PF Position 9/SPI1 Slave Select Output b/EPPI0 Data 9/LP3 Data 1
100	PF_08/nSPI1_SEL5/PPI0_D08/LP3_D0	I/O	PF Position 8/SPI1 Slave Select Output b/EPPI0 Data 8/LP3 Data 0
101	GND	Shield	
102	GND	Shield	
103	GND	Shield	
104	GND	Shield	
105	GND	Shield	
106	GND	Shield	
107	GND	Shield	
108	GND	Shield	
109	GND	Shield	
110	GND	Shield	

Table 4.1: Connector description X1

4.2 Connector X2

Pin No.	Signal Name	Type	Function
101	PB_04/nSMC0_AMS2/SMC0_ABE0/SPORT0_AFS	I/O	PB Position 4/SMC0 Memory Select 2/SMC0 Byte Enable 0/SPORT0 Channel A Frame Sync
102	PB_05/nSMC0_AMS3/SMC0_ABE1/SPORT0_ACLK	I/O	PB Position 5/SMC0 Memory Select 3/SMC0 Byte Enable 1/SPORT0 Channel A Clock
103	nSMC0_AMS0	O – 47R serial	SMC0 Memory Select 0
104	SMC0_A01	O – 47R serial	SMC0 Address 1
105	SMC0_A02	O – 47R serial	SMC0 Address 2
106	PA_00/SMC0_A03/EPPI2_D00/LP0_D0	I/O	PA Position 0/SMC0 Address 3/EPPI2 Data 0/LP0 Data 0
107	PA_01/SMC0_A04/EPPI2_D01/LP0_D1	I/O	PA Position 1/SMC0 Address 4/EPPI2 Data 1/LP0 Data 1
108	PA_02/SMC0_A05/EPPI2_D02/LP0_D2	I/O	PA Position 2/SMC0 Address 5/EPPI2 Data 2/LP0 Data 2
109	PA_03/SMC0_A06/EPPI2_D03/LP0_D3	I/O	PA Position 3/SMC0 Address 6/EPPI2 Data 3/LP0 Data 3
110	PA_04/SMC0_A07/EPPI2_D04/LP0_D4	I/O	PA Position 4/SMC0 Address 7/EPPI2 Data 4/LP0 Data 4
111	PA_05/SMC0_A08/EPPI2_D05/LP0_D5	I/O	PA Position 5/SMC0 Address 8/EPPI2 Data 5/LP0 Data 5
112	PA_06/SMC0_A09/EPPI2_D06/LP0_D6	I/O	PA Position 6/SMC0 Address 9/EPPI2 Data 6/LP0 Data 6
113	PA_07/SMC0_A10/EPPI2_D07/LP0_D7	I/O	PA Position 7/SMC0 Address 10/EPPI2 Data 7/LP0 Data 7
114	PA_08/SMC0_A11/EPPI2_D08/LP1_D0	I/O	PA Position 8/SMC0 Address 11/EPPI2 Data 8/LP1 Data 0
115	GND	Power	
116	3V3	Power	
117	3V3	Power	
118	3V3	Power	
119	GND	Power	
120	GND	Power	
121	GND	Power	
122	SMC0_D00	I/O – 47R serial	SMC0 Data 0
123	SMC0_D01	I/O – 47R serial	SMC0 Data 1
124	SMC0_D02	I/O – 47R serial	SMC0 Data 2
125	SMC0_D03	I/O – 47R serial	SMC0 Data 3
126	SMC0_D04	I/O – 47R serial	SMC0 Data 4
127	SMC0_D05	I/O – 47R serial	SMC0 Data 5
128	SMC0_D06	I/O – 47R serial	SMC0 Data 6
129	SMC0_D07	I/O – 47R serial	SMC0 Data 7
130	SMC0_D08	I/O – 47R serial	SMC0 Data 8
131	SMC0_D09	I/O – 47R	SMC0 Data 9

Pin No.	Signal Name	Type	Function
		serial	
132	SMC0_D10	I/O – 47R serial	SMC0 Data 10
133	SMC0_D11	I/O – 47R serial	SMC0 Data 11
134	SMC0_D12	I/O – 47R serial	SMC0 Data 12
135	SMC0_D13	I/O – 47R serial	SMC0 Data 13
136	SMC0_D14	I/O – 47R serial	SMC0 Data 14
137	SMC0_D15	I/O – 47R serial	SMC0 Data 15
138	nSYS_FAULT	O – 10k pull-up	SYS Fault Output
139	nSYS_HWRST	I/O – 470R pull-up	SYS Processor Reset Control
140	nSMC0_BR	I – 10k pull-up + 47R serial	SMC0 Bus Request
141	PB_01/nSMC0_AMS1/EPPI2_FS1/LP0_ACK	I/O	PB Position 1/SMC0 Memory Select 1/EPPI2 Frame Sync 1 (HSYNC)/LP0 Acknowledge
142	PB_04/nSMC0_AMS2/SMC0_ABE0/SPORT0_AFS	I/O	PB Position 4/SMC0 Memory Select 2/SMC0 Byte Enable 0/SPORT0 Channel A Frame Sync
143	PB_05/nSMC0_AMS3/SMC0_ABE1/SPORT0_ACLK	I/O	PB Position 5/SMC0 Memory Select 3/SMC0 Byte Enable 1/SPORT0 Channel A Clock
144	nSMC0_AOE/SMC0_NORDV	O – 47R serial	SMC0 Output Enable/SMC0 NOR Data Valid
145	nSMC0_ARE	O – 47R serial	SMC0 Read Enable
146	nSMC0_AWE	O – 47R serial	SMC0 Write Enable
147	SMC0_ARDY/SMC0_NORWT	I – 10k pull-up + 47R serial	SMC0 Asynchronous Ready/SMC0 NOR Wait
148	GND	Power	
149	SYS_CLKOUT_BUF	O	Buffered SYS Processor Clock Output
150	GND	Power	
151	nc		
152	Nc		
153	SYS_BMODE0	I – 10k pull-down	SYS Boot Mode Control 0
154	SYS_BMODE1	I – 10k pull-down	SYS Boot Mode Control 1
155	SYS_BMODE2	I – 10k pull-down	SYS Boot Mode Control 2
156	nc		
157	nc		
158	nc		
159	nc		
160	GND	Power	
161	nc		
162	PE_13/ETH1_CRS/PWM1_CH/RSI0_D4	I/O	PE Position 13/ETH1 Carrier Sense/RMII Receive Data Valid/ PWM1 Channel C High Side/RSI0 Data 4
163	PG_14/nUART1_RX/SYS_ID	I/O	PG Position 14/UART1 Receive/SYS Core 1 Idle

Pin No.	Signal Name	Type	Function
	LE1/TIMER0_ACI1		Indicator/TIMER0 Alternate Capture Input 1
164	PG_15/nUART1_TX/SYS_IDLE0/SYS_SLEEP/TIMER0_ACI4	I/O	PG Position 15/UART1 Transmit/SYS Core 0 Idle Indicator/SYS Processor Sleep Indicator/TIMER0 Alternate Capture Input 4
165	PD_09/nSPI0_SEL5/nUART0_RTS/nSPI1_SEL4	I/O	PD Position 9/SPI0 Slave Select Output 5/UART0 Request to Send/SPI1 Slave Select Output 4
166	PE_14/ETH1_RXERR/SPORT2_ATDV/TIMER0_TMR0	I/O	PE Position 14/ETH1 Receive Error/SPORT2 Channel A Transmit Data Valid/ TIMER0 Timer 0
167	PD_10/SPI0_RDY/nUART0_CTS/nSPI1_SEL3	I/O	PD Position 10/SPI0 Ready/UART0 Clear to Send/SPI1 Slave Select Output 3
168	PE_12/nETH1_PHYINT/PWM1_CL/RSI0_D5	I/O	PE Position 12/ETH1 RMII Management Data Interrupt/ PWM1 Channel C Low Side/RSI0 Data 5
169	USB0_VBC	O	USB0 VBUS Control
170	USB0_VBUS	I	USB0 Bus Voltage
171	USB0_ID	I	USB0 OTG ID
172	USB0_DP	I/O	USB0 Data +
173	USB0_DM	I/O	USB0 Data –
174	ETH_TX+	I/O – 49R9 pull-up	Ethernet
175	ETH_TX-	I/O – 49R9 pull-up	Ethernet
176	nc		
177	ETH_RX+	I/O – 49R9 pull-up	Ethernet
178	ETH_RX-	I/O – 49R9 pull-up	Ethernet
179	nc		
180	ETH_LED0	O	Ethernet
181	nc		
182	PB_01/nSMC0_AMS1/EPPI2_FS1/LP0_ACK	I/O	PB Position 1/SMC0 Memory Select 1/EPPI2 Frame Sync 1 (HSYNC)/LP0 Acknowledge
183	PB_00/SMC0_NORCLK/EPPI2_CLK/LP0_CLK	I/O	PB Position 0/SMC0 NOR Clock/EPPI2 Clock/LP0 Clock
184	PB_09/nSMC0_BGH/SPORT0_AD0/TIMER0_ACLK2	I/O	PB Position 9/SMC0 Bus Grant Hang/SPORT0 Channel A Data 0/TIMER0 Alternate Clock 2
185	PB_12/nSMC0_BG/SPORT0_BTDV/SPORT0_AD1/TIMER0_ACLK1	I/O	PB Position 12/SMC0 Bus Grant/SPORT0 Channel B Transmit Data Valid/ SPORT0 Channel A Data 1/TIMER0 Alternate Clock 1
186	nc		
187	PB_11/SMC0_A25/SPORT0_BD0/TIMER0_ACLK3	I/O	PB Position 11/SMC0 Address 25/SPORT0 Channel B Data 0/TIMER0 Alternate Clock 3
188	PB_10/SMC0_A24/SPORT0_BD1/TIMER0_ACLK0	I/O	PB Position 10/SMC0 Address 24/SPORT0 Channel B Data 1/TIMER0 Alternate Clock 0
189	PB_08/SMC0_A23/EPPI2_D17/SPORT0_BCLK	I/O	PB Position 8/SMC0 Address 23/EPPI2 Data 17/SPORT0 Channel B Clock
190	PB_07/SMC0_A22/EPPI2_D16/SPORT0_BFS	I/O	PB Position 7/SMC0 Address 22/EPPI2 Data 16/SPORT0 Channel B Frame Sync
191	PB_06/SMC0_A21/SPORT0_ATDV/TIMER0_ACLK4	I/O	PB Position 6/SMC0 Address 21/SPORT0 Channel A Transmit Data Valid/TIMER0 Alternate Clock 4

Pin No.	Signal Name	Type	Function
192	PA_15/SMC0_A20/EPPI2_D15/LP1_D7	I/O	PA Position 15/SMC0 Address 20/EPPI2 Data 15/LP1 Data 7
193	PA_14/SMC0_A19/EPPI2_D14/LP1_D6	I/O	PA Position 14/SMC0 Address 19/EPPI2 Data 14/LP1 Data 6
194	PA_13/SMC0_A18/EPPI2_D13/LP1_D5	I/O	PA Position 13/SMC0 Address 18/EPPI2 Data 13/LP1 Data 5
195	PA_12/SMC0_A17/EPPI2_D12/LP1_D4	I/O	PA Position 12/SMC0 Address 17/EPPI2 Data 12/LP1 Data 4
196	PB_03/SMC0_A16/EPPI2_FS3/LP1_CLK	I/O	PB Position 3/SMC0 Address 16/EPPI2 Frame Sync 3 (FIELD)/LP1 Clock
197	PA_11/SMC0_A15/EPPI2_D11/LP1_D3	I/O	PA Position 11/SMC0 Address 15/EPPI2 Data 11/LP1 Data 3
198	PA_10/SMC0_A14/EPPI2_D10/LP1_D2	I/O	PA Position 10/SMC0 Address 14/EPPI2 Data 10/LP1 Data 2
199	PB_02/SMC0_A13/EPPI2_FS2/LP1_ACK	I/O	PB Position 2/SMC0 Address 13/EPPI2 Frame Sync 2 (VSYNC)/ LP1 Acknowledge
200	PA_09/SMC0_A12/EPPI2_D09/LP1_D1	I/O	PA Position 9/SMC0 Address 12/EPPI2 Data 9/LP1 Data 1
201	GND	Shield	
202	GND	Shield	
203	GND	Shield	
204	GND	Shield	
205	GND	Shield	
206	GND	Shield	
207	GND	Shield	
208	GND	Shield	
209	GND	Shield	
210	GND	Shield	

Table 4.2: Connector description X2

*) Only available if Ethernet PHY is disconnected (see chapter 2.4)

5 Application Information

5.1 Supply Voltage Decoupling

Following table shows the pins that should be decoupled by capacitors.

Pin No.	Signal Name	Capacitor value
34	3V3	47µF Tantal
34	3V3	100nF
35	3V3	100nF
36	3V3	100nF
116	3V3	100nF
117	3V3	100nF
118	3V3	100nF
170	USB0_VBUS	100nF

Table 5.1: Recommended decoupling capacitors

5.2 Reset circuit

The integrated reset circuit monitors the 3.3V power rail. If this voltage drops below 2.93V, the $\overline{\text{SYS\_HWRST}}$ signal will be asserted. If the 3.3V voltage domain rises above this threshold, $\overline{\text{SYS\_HWRST}}$ will be kept low for 140 to 280ms and will be released afterwards.

The $\overline{\text{SYS\_HWRST}}$ signal is an open collector output with an internal pull-up resistor of 470R. This signal can be used as external manual reset by connecting an external push-button that ties the signal to ground.

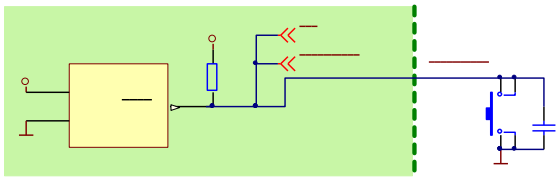


Figure 5.1: Internal reset circuit

If $\overline{\text{SYS\_HWRST}}$ is used to reset other devices then it is recommended to use a tri-state buffer to unload the internal reset circuit.

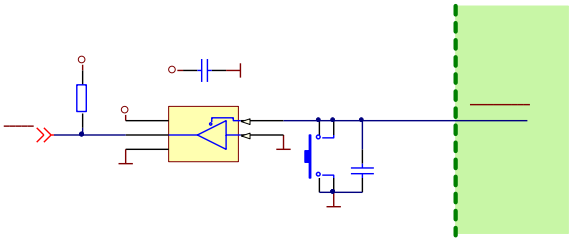


Figure 5.2: Advanced reset circuit

6 Mechanical Outline

All dimensions are given in millimeters. Outline dimensions +/- 0,5mm.

6.1 Top View

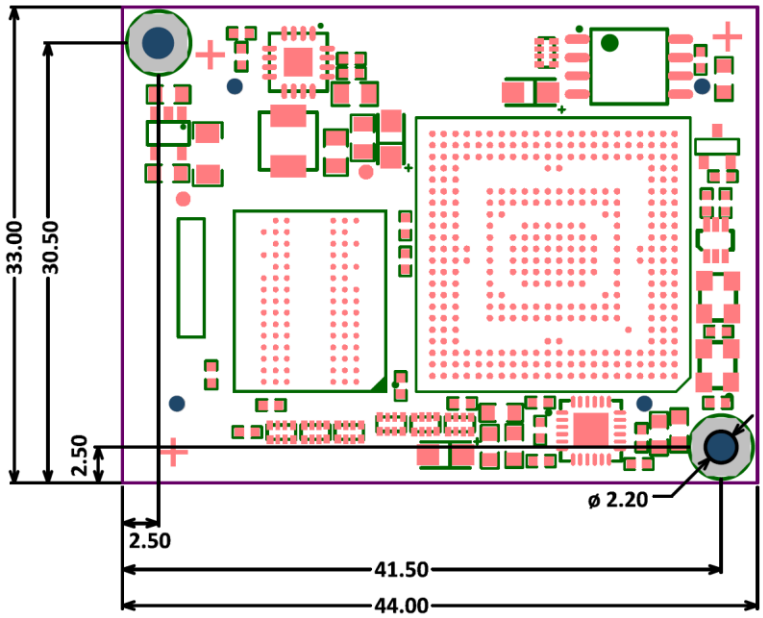


Figure 6.1: Mechanical outline (top view)

6.2 Bottom View

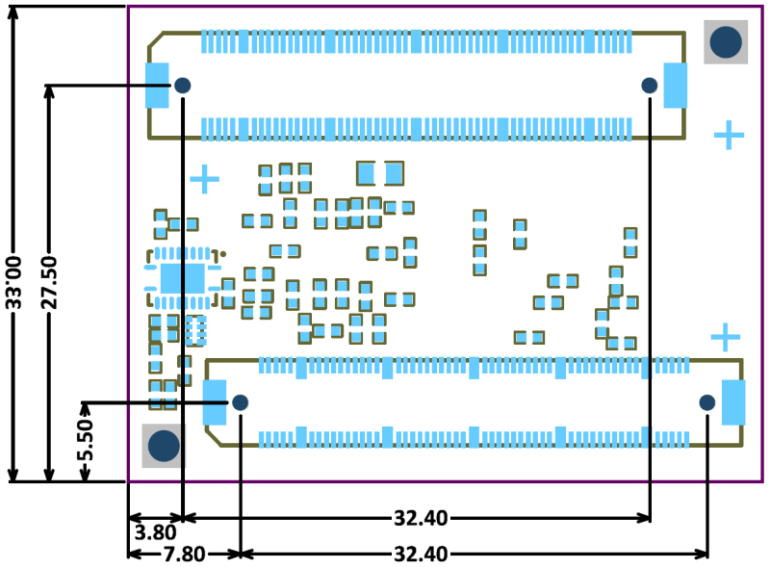


Figure 6.2: Mechanical outline and Bottom Connectors (bottom view)

6.3 Side View

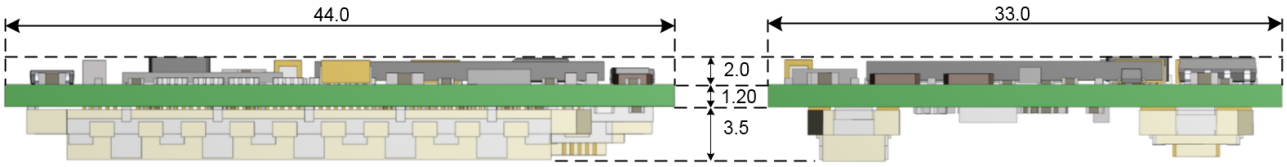


Figure 6.3: Mechanical outline (side view)

6.4 Footprint

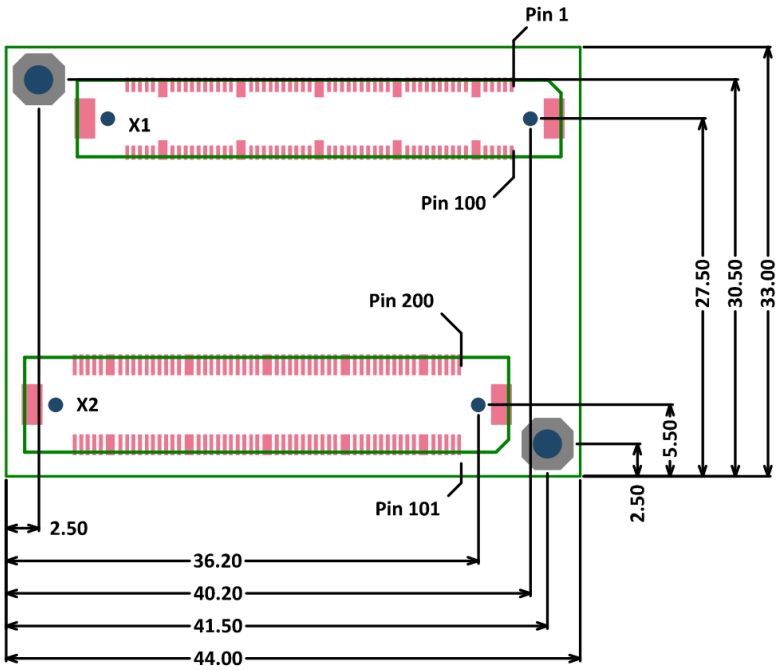


Figure 6.4: Footprint (top view)

The footprint for Altium Designer is available on request.

The used connectors can be found in Table 6.1. For detailed dimensions of the connectors please see the datasheet from the manufacturer's homepage.

6.5 Connectors

Connector Core Module	Matching Connector	Manufacturer	Manufacturer Part No.
X1	X2	Hirose	FX-10A-100S/10SV
X2	X1	Hirose	FX-10A-100P/10SV

Table 6.1: Core Module connector types

The Core Module features 2 connectors, one male and one female. The base board uses the same connectors but oriented in the opposite way.

7 Support

7.1 General Support

General support for products can be found at Bluetechnix' support site https://support.bluetechnix.at/wiki

7.2 Board Support Packages

Board support packages and software downloads are for registered customers only
https://support.bluetechnix.at/software/

7.3 Blackfin® Software Support

7.3.1 BLACKSheep® OS

BLACKSheep® OS stands for a powerfully and multithreaded real-time operating system (RTOS) originally designed for digital signal processing application development on Analog Devices Blackfin® embedded processors. This high-performance OS is based on the reliable and stable real-time VDK kernel from Analog Devices that comes with VDSP++ IDE. Of course BLACKSheep® OS is fully supported by all Bluetechnix Core-Modules and development hardware.

7.3.2 LabVIEW

You can get LabVIEW embedded support for Bluetechnix Core Modules by Schmid-Engineering AG http://www.schmid-engineering.ch.

7.3.3 uClinux

You can get uClinux support (boot loader and uClinux) for Bluetechnix Core Modules at http://blackfin.uClinux.org.

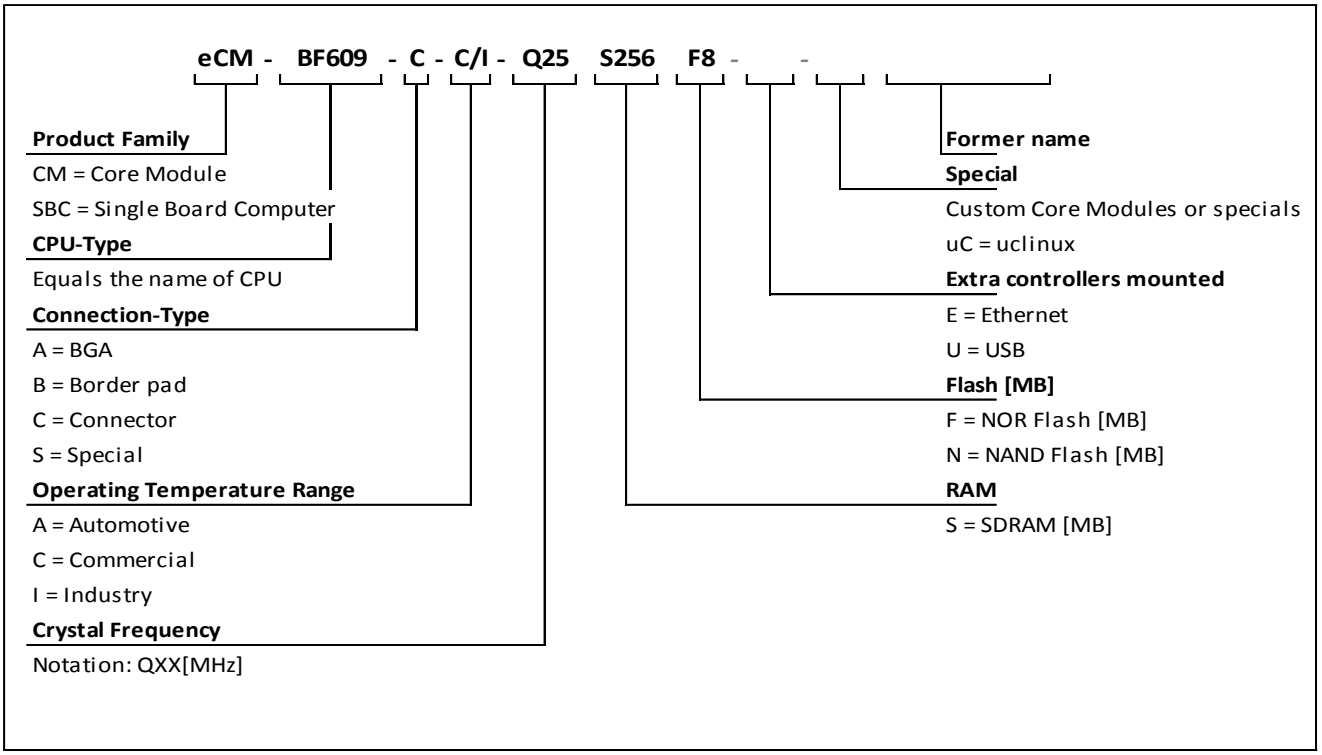
7.4 Blackfin® Design Services

Based on more than seven years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

7.4.1 Upcoming Products and Software Releases

Keep up to date with all product changes, releases and software updates of Bluetechnix at http://www.bluetechnix.com.

8 Ordering Information



8.1 Predefined mounting options for eCM-BF609

Article Number	Name	Temperature Range
100-1217-1	eCM-BF609-C-C-Q25S256F8 (eCM-BF561)	Commercial
100-1218-1	eCM-BF609-C-I-Q25S256F8 (eCM-BF561)	Industrial

Table 8.1: Ordering information

8.2 Development Boards & Kits

Article Number	Name	Type
100-3401-1	Blackfin Evaluation Starter Package with eCM-BF609 including eDEV-BF6xx	Development Kit with Core Module and carrier board

Table 8.2: Ordering information

NOTE: Custom Core Modules are available on request! Please contact Bluetechnix (office@bluetechnix.com) if you are interested in custom Core Modules.

9 Dependability

9.1 MTBF

Please keep in mind that a part stress analysis would be the only way to obtain significant failure rate results, because MTBF numbers just represent a statistical approximation of how long a set of devices should last before failure. Nevertheless, we can calculate an MTBF of the Core Module using the bill of material. We take all the components into account. The PCB and solder connections are excluded from this estimation. For test conditions we assume an ambient temperature of 30°C of all Core Module components except the Blackfin® processor (80°C) and the memories (70°C). We use the MTBF Calculator from ALD (http://www.aldservice.com/) and use the reliability prediction MIL-217F2 Part Stress standard. Please get in touch with Bluetechnix (office@bluetechnix.com) if you are interested in the MTBF result.

10 Product History

10.1 Version Information

10.1.1 eCM-BF609-C-I-Q25S256F8

Version	Component	Type
1.0.0	Processor	ADSP-BF609-ENG
	RAM	MEM2G16D2DABG-25I
	Flash	MX25L6406EM2I-12G (8MB)
	ETH-PHY	KSZ8031RNLI
1.1.0	Processor	ADSP-BF609BBCZ-5X
	RAM	MEM2G16D2DABG-25I
	Flash	MX25L6406EM2I-12G (8MB)
	ETH-PHY	KSZ8031RNLI

Table 10.1: Overview eCM-BF609 Industrial product changes

10.1.2 eCM-BF609-C-C-Q25S256F8

Version	Component	Type
1.0.0	Processor	ADSP-BF609-ENG
	RAM	MEM2G16D2DABG-25I
	Flash	MX25L6406EM2I-12G (8MB)
1.1.0	Processor	ADSP-BF609BBCZ-5X
	RAM	MEM2G16D2DABG-25I
	Flash	MX25L6406EM2I-12G (8MB)
	ETH-PHY	KSZ8031RNLI

Table 10.2: Overview eCM-BF609 product changes

10.2 Anomalies

Version	Date	Description
V1.0	2012 04 26	The TWI0 signals must be swapped to be compatible with BLT products.
V1.1	2013 05 13	No anomalies reported.

Table 10.3 – Product anomalies

11 Document Revision History

Version	Date	Document Revision
1	2012 04 26	Preliminary release V1.0 of the document
2	2013 03 11	Updated connector X1 description
3	2013 05 13	Update table 2.3.1 Core Module Memory Update table 3.1.1 Operating Conditions Update view 6.3 Side View to eCM-BF609 V1.1 Update chapter 10 to eCM-BF609 V1.1 Update chapter 6 to eCM-BF609 V1.1 Add chapter 2.2.1
4	2013 05 17	Update table 15 (BMODE0 and BMODE2 swapped)

Table 11.1: Revision history

12 List of Abbreviations

Abbreviation	Description
ADI	Analog Devices Inc.
AI	Analog Input
AMS	Asynchronous Memory Select
AO	Analog Output
CM	Core Module
DC	Direct Current
DSP	Digital Signal Processor
eCM	Enhanced Core Module
EBI	External Bus Interface
ESD	Electrostatic Discharge
GPIO	General Purpose Input Output
I	Input
I²C	Inter-Integrated Circuit
I/O	Input/Output
ISM	Image Sensor Module
LDO	Low Drop-Out regulator
MTBF	Mean Time Between Failure
NC	Not Connected
NFC	NAND Flash Controller
O	Output
OS	Operating System
PPI	Parallel Peripheral Interface
PWR	Power
RTOS	Real-Time Operating System
SADA	Stand Alone Debug Agent
SD	Secure Digital
SoC	System on Chip
SPI	Serial Peripheral Interface
SPM	Speech Processing Module
SPORT	Serial Port
TFT	Thin-Film Transistor
TISM	Tiny Image Sensor Module
TSC	Touch Screen Controller
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
USBOTG	USB On The Go
ZIF	Zero Insertion Force

Table 12.1: List of abbreviations

A List of Figures and Tables

Figures

Tables