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FAIRCHILD SEMICONDUCTOR®

October 2009

FAN6103
Power Supply Supervisor Plus PWM

Features

- PC Half-Bridge Power Supply Supervisor Plus PWM
- High Integration, Few External Components
- Over-Voltage Protection for 3.3V, 5V, and 12V
- Under-Voltage Protection for 3.3V, 5V, and 12V
- Under-Voltage protection for –12V and/or –5V
- Over-Power and Short-Circuit Protection
- Power-Down Warning Circuitry
- Power-Good Circuitry
- Delay Time for PSON and PG Signal
- Remote ON/OFF Function
- On-Chip Oscillator and Error Amplifier
- Latching PWM for Cycle-By-Cycle Switching
- Push-Pull PWM Operation and Totem-Pole Outputs
- Soft-Start and Maximum 93% Duty Cycle

Applications

- Desktop PC Power Supply

Description

FAN6103 controller is designed for switching mode power supply for desktop PCs. It provides all the functions necessary to monitor and control the output of the power supply. Remote ON/OFF control, power good circuitry, and protection features against over-voltage and over-power are implemented. It directly senses all the output rails for OVP without the need of external dividers. An innovated AC-signal sampling circuitry provides a sufficient power-down warning signal for PG.

A built-in timer generates accuracy timing for control circuit, including the PS-off delay. The cycle-by-cycle PWM switching prevents the power transformer from saturation and ensures the fastest response for the short-circuit protection, which greatly reduces the stress for power transistors.

Utilizing minimum external components, the FAN6103 includes all of the functions for push-pull and/or half-bridge topology, decreasing the production cost and PCB space, while increasing the mean time between failures for power supply

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FAN6103NZ	-40°C to +105°C	RoHS	16-Pin Dual Inline Package (DIP)	Tube

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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Application Diagram

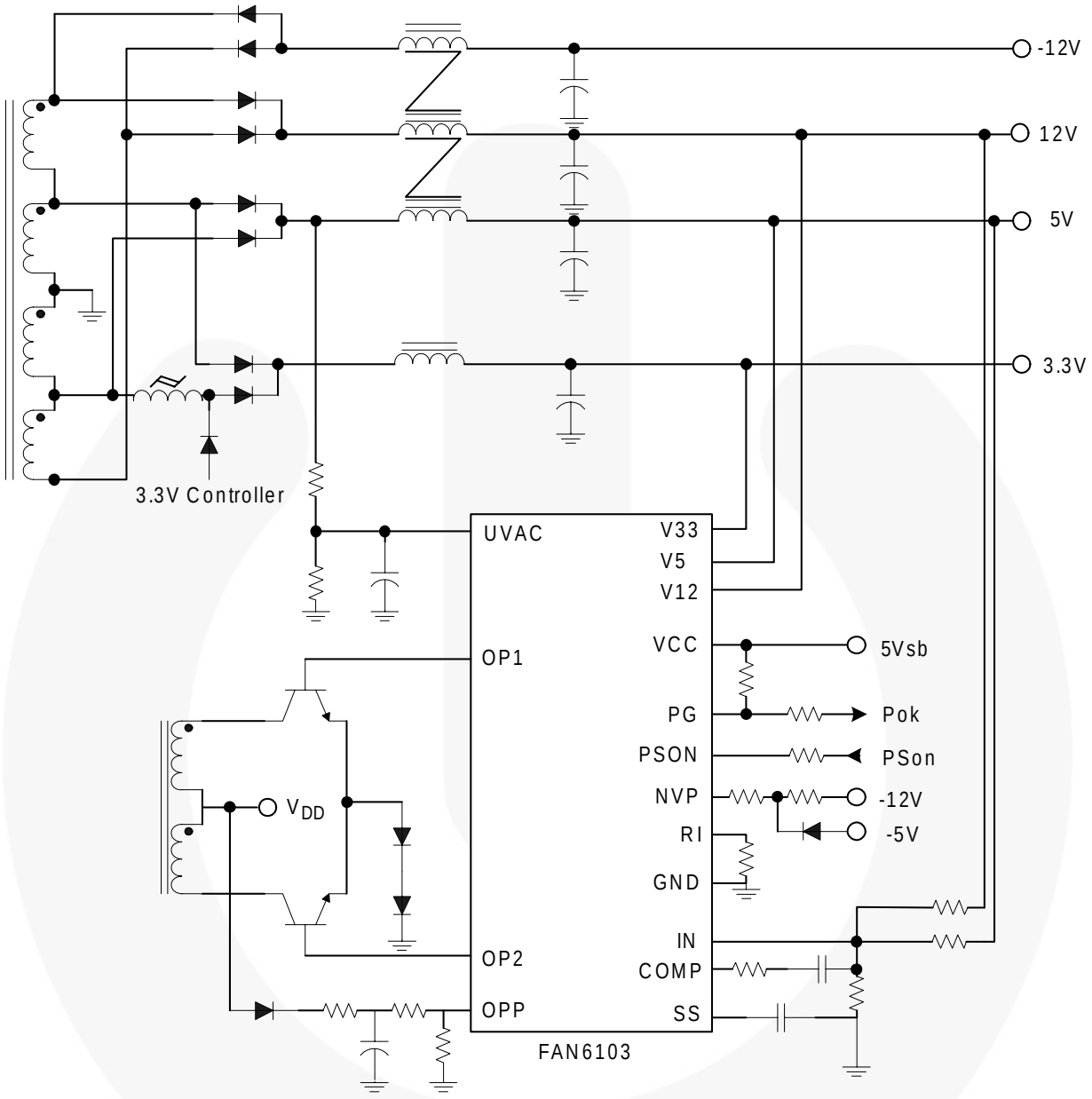


Figure 1. Typical Application

Block Diagram

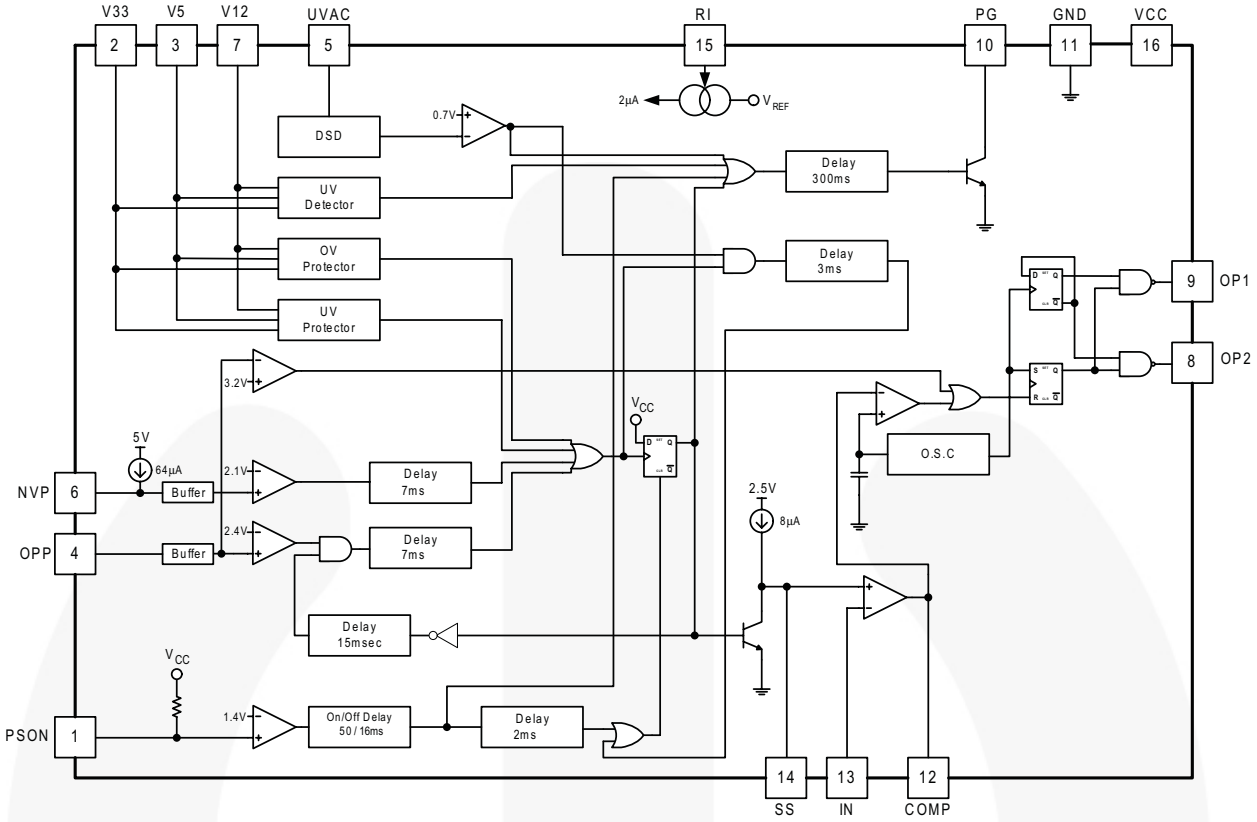
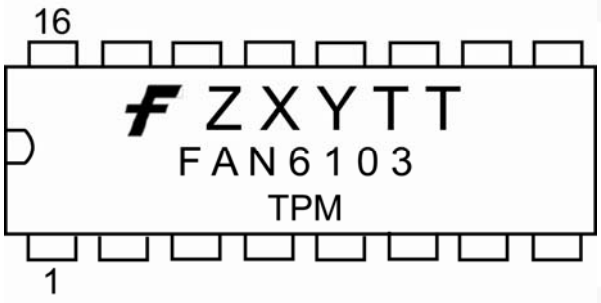


Figure 2. Function Block Diagram

Marking Information



F – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 1-Digit Week Code
TT – 2 -Digit Die Run Code
T – Package Type (N:DIP)
P – Z: Pb Free
M – Manufacture Flow Code

Figure 3. Top Mark

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Pin Configuration

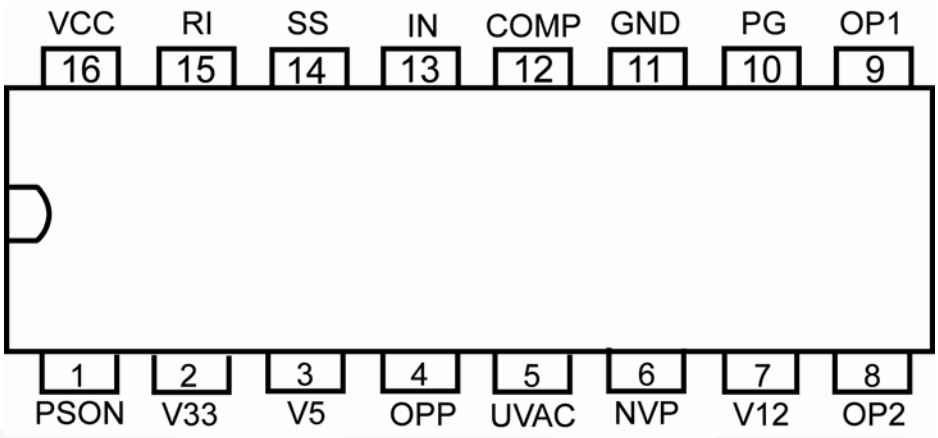

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	PSON	**Remote on/off logic input**. Turn on/off the PWM output after the 16ms / 50ms delay. PSON = 0 means that the main SMPS is operational. PSON = 1 means that the main SMPS is off and the latch is reset.
2	V33	**3.3V over-voltage/under-voltage control sense input**.
3	V5	**5V over-voltage/under-voltage control sense input**.
4	OPP	**Over-power sense input**. This pin is connected to driver transformer or the output of current transformer. When not in use, this pin should be grounded.
5	UVAC	**AC-fail detection**. Detect main AC voltage under-voltage or failure.
6	NVP	**The protection input for negative output**, such as –12V and/or –5V; trip voltage = 2.1V.
7	V12	**12V over-voltage/under-voltage control sense input**.
8	OP2	**The totem-pole output drivers of push-pull PWM**. The output are enabled (LOW) only when the NAND gate inputs are HIGH; the maximum duty cycle on output OP2 is 46%.
9	OP1	**The totem-pole output drivers of push-pull PWM**. The output are enabled (LOW) only when the NAND gate inputs are HIGH the maximum duty cycle on output OP1 is 46%.
10	PG	**Power-good logic output, 0 or 1 (open-collector)**. PG = 1 means that the power is ready for operation. The PG delay is 300ms.
11	GND	**Ground**.
12	COMP	**Error amplifier output and the input of the PWM comparator**.
13	IN	**The negative input of error amplifier**. The positive input of error amplifier is a 2.5V reference voltage.
14	SS	**The soft-start**, it is settable through an external capacitor. The current source output at this pin is 8μA and the voltage is clamped at 2.5V.
15	RI	**Reference Resistor**. Connected to external resistor for the reference setting.
16	VCC	**Supply voltage**; 4.5V ~ 5.5V, connected to 5V standby.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	DC Supply Voltage			16	V
V_H	Supply Voltage on PSON, V33, V5, V12, OP1, OP2 Pins		-0.3	16.0	V
V_L	Supply Voltage on OPP, UVAC, RI, SS , NVP, IN, COMP, PG Pins		-0.3	7.0	V
I_{OUT}	Output Current at PG			30	mA
P_D	Power Dissipation T_A < 50°C			1500	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			82.5	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Soldering)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		3000	V
		Charged Device Model, JESD22-C101		1250	

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

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Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, and R_I = 75kΩ unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
V_{CC} Section							
V_{CC}	DC Supply Voltage			4.5		5.5	V
I_{CC1}	Total Supply Current		PSON = LOW, OP1/OP2 = 1000pF			10	mA
I_{CC2}	Total Supply Current		PSON = HIGH, OP1/OP2 = 1000pF		5	10	mA
Protection Section							
V_{OVP}	Over-Voltage Protection	3.3V		3.9	4.1	4.3	V
		5.0V		5.8	6.1	6.5	V
		12.0V		13.9	14.5	14.9	V
V_{UVP}	Under-Voltage Protection	3.3V		2.0	2.6	2.8	V
		5.0V		3.0	3.6	3.9	V
		120V		6.0	7.2	8.0	V
V_{UVS}	Under-Voltage Sense for PG Low	3.3V		2.5	2.8	3.0	V
		5.0V		4.0	4.3	4.5	V
		12.0V		9.4	10.1	10.4	V
V_{OPP}	Over-Power Protection (with T_{OPP} Delay Time) (3)		V_{UVAC} = 1.5V	2.25	2.32	2.39	V
V_{OPPH}	Over-Power Protection (without Delay Time)			3.0	3.2	3.4	V
V_X	Disable Under-Voltage / Over-Power Protection Threshold			0.2	0.3	0.4	V
V_{NVP}	Negative Voltage Protection Voltage Level			2.0	2.1	2.2	V
I_{NVP}	Negative Voltage Protection Source Current			63	67	71	µA
T_{OVP}	Timing for Over-Voltage Protection			0.37	0.70	1.35	ms
T_{UVP}	Timing for Under-Voltage Protection			0.80	2.40	3.75	ms
T_{UVS}	Timing for Under-Voltage Sense for PG Low			0.37	1.20	1.88	ms
T_{OPP}	Timing for Over-Power Protection			5	7	9	ms
T_{NVP}	Timing for Negative Voltage Protection			3.3	7.0	10.2	ms
PWM Output Section							
V_{OL}	Output Voltage Low					0.8	V
V_{OH}	Output Voltage High			4			V
R_O	Output Impedance of V_{OH}			1.5		3.3	kΩ

Note:

3. $V_{OPPS} = (2/3) \cdot V_{OPP} + (1/3) \cdot V_{UVAC}$.

Continued on following page…

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Electrical Characteristics (Continued)

V_{CC} = 5V, T_A = 25°C, and R_I = 75kΩ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power-Good Section						
t_{PG}	Timing for PG Delay	R_I = 75kΩ	200	300	400	ms
V_{UVAC}	UVAC Voltage Sense for PG		0.68	0.70	0.72	V
t_R	PG Good Output Rising Time	C_L = 100pF, Pull 2.25V to 5.00V		1	3	µs
t_F	PG Good Falling Time	C_L = 100pF, Pull to 5.00V to 2.25V		300	500	ns
V_{OL2}	PG Output Saturation Level	I_{PG} = 10mA			0.5	V
I_{ON2}	PG Leakage Current Collector	V_{PG} = 5V			1	µA
Remote ON/OFF Section						
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
$V_{HYSTERESIS}$	PSON Input Hysteresis Voltage		0.3			V
I_{PSON}	Remote Input Driving Current				0.5	mA
$t_{PSON(ON)}$	Timing PSON to ON	R_I = 75kΩ	38	50	62	ms
$t_{PSON(OFF)}$	Timing PSON to OFF	R_I = 75kΩ	8	16	24	ms
t_{PSOFF}	Timing PG LOW to Power OFF	R_I = 75kΩ	1.5	2.0	6.3	ms
Error Amplifier Section						
V_{REF}	Reference Voltage	T_A = 25°C	2.46	2.50	2.54	V
I_{IB}	Input Bias Current				0.1	µA
A_{VOL}	Open-Loop Voltage Gain		50	60		dB
BW	Unity Gain Bandwidth		0.3	1.0		MHz
PSRR	Power Supply Rejection Ratio		50			dB
Oscillator Section						
f_{OSC}	PWM Frequency	R_I = 75kΩ	62	65	68	kHz
DC_{MAX}	Max Duty Cycle		85		93	%
Soft-Start Section						
I_{SS}	Charge Current		7	8	9	µA

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Typical Performance Characteristics

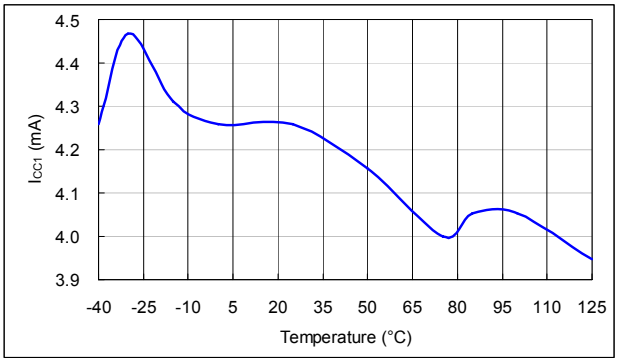


Figure 5. Operating Supply Current vs. Temperature

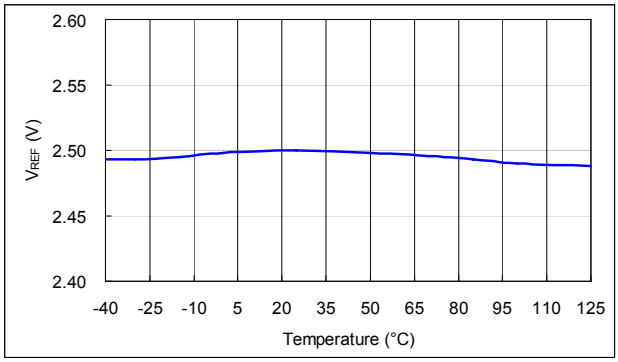


Figure 6. Reference Voltage vs. Temperature

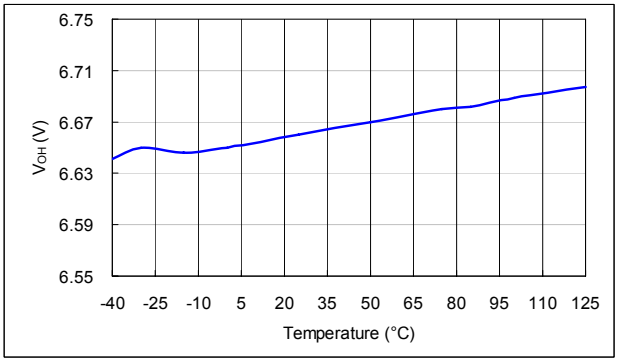


Figure 7. PWM Output Voltage vs. Temperature

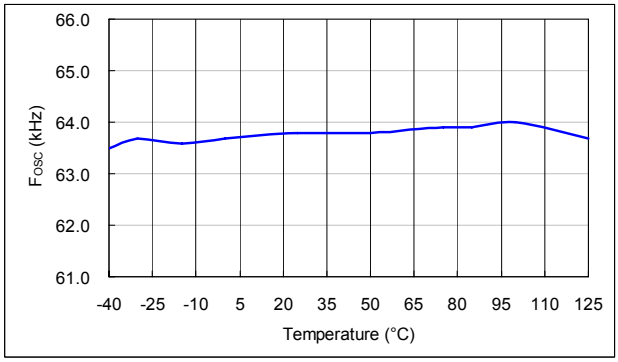


Figure 8. Frequency vs. Temperature

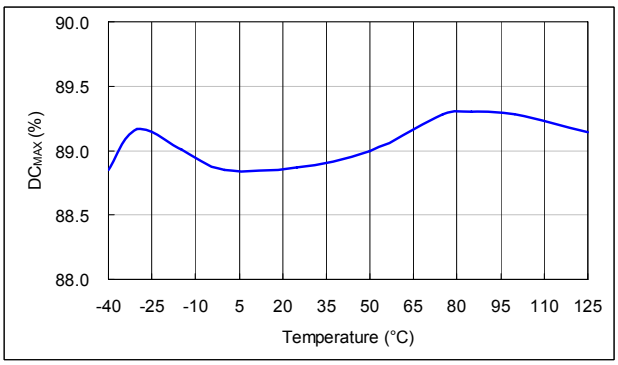


Figure 9. Maximum Duty Cycle vs. Temperature

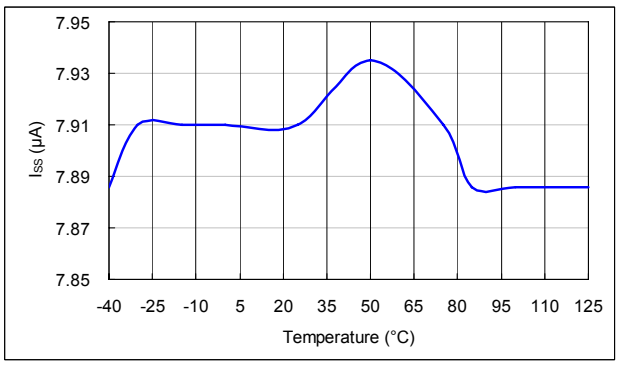


Figure 10. Charge Current vs. Temperature

Typical Performance Characteristics (Continued)

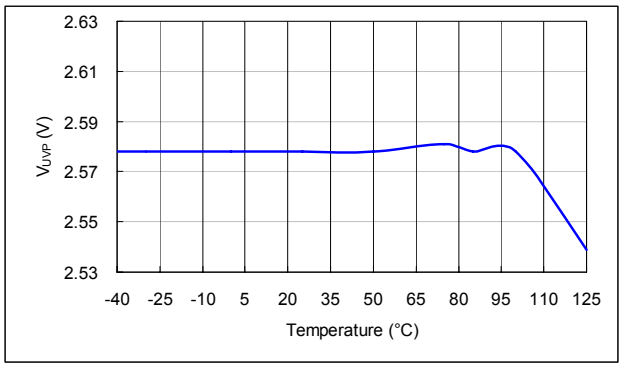


Figure 11. 3.3V V_{UVP} vs. Temperature

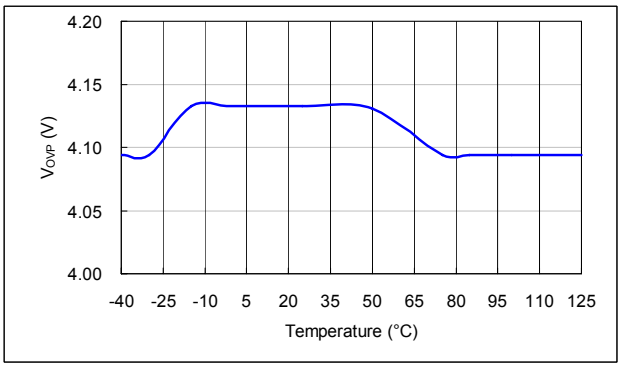


Figure 12. 3.3V V_{OVP} vs. Temperature

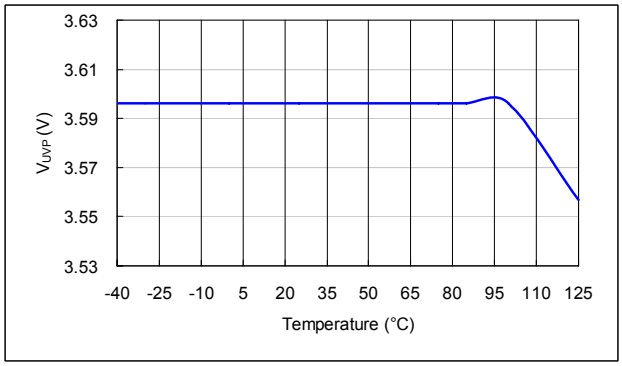


Figure 13. 5V V_{UVP} vs. Temperature

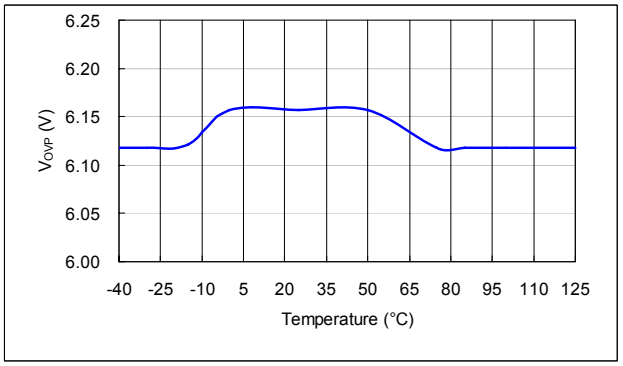


Figure 14. 5V V_{OVP} vs. Temperature

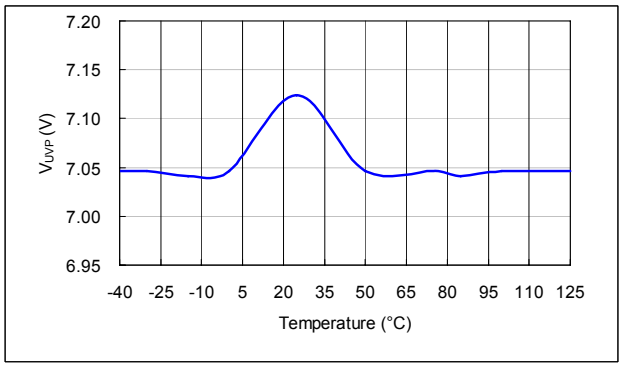


Figure 15. 12V V_{UVP} vs. Temperature

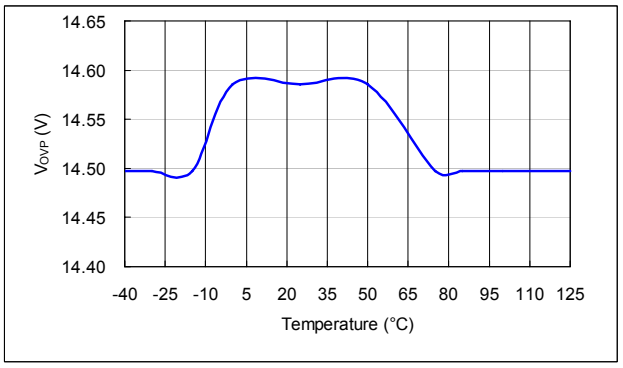


Figure 16. 12V V_{OVP} vs. Temperature

Functional Description

FAN6103 is suitable for half-bridge, push-pull topology and incorporates with a three-channel supervisor. The PWM section comprises a built-in 65KHz oscillator and high-immunity circuits, which protect the system from noise interference and provide more noise margins. FAN6103 has OVP and UVP for 12V, 5V, and 3.3V. NVP is used for negative voltage protection, such as -12V and/or -5V. The UVAC is applied to detect AC line condition.

Over-Power Protection (OPP)

FAN6103 provides over-power protection to detect over-power or short-circuit conditions. When it detects the voltage level over 2.4V, the supervisor triggers PG to LOW and pulls the SS pin LOW to switch off the power.

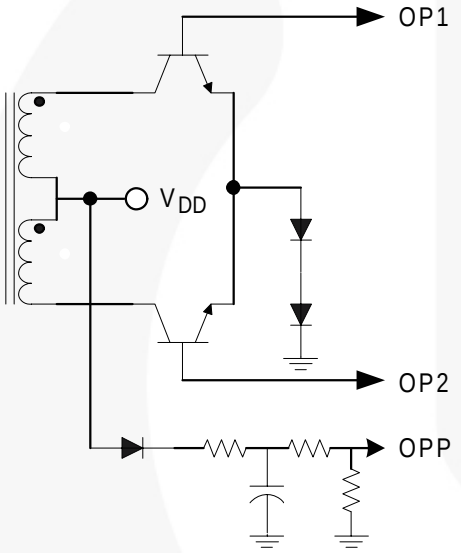


Figure 17. OPP Protection Circuit

Negative-Voltage Protection (NVP)

The NVP provides an under-voltage protection for negative voltage output. An under-voltage represents the phenomenal of the overload condition in negative voltage output. For example, the -12V output may drop to -10V during the overload situation. A resistor determining the threshold of the protection is connected from pin NVP to the negative voltage output. Via this resistor, NVP output a 64µA constant current to the negative voltage output. When the NVP voltage is over 2.1V for longer than 7ms, FAN6103 locks the power output off:

$$V_{NVP} = 64\mu A \times (R_1 + R_2) + (-12V) \quad (1)$$

The power outputs are locked off when V_{NVP} > 2.1V.

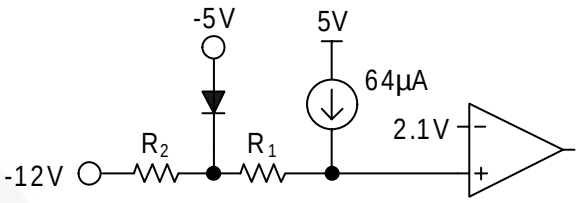


Figure 18. NVP Protection Circuit

AC-Fail Detection

Through a resistor divider, UVAC is connected to the secondary power transformer for detecting the AC line condition. Once the voltage of UVAC is lower than 0.7V for a period of time, such as 200µs, the PG signal is pulled LOW to indicate an AC line power-down condition. The voltage amplitude of the PWM switching signal in the secondary power transformer is proportional to the AC line voltage. Adjust the ratio of resistor divider to determine the threshold of power-down warning. A small capacitor is connected from UVAC to ground for filtering the switching noise.

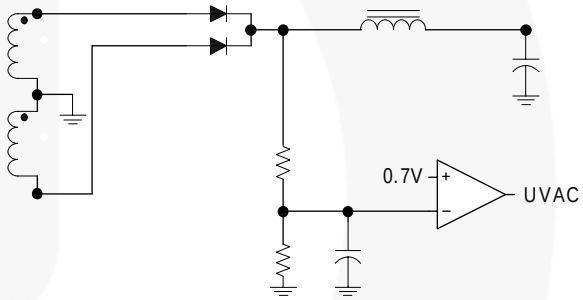


Figure 19. AC Detection Circuit

Timing Chart

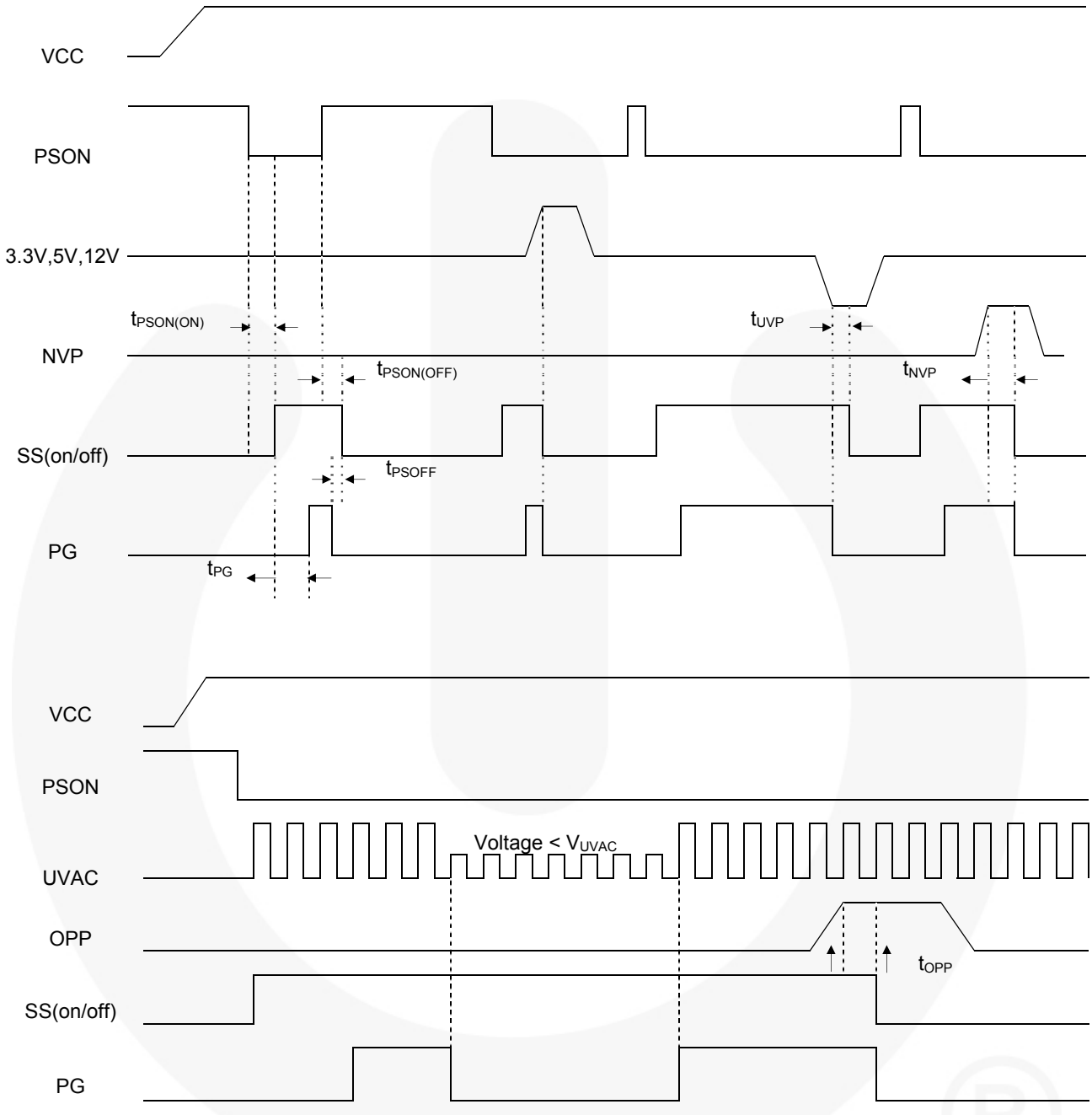
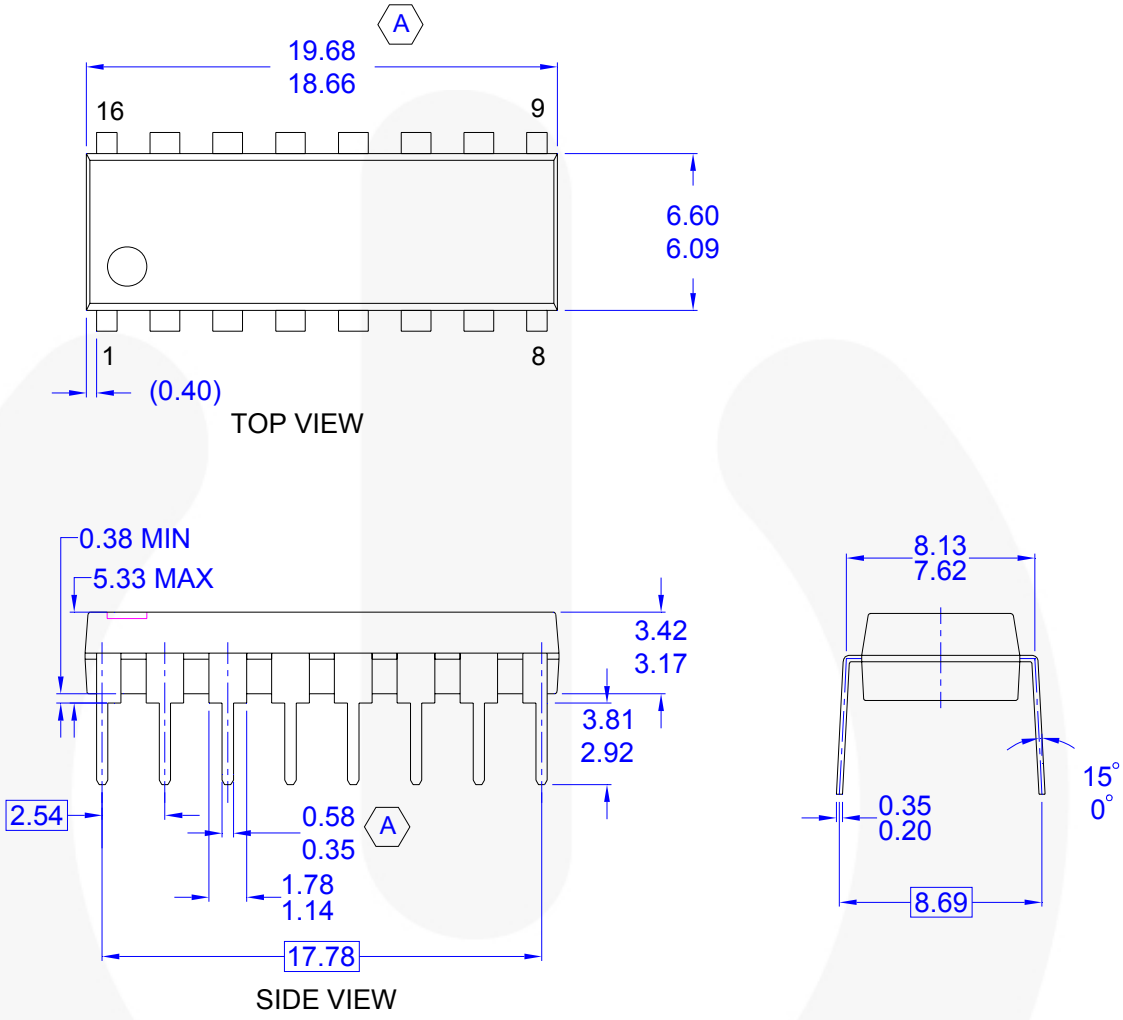


Figure 20. Timing Diagram

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BB

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS

D) CONFORMS TO ASME Y14.5M-1994

E) DRAWING FILE NAME: N16EREV1

Figure 21. 16-Pin Dual In-Line Package (DIP)

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TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
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