700MHz, Crystal-to-LVDS Frequency Synthesizer

ICS8442I-90

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES JANUARY 27, 2015

DATA SHEET

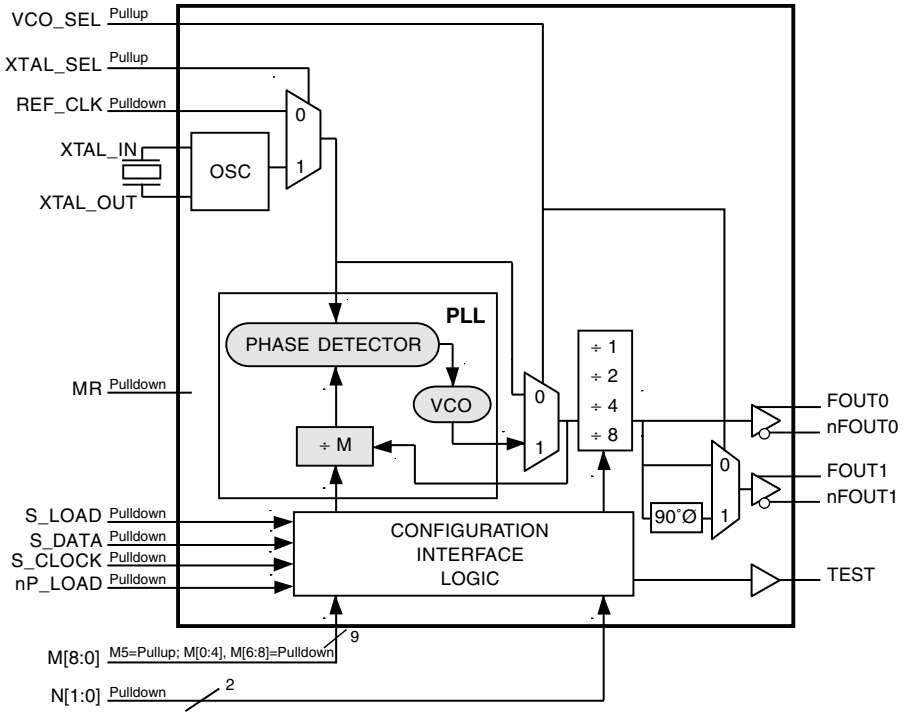
General Description

The ICS8442I-90 is a general purpose, dual output Crystal-to-Differential LVDS High Frequency Synthesizer. The ICS8442I-90 has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels and translates them to LVDS levels. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interface to the configuration logic.

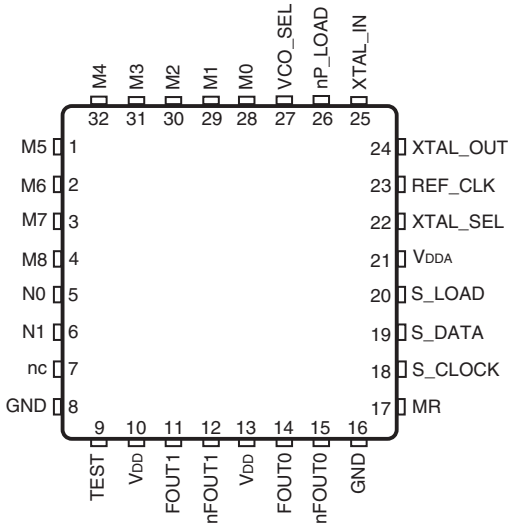
Features

- Dual differential LVDS outputs FOUT1/nFOUT1 lags FOUT0/nFOUT0 by 90°
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_CLK
- Output frequency range: 31.25MHz – 700MHz
- Crystal input frequency range: 10MHz to 25MHz
- VCO range: 250MHz – 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 7ps (maximum), (N= ÷1, ÷2, ÷4)
- Cycle-to-cycle jitter: 34ps (maximum), (N= ÷1, ÷2)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For Replacement device use: 8442BYILF or 8T49N222

Block Diagram



Pin Assignment



ICS8442I-90
32 Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Functional Description

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8442I-90 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVDS output buffers. The divider provides a 50% output duty cycle.

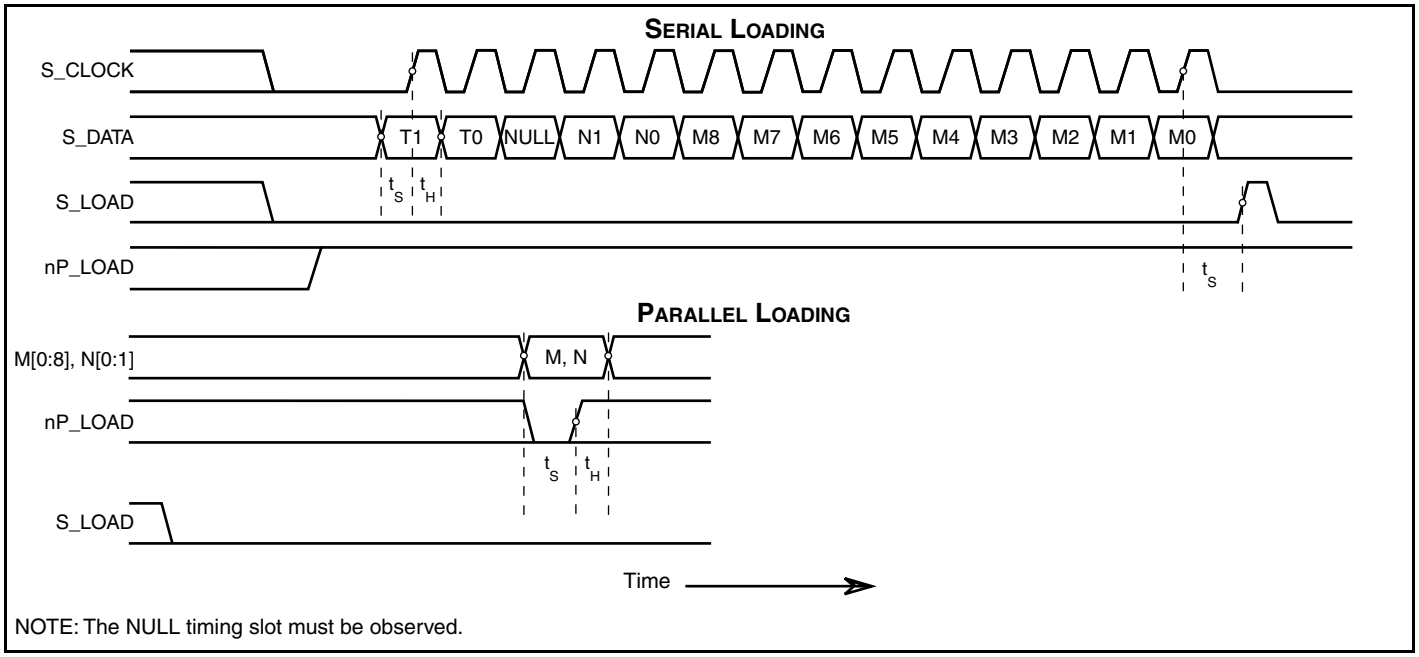
The programmable features of the ICS8442I-90 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: fVCO = fXTAL x M

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $10 \leq M \leq 28$. The frequency out is defined as follows:

$$FOUT = \frac{fVCO}{N} = \frac{fXTAL \times M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_DATA, Shift Register Input
1	0	Output of M Divider
1	1	CMOS f_{OUT}



NOTE: The NULL timing slot must be observed.

Figure 1. Parallel & Serial Load Operations

Table 1. Pin Descriptions

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C Function Table. LVCMOS / LVTTL interface levels.
7	nc	Unused		No connect.
8, 16	GND	Power		Power supply ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTL interface levels.
10, 13	V_{DD}	Power		Core supply pins.
11, 12	FOUT1, nFOUT1	Output		Differential clock outputs for the synthesizer. Lags FOUT0, nFOUT0 by 90°. LVDS interface levels.
14, 15	FOUT0, nFOUT0	Output		Differential clock outputs for the synthesizer. LVDS interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels.
21	V_{DDA}	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when LOW. LVCMOS / LVTTL interface levels.
23	REF_CLK	Input	Pulldown	Single-ended reference clock input. LVCMOS / LVTTL interface levels.
24, 25	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. In bypass mode, VCO_SEL = 0, the differential outputs are phase aligned. NOTE 1. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.
NOTE 1: In bypass mode, VCO_SEL = 0, the differential outputs are phase aligned.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Parallel and Serial Mode Function Table

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. When HIGH, forces the outputs to a differential LOW state (FOUTx = LOW and nFOUTx = HIGH), but does not effect loaded M, N, and T values.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Programmable VCO Frequency Function Table (NOTE 1)

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or REF_CLK input frequency of 25MHz.

Table 3C. Programmable Output Divider Function Table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1 (default)	250	700
0	1	2	125	350
1	0	4	62.5	175
1	1	8	31.25	87.5

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.16	3.3	V_{DD}	V
I_{DD}	Power Supply Current				210	mA
I_{DDA}	Analog Supply Current				16	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	S_LOAD, REF_CLK, M[0:4], M[6:8], N0, N1, MR, S_CLOCK, S_DATA, nP_LOAD	$V_{DD} = V_{IN} = 3.465V$			150	µA
		M5, XTAL_SEL, VCO_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	S_LOAD, REF_CLK, M[0:4], M[6:8], N0, N1, MR, S_CLOCK, S_DATA, nP_LOAD	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		M5, XTAL_SEL, VCO_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1		2.6			V
V_{OL}	Output Low Voltage	TEST; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		494	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25		1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

Table 6. Input Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	REF_CLK; NOTE 1		10		25	MHz
		XTAL_IN, XTAL_OUT; NOTE 1		10		25	MHz
		S_CLOCK				50	MHz
t_R / t_F	Input Rise/Fall Time	S_CLOCK, S_DATA, S_LOAD			6		ns
		nP_LOAD				50	ns

NOTE 1: For the input crystal and REF_CLK frequency range, the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 10MHz, valid values of M are $25 \leq M \leq 70$. Using the maximum frequency of 25MHz, valid values of M are $10 \leq M \leq 28$.

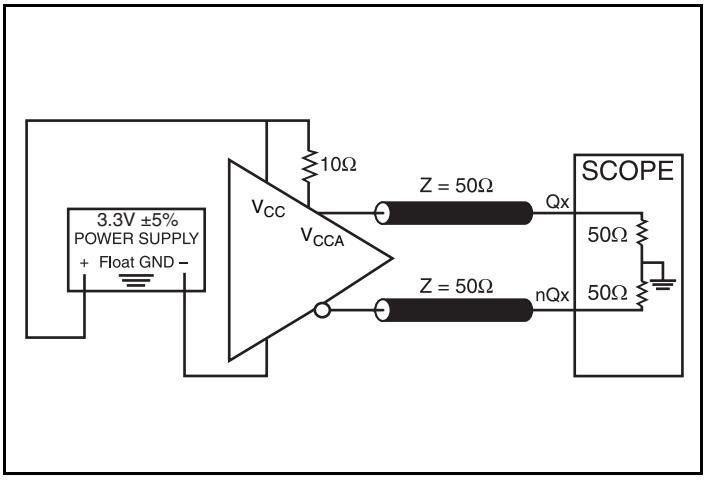
AC Electrical Characteristics

Table 7. AC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, T_A = -40°C to 85°C

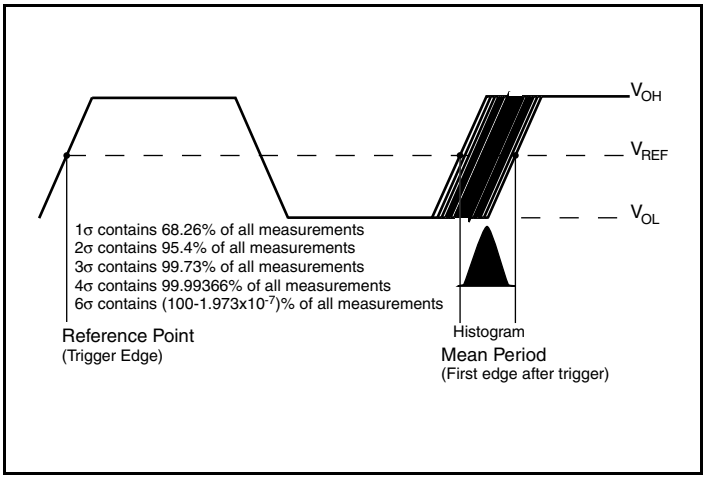
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			31.25		700	MHz
*t*jit(per)	Period Jitter, RMS; NOTE 1, 2		N = ÷1, ÷2, ÷4		4	7	ps
			N = ÷8		7	26	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 2		N = ÷1, ÷2		12	34	ps
			N = ÷4		18	56	ps
*t*phase(Ø)	Output Phase Relationship; NOTE 3				90		°
t_R / t_F	Output Rise/Fall Time		20% to 80%	85		615	ps
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle			45		55	%
t_{LOCK}	PLL Lock Time					1	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Not valid when VCO_SEL = 0.

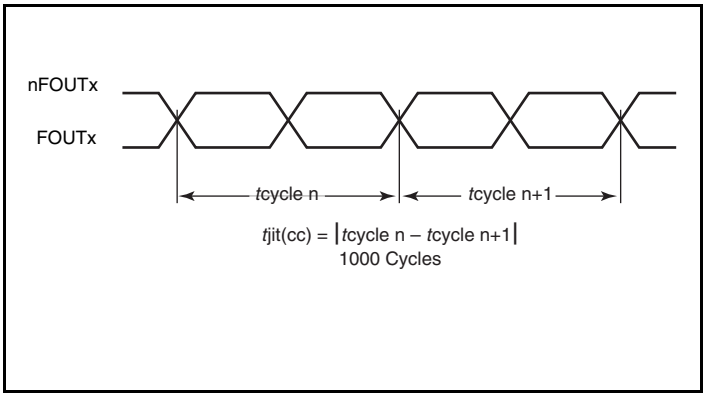
Parameter Measurement Information



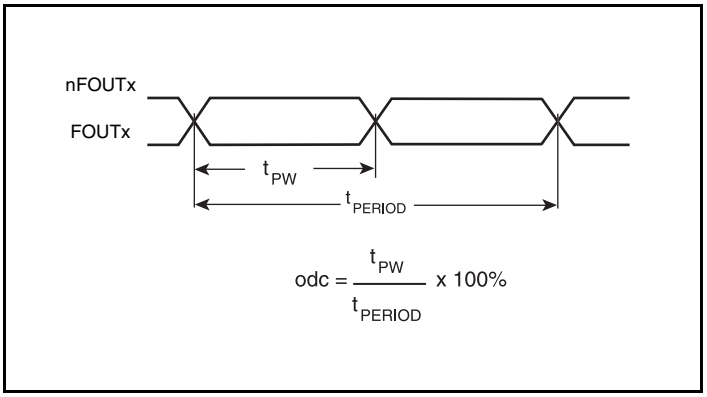
Output Load AC Test Circuit



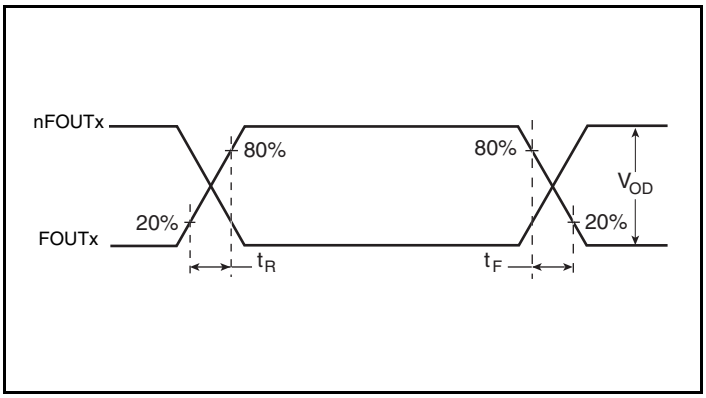
Period Jitter



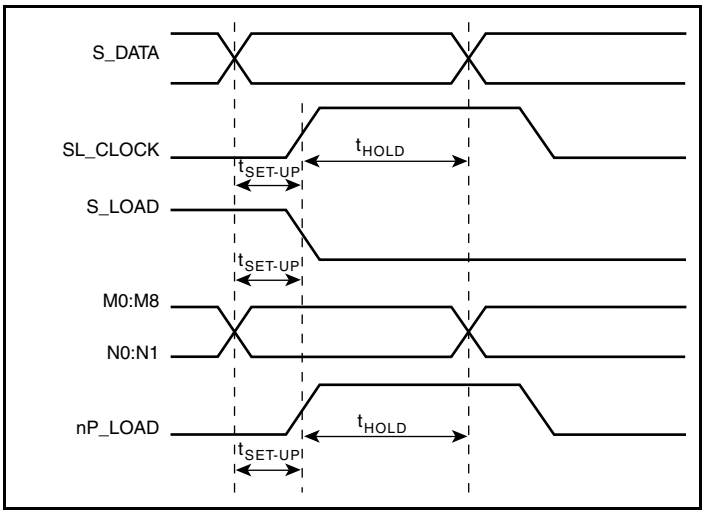
Cycle-to-Cycle Jitter



Output Duty Cycle/Pulse Width/Period

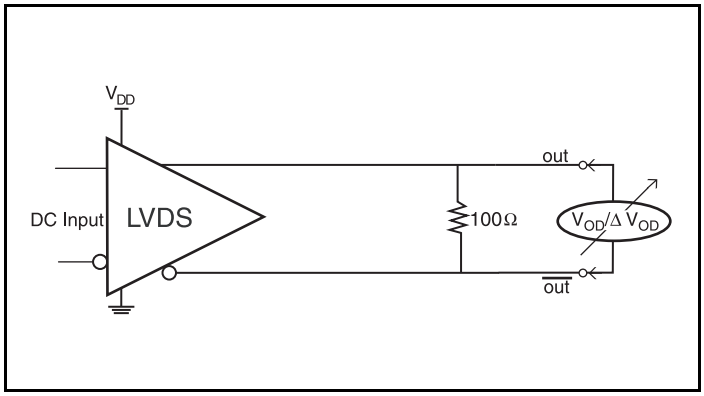


Output Rise/Fall Time

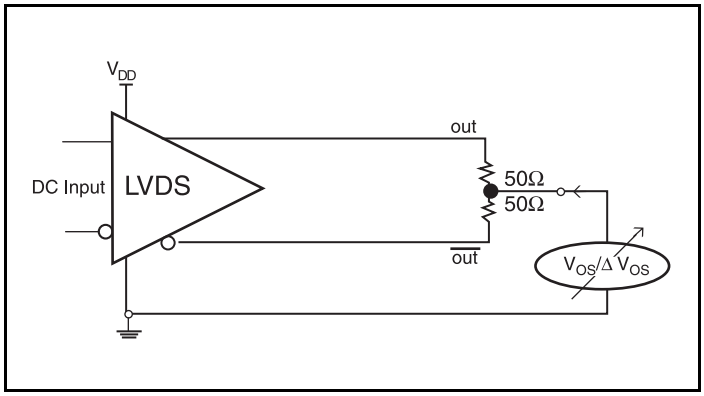


Setup and Hold Time

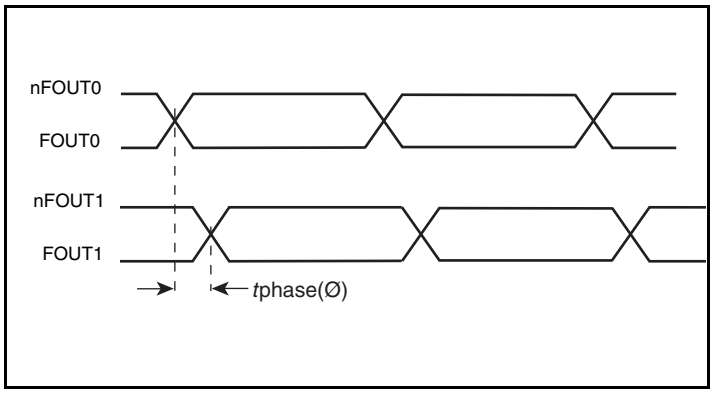
Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup



Output Phase Relationship

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8422I-90 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a 0.01µF bypass capacitor should be connected to each V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

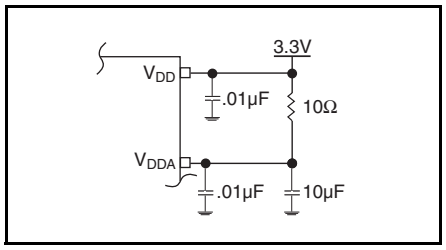


Figure 2. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Crystal Input Interface

A crystal can be characterized for either series or parallel mode operation. The ICS8442I-90 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate frequencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in *Figure 3*. Typical results using parallel 18pF crystals are shown in Table 10.

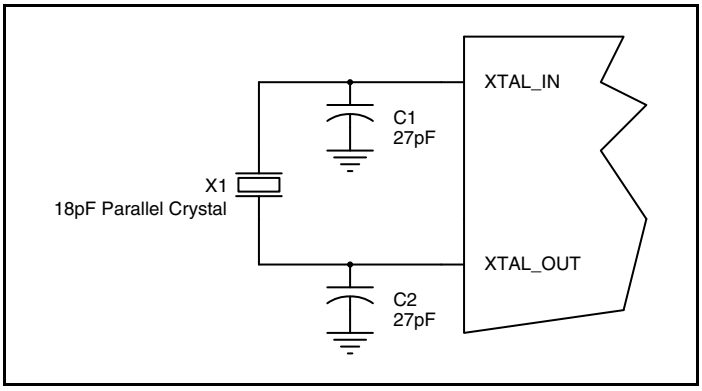


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A*. The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

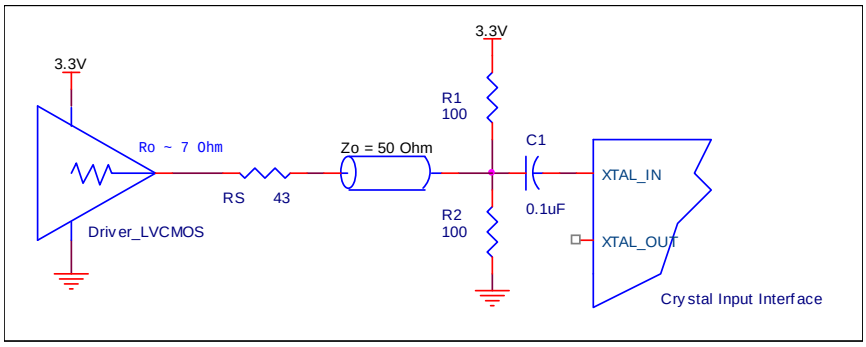


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

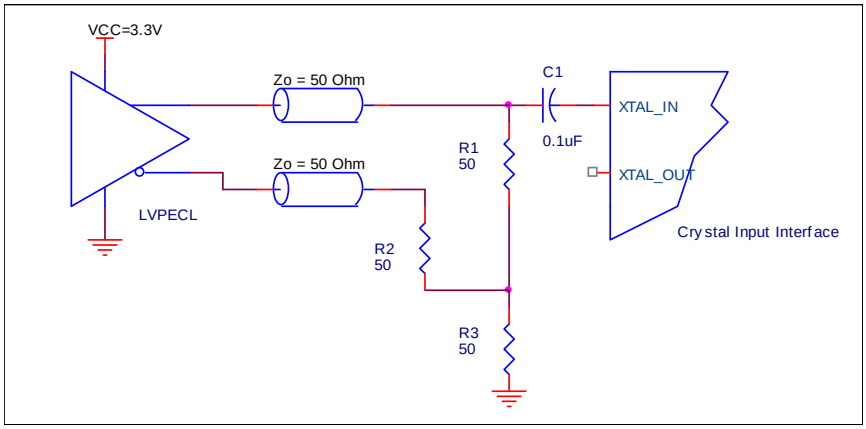


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 5 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

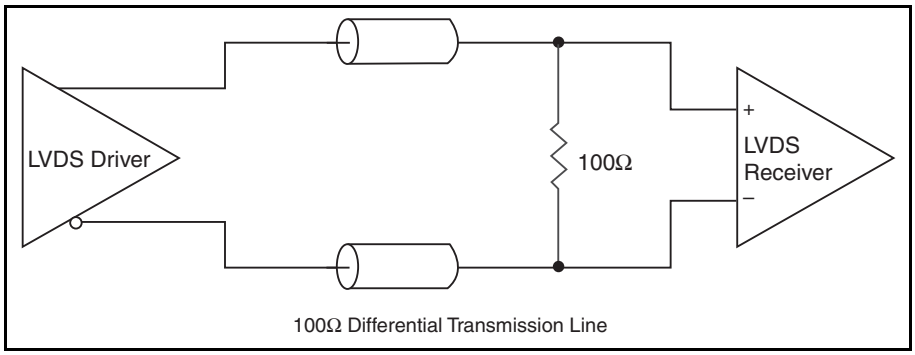


Figure 5. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

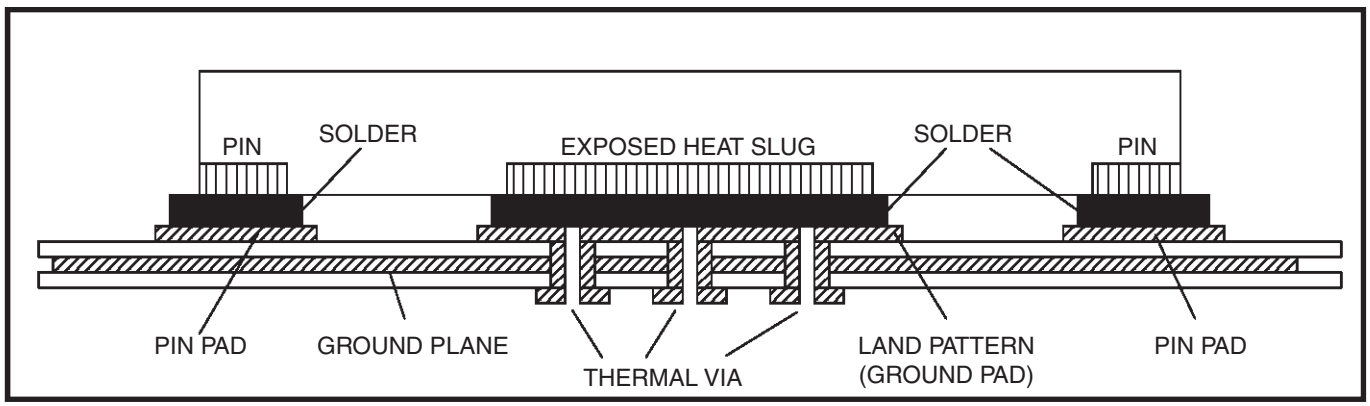


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Layout Guideline

Figure 7 shows an example of ICS8442I-90 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 16MHz crystal is used. The C1 and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS termination are shown in this schematic.

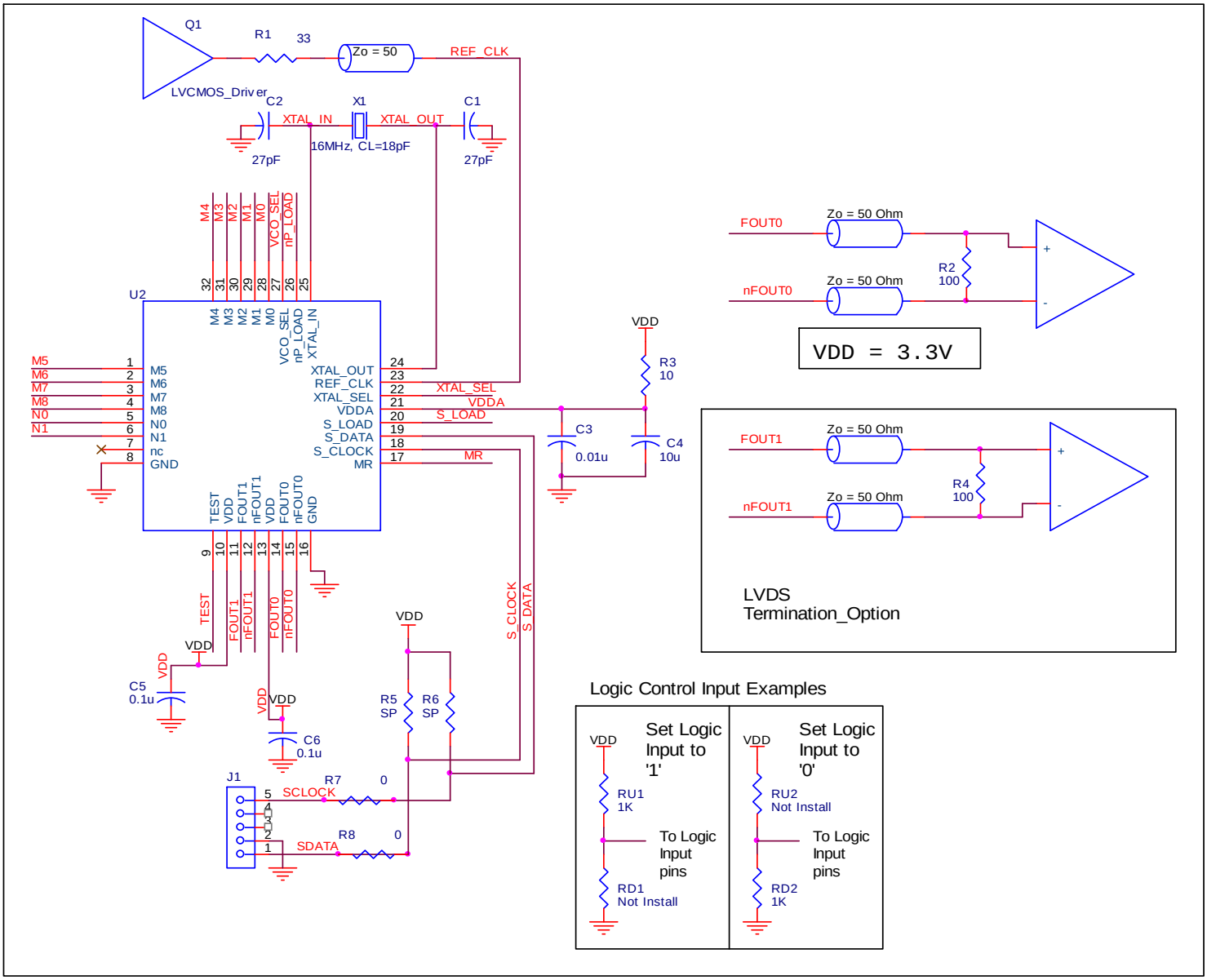


Figure 7. ICS8422I-90 Schematic of Recommended Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8442I-90.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8442I-90 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (210mA + 16mA) = **783.09mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.783W * 37°C/W = 114°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

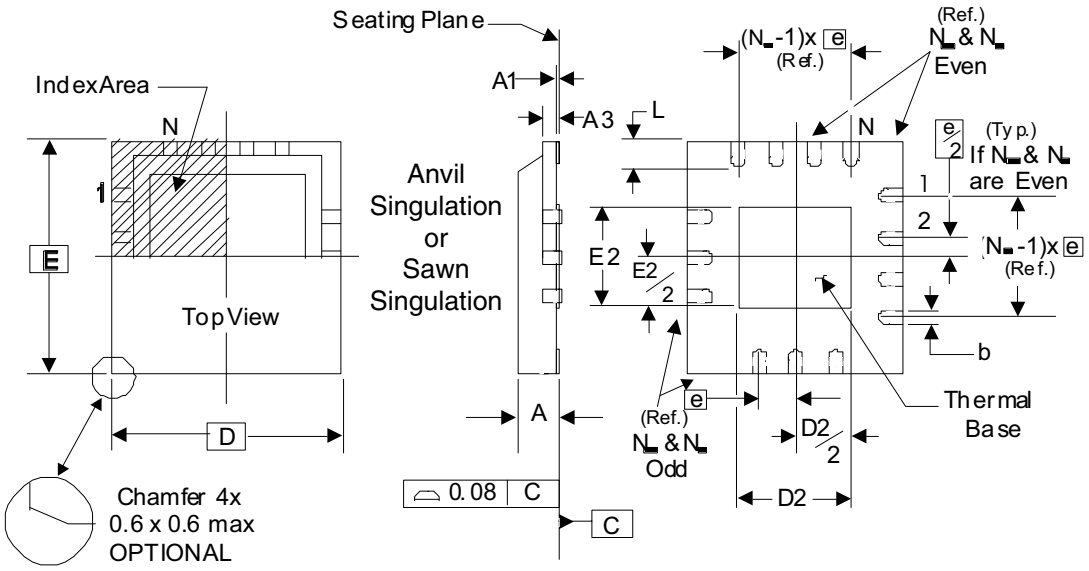
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29°C/W

Transistor Count

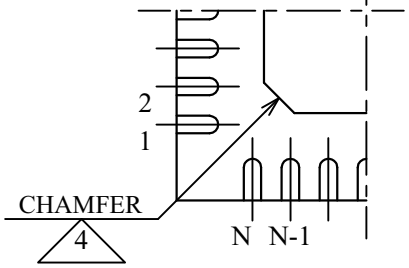
The transistor count for ICS8422I-90 is: 4358

Package Outline and Package Dimensions

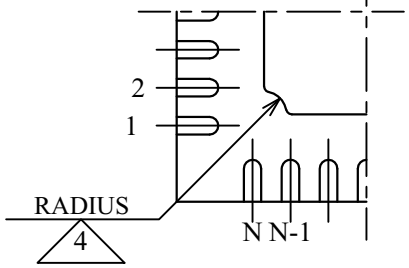
Package Outline - K Suffix for 32 Lead VFQFN



Bottom View w/Type A ID



Bottom View w/Type C ID



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 10. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 10.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B			Product Discontinuation Notice - Last Time Buy Expires January 27, 2015, PDN# CQ-14-02	1/31/14

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8442AKI-90LF	ICS442AI90L	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8442AKI-90LFT	ICS442AI90L	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056