**Si5351A Datasheet Addendum**

**Device Specification Summary for Si5351A-B04486-GT**

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**I$^2$C-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR**

**Crystal Frequency (MHz):** 25.000000000
**Internal Load Capacitance (pF):** 10
**SSC:** Disabled
**Default I2C address:** 0x62

**Output Clock Configuration:**
CLK0 (MHz): 49.152000000 from PLLA
CLK1 (MHz): 24.000000000 from PLLB
CLK2 (MHz): 45.158400000 from PLLB

**Output Driver Configuration:**
CLK0: Powered on, Not inverted, Drive strength = b01 , Output disable state = Low,Clock Source = b11
CLK1: Powered on, Not inverted, Drive strength = b01 , Output disable state = Low,Clock Source = b11
CLK2: Powered on, Not inverted, Drive strength = b01 , Output disable state = Low,Clock Source = b11

| Device Pinout | |
|---|---|
| Pin # | Description |
| 1 | VDD |
| 2 | XA |
| 3 | XB |
| 4 | SCL |
| 5 | SDA |
| 6 | CLK2 |
| 7 | VDDO |
| 8 | GND |
| 9 | CLK1 |
| 10 | CLK0 |

This datasheet addendum is provided as supplemental information to the Si5351-B datasheet available from www.silabs.com/timing