Maxim › Design Support › Technical Documents › Reference Schematics › A/D and D/A Conversion/Sampling Circuits › APP 5839

Keywords: Alameda MAXREFDES24, analog output, programmable logic controllers, industrial control and automation
Related Parts

REFERENCE SCHEMATIC 5839

ALAMEDA (MAXREFDES24#): 4-CHANNEL ANALOG OUTPUT

May 06, 2014

Abstract: The Alameda (MAXREFDES24#) subsystem reference design features four dense, highly accurate analog outputs in a compact, galvanically isolated form factor. Each channel provides current or voltage. This design uniquely fits in programmable logic controllers (PLC), distributed control systems (DCS), and other industrial applications. Hardware, firmware design files, and lab measurements are provided for rapid prototyping and development. The board is also available for purchase.

Introduction

[More detailed image](#) (JPG)

In [PLC](#) and [DCS](#) systems, analog output currents and voltages provide critical control and actuation functions. The [Alameda (MAXREFDES24#)](#) reference design shown in **Figure 1** features four flexible and programmable analog outputs that meet industrial control requirements.

The [MAX5134](#) lies at the heart of the system. This four-channel, 16-bit, high-accuracy [digital-to-analog converter](#) ([DAC](#)) provides [voltage](#) outputs that drive the inputs of four [MAX15500](#) signal conditioners. These signal conditioners produce user-programmable accurate current or voltage outputs. The MAX15500 also provides extensive error reporting. The [MAX6126](#) produces an ultra-high-precision voltage reference for the DAC and the output conditioners. The [MAX14850](#) galvanically isolates data communication from the field side and the system [controller](#).

The Alameda also integrates an isolated, wide DC input range, flyback converter power supply. The peak current-mode flyback controller, [MAX17498B](#), efficiently drives an isolated [transformer](#) and generates ±24V and +8V outputs. The [MAX1659](#) low-dropout ([LDO](#)) [linear regulator](#) then regulates the +8V output to a +5V low-noise output. The entire system requires only a 24V input for power.

The subsystem features all typical bipolar current and voltage output ranges, and appropriate subsets, with less than ±0.1% typical total unadjusted error ([TUE](#)). The circuit also provides open-circuit detection, [brownout](#) detection, overtemperature protection, short-circuit and overcurrent protection, which are all critical for industrial applications. Flexible power-up options make Alameda an ideal choice for robust industrial control systems.
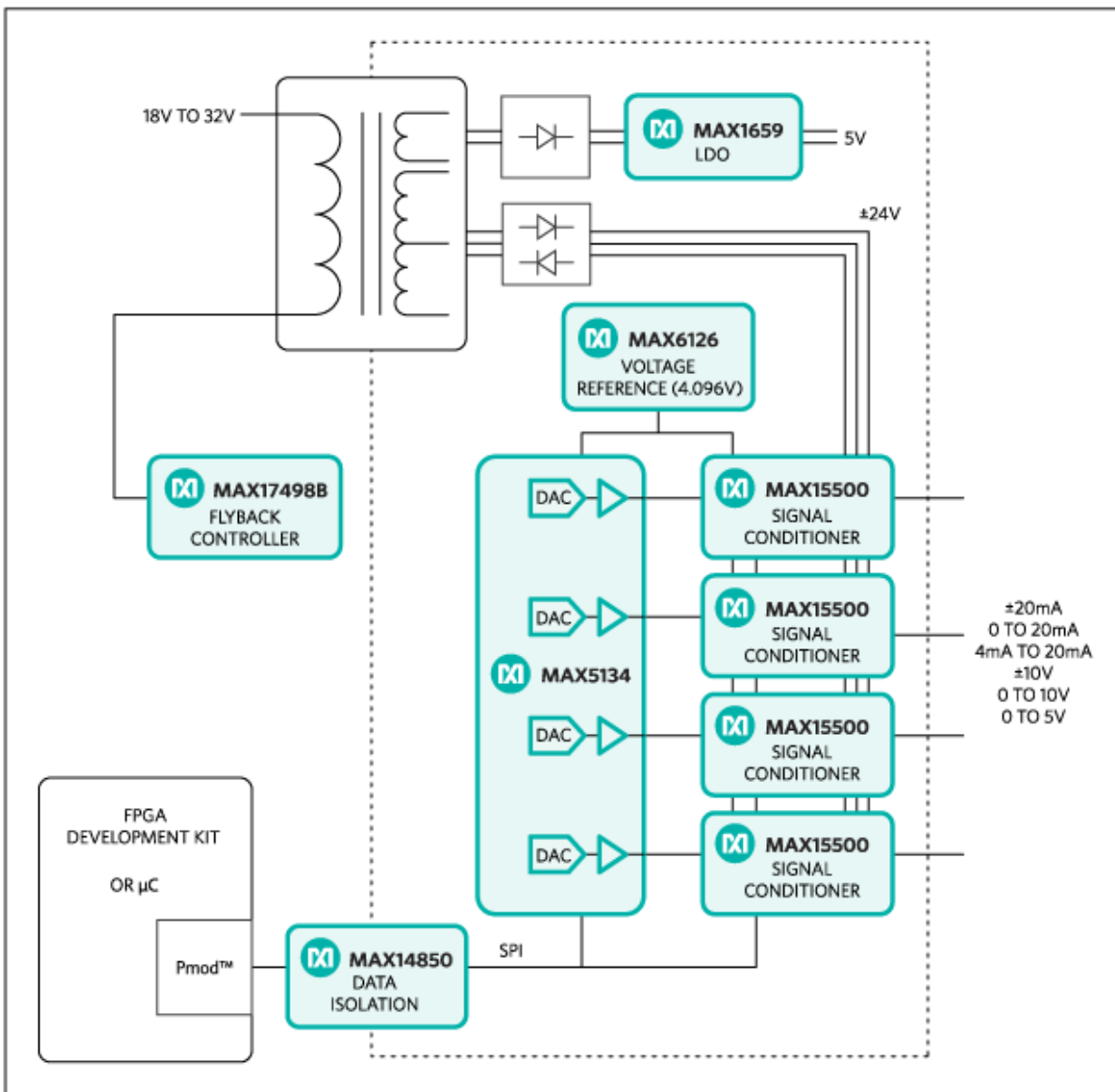
Figure 1. The Alameda subsystem design block diagram.

Features

- Programmable high-accuracy current/voltage output
- Current output drives up to 1kΩ
- Voltage output drives loads down to 1kΩ
- Extensive error reporting
- Isolated power and data
- Device drivers
- Example C source code
- Pmod™-compatible form factor

Competitive Advantages

- Flexibility
- System safety
- Small solution size
- Low cost

Applications

- PLCs
- DCS
- Distributed I/Os
- Embedded systems
- Industrial control and automation
- Industrial sensors

Detailed Description of Hardware

Alameda connects to Pmod-compatible field-programmable gate array (FPGA)/microcontroller development boards. Alameda requires a 3.3V supply voltage from the Pmod connector and uses the SPI pin assignments as illustrated on the right.

The power requirements are shown in **Table 1**. Note that the external +24V power supply is required for full system operation. The currently supported platforms and ports are shown in **Table 2**.

Table 1. Power Requirements for the Alameda Subsystem Reference Design

Power Name	Input Voltage (V)	Input Current (mA, typ)
3.3V Pmod Power Supply	3.3	6
+24V	18 to 32	140

Table 2. Supported Platforms and Ports

Supported Platforms	Communication Ports	Physical Support Ports
LX9 platform (Spartan®-6)	J4	J5 (no electrical connection)
ZedBoard platform (Zynq®-7020)*	JB1	JA1 (no electrical connection)

*Tested with ZedBoard Rev C.

The MAX15500 (U1–U4) is a single-channel, low-cost, precision analog current/voltage output conditioner developed to meet the requirements of PLCs and other industrial control and automation applications. The MAX15500 operates from a ±15V to ±32.5V power-supply range.

The MAX15500 can generate both unipolar and bipolar current and voltage outputs. In current mode, the device produces currents of -1.2mA to +24mA or -24mA to +24mA. In voltage mode, the device produces voltages of -0.3V to +6V, -0.6V to +12V, or ±12V. To allow for overrange and underrange capability in unipolar mode, the transfer function of the MAX15500 is offset so that when the voltage at AIN is 5% of full scale, IOUT is 0mA and VOUT is 0V. Once VAIN attains full scale, VOUT or IOUT becomes full scale +5% or +20% depending on the state of FSMODE.

The MAX15500 protects against overcurrent and short-circuit conditions when OUT goes to ground or a voltage up to ±32.5V. The device also monitors for overtemperature and supply brownout conditions. The supply brownout threshold is programmable between ±10V and ±24V in 2V increments. The MAX15500 provides extensive error reporting of short-circuit, open-circuit, brownout, and overtemperature conditions through the SPI interface and an additional open-drain interrupt output (ERROR). The MAX15500 also includes an analog 0 to 3V output (MON) to monitor the load condition at OUT.

The MAX5134 (U5) is a quad 16-bit, buffered voltage-output, high-linearity DAC. The device features 4-channel, very low deadband (0.02V max) rail-to-rail outputs. For most applications, no negative biasing power supply is required.

The MAX6126 (U6) drives the analog output conditioners and the DAC's reference inputs with an ultra-high-precision 4.096V voltage reference with 0.02% initial accuracy and a 3ppm/°C maximum temperature coefficient (tempco).

The DAC's outputs directly drive the conditioners' inputs with no external components, making the interface simple.

The MAX17498B (U8) provides an isolated, functional insulation class power solution that accepts single +18V to +32V DC voltage and converts it to ±24V and +8V using an isolation transformer in flyback architecture. Post-regulation is accomplished using the MAX1659 LDO (U9) for the 5V output.

Data isolation between the subsystem and the controller is accomplished using the MAX14850 (U7) digital data isolator. The combined power and data isolation achieved is 600V$_{RMS}$.
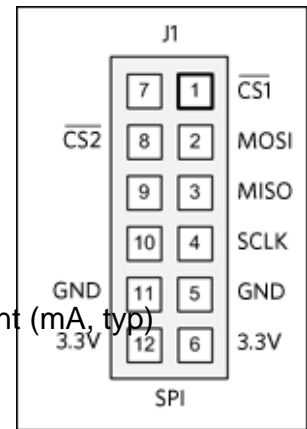
Detailed Description of Firmware for LX9 and ZedBoard Platforms

Table 2 shows the currently supported platforms and ports. Support for additional platforms may be added periodically under Firmware Files in the All Design Files section.

The Alameda firmware released for the LX9 development kit targets a Microblaze™ soft-core microcontroller placed inside a Xilinx® Spartan-6 FPGA. The Alameda firmware also supports the ZedBoard kit and targets an ARM® Cortex®-A9 processor placed inside a Xilinx Zynq system-on-chip (SoC).

The firmware is a working example of how to initiate the system and wait for a user's input. A user can select the output mode and type in the DAC input codes. The simple process flow is shown in **Figure 2**. The firmware is written in C using the Xilinx software development kit (SDK) tool, which is based on the EclipseTM open source standard. Custom Alameda-specific design functions were created utilizing the standard Xilinx XSpi core version 3.03a. The SPI clock frequency is set to 2MHz on the LX9 platform and 3.125MHz on the ZedBoard platform.
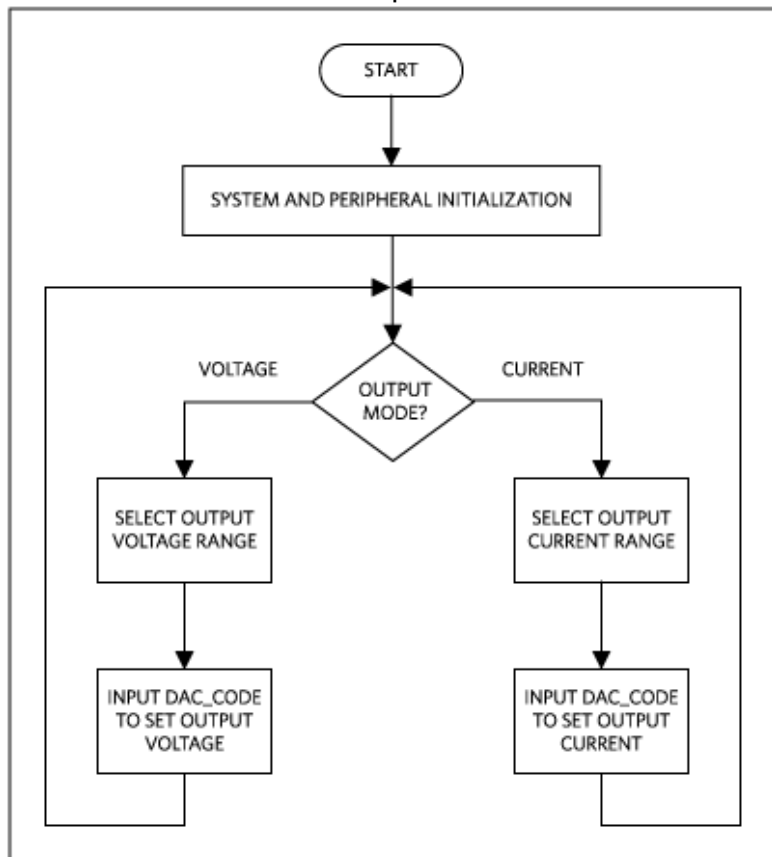
Figure 2. The Alameda firmware flowchart.

The complete source code is provided to speed up customer development. Code documentation can be found with the corresponding firmware platform files.

Quick Start

Required equipment:
- Windows® PC with two USB ports
- Alameda (MAXREFDES24#) board
- Alameda-supported platform (i.e., LX9 development kit or ZedBoard kit)
- One 24V, 150mA minimum DC power supply
- One 750Ω, 0.25W resistor

Download, read, and carefully follow each step in the appropriate Alameda Quick Start Guide:
Alameda (MAXREFDES24#) LX9 Quick Start Guide
Alameda (MAXREFDES24#) ZedBoard Quick Start Guide

Lab Measurements

Equipment used:
- Alameda (MAXREFDES24#) board
- FPGA development kit
- One 750Ω, 0.25W resistor load
- Agilent 3458A digital multimeter
- Agilent E3631A DC power supply (any 24V, 150mA minimum DC power supply works)

National Instruments [GPIB](#) card and [cable](#)
- Thermonics T-2800 precision temperature forcing system
- Perl script for controlling the FPGA development kit and measurement equipment
- Windows PC

INL, DNL, and TUE are the most important specifications for PLC and other process control systems. The MAX15500 is highly flexible and configurable to meet the needs of various applications. The data was taken at +25°C. In the following pictures, the DNL, INL, and TUE for the first 320 DAC codes are shown as 0 because codes 0 to 320 are in the deadband (0 to 0.02V) of the MAX5134.

Measurements of DNL, INL, and TUE for the -10V to +10V voltage output mode, with 20% overrange are shown in **Figure 3**, **Figure 4**, and **Figure 5**, respectively.
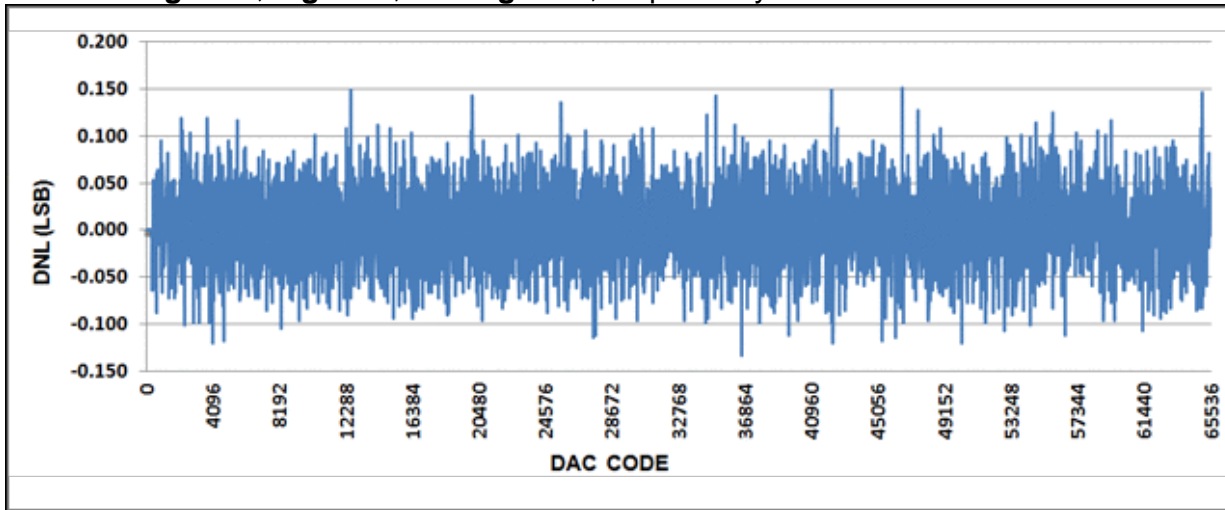
Figure 3. DNL for -10V to +10V output range, with 20% overrange.
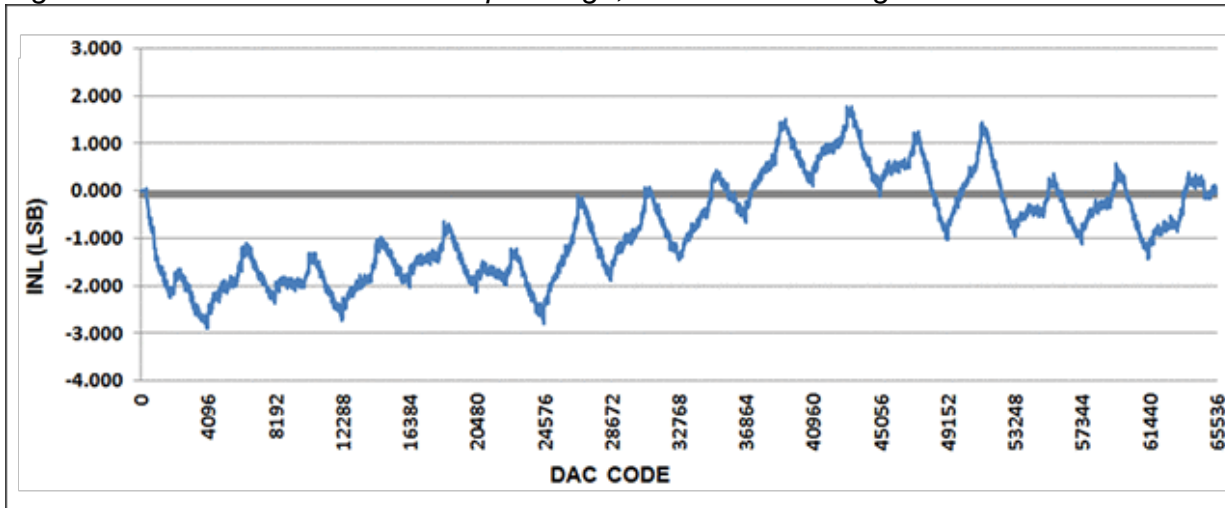
Figure 4. INL for -10V to +10V output range, with 20% overrange.
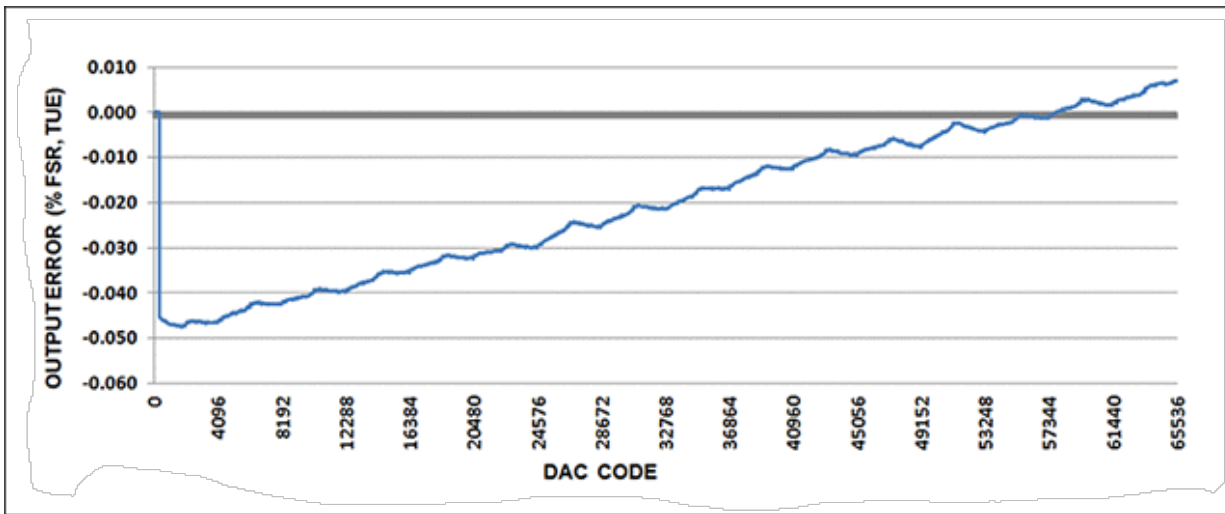
Figure 5. Output error for -10V to +10V output range, with 20% overrange.

Measurements of DNL, INL, and TUE for the 0 to 10V voltage output mode, with 20% overrange are shown in **Figure 6**, **Figure 7**, and **Figure 8**, respectively.
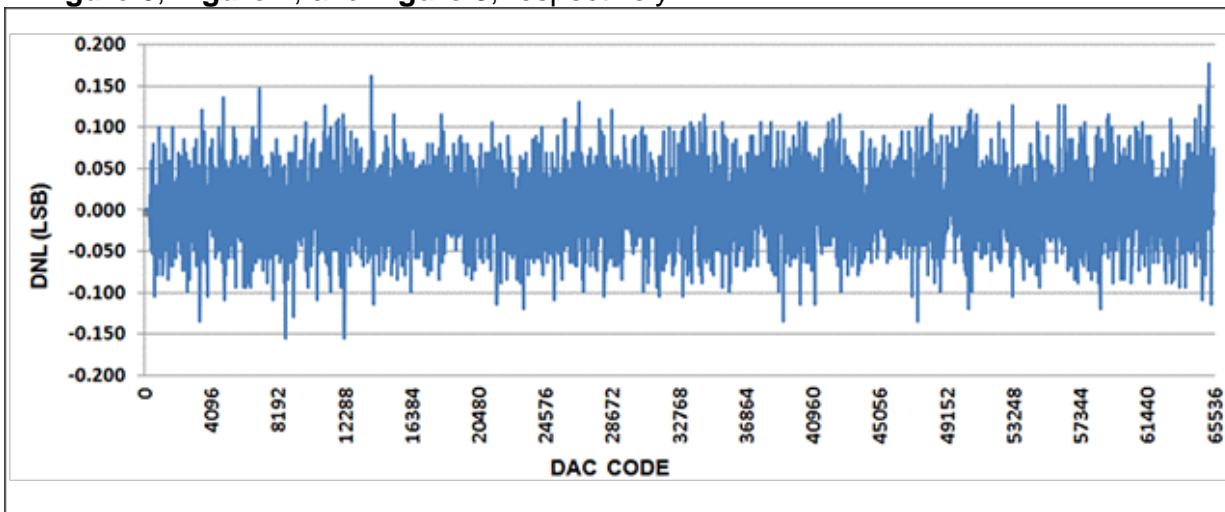
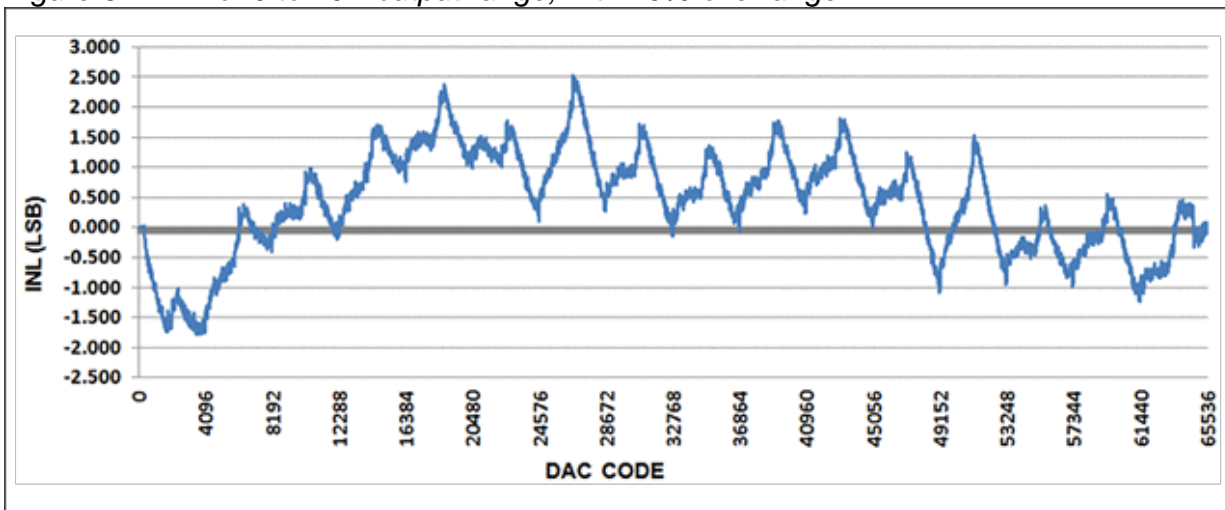*Figure 6. DNL for 0 to 10V output range, with 20% overrange.*

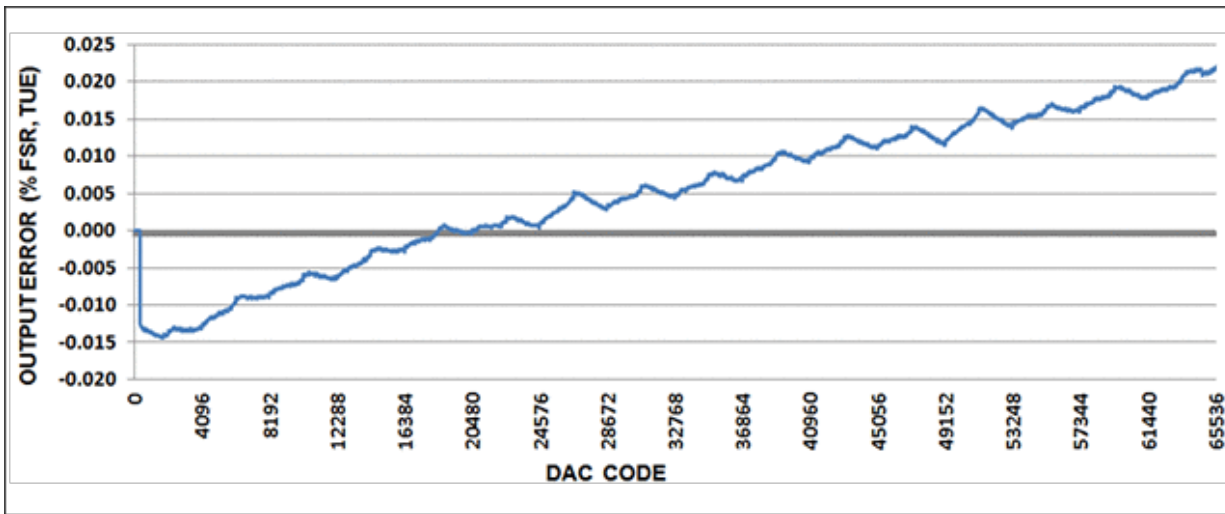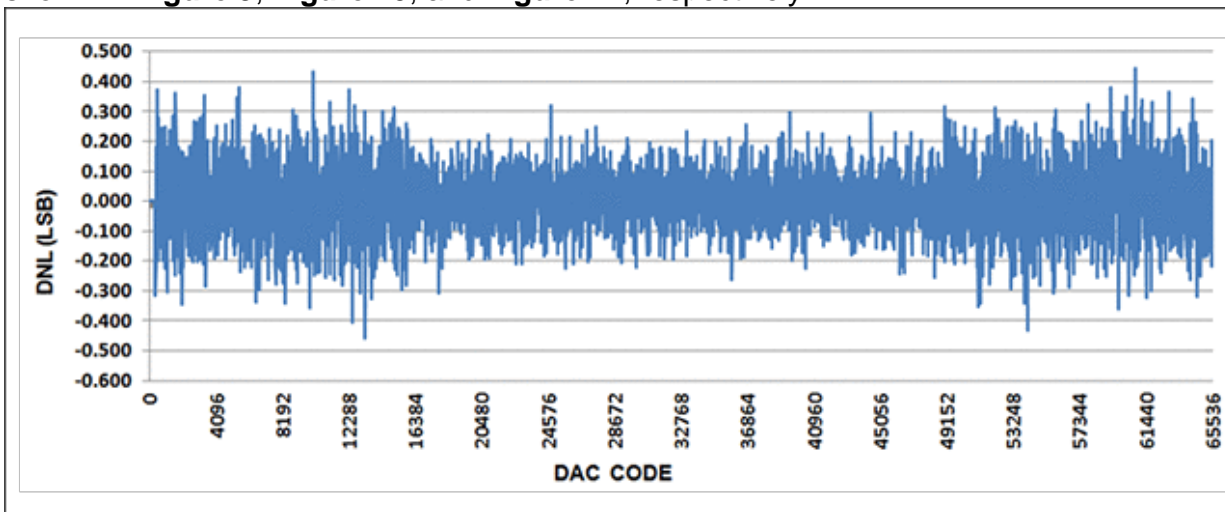*Figure 7. INL for 0 to 10V output range, with 20% overrange.*

Figure 8. Output error for 0 to 10V output range, with 20% overrange.

Measurements of DNL, INL, and TUE for the -20mA to +20mA current output mode, with 20% overrange are shown in **Figure 9**, **Figure 10**, and **Figure 11**, respectively.

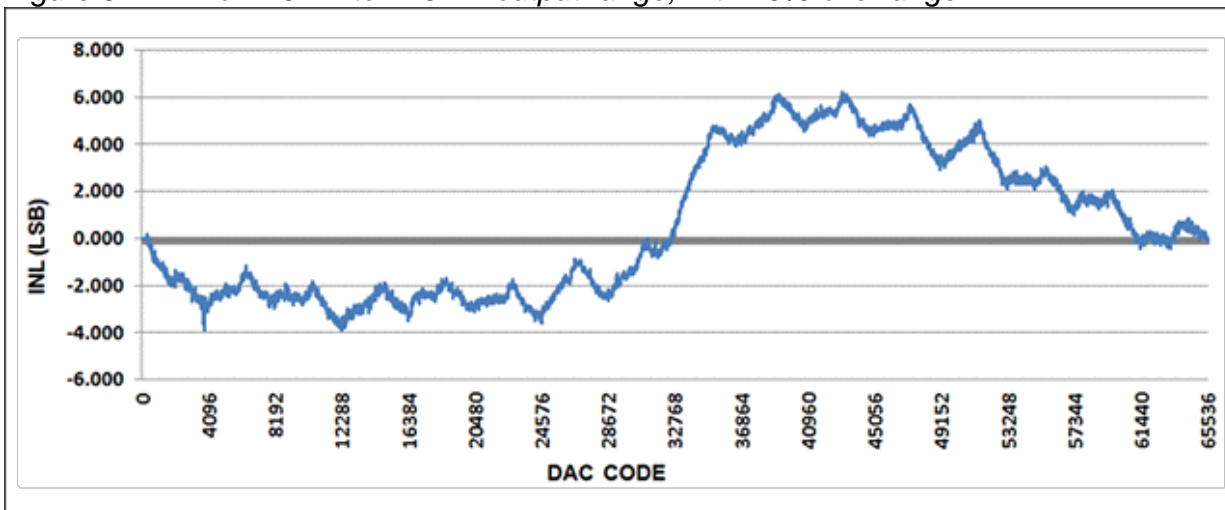*Figure 9. DNL for -20mA to +20mA output range, with 20% overrange.*

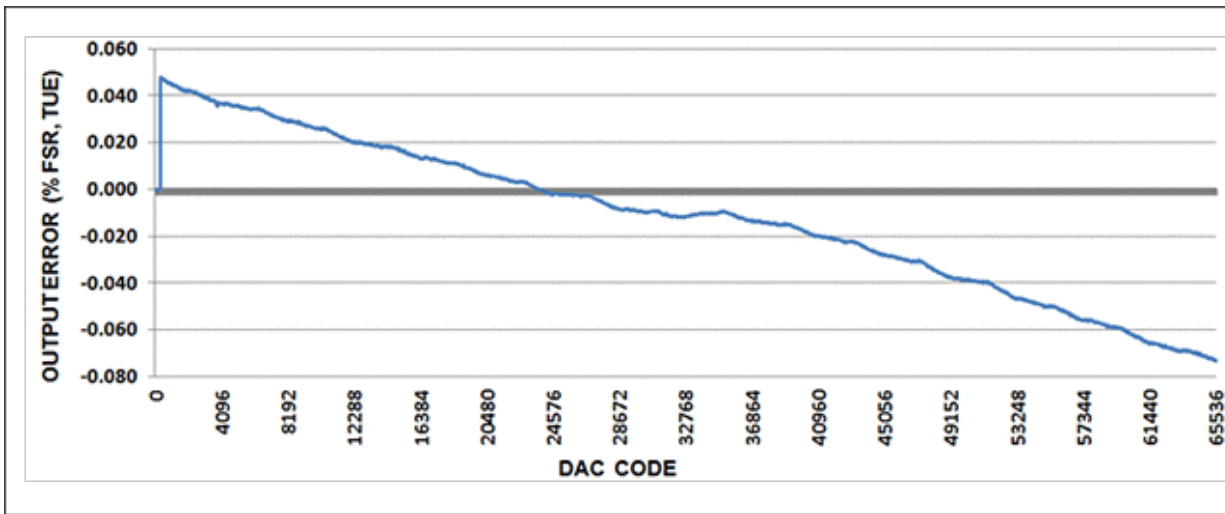*Figure 10. INL for -20mA to +20mA output range, with 20% overrange.*

Figure 11. Output error for -20mA to +20mA output range, with 20% overrange.

Measurements of DNL, INL, and TUE for the 0 to 20mA current output mode, with 20% overrange are shown in **Figure 12**, **Figure 13**, and **Figure 14**, respectively.
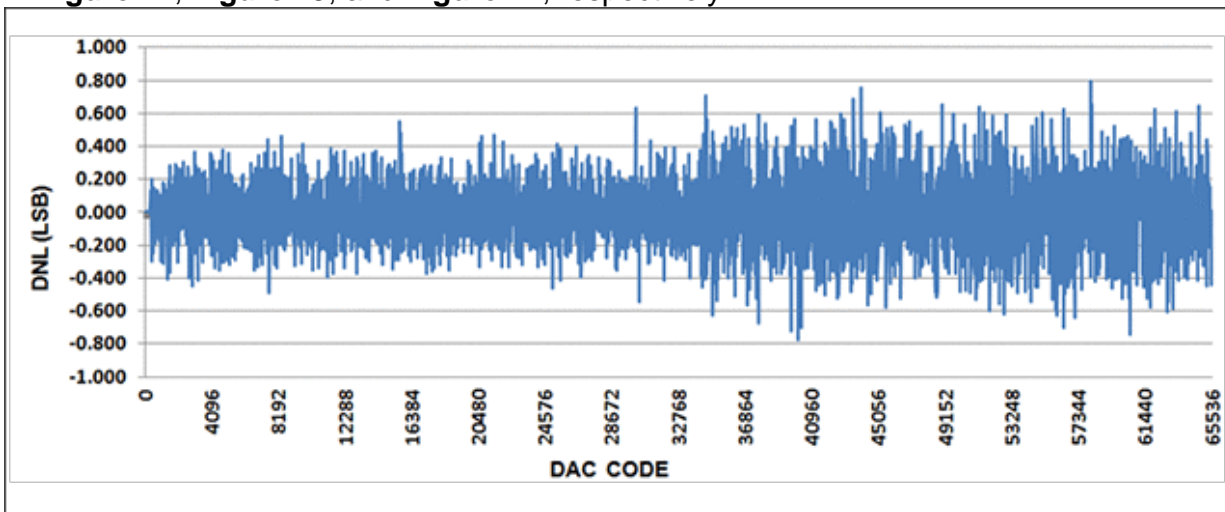

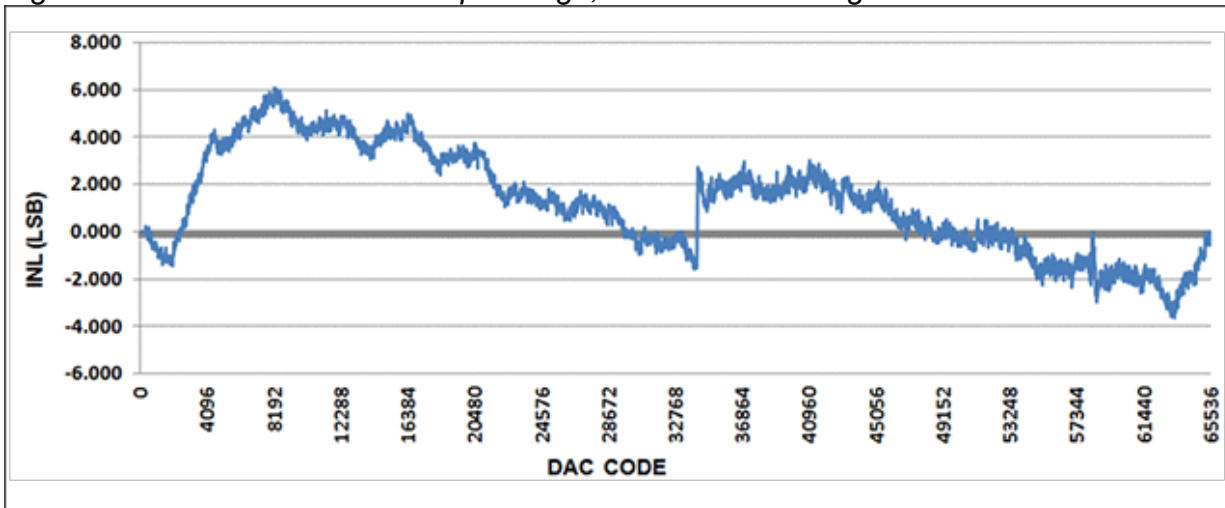Figure 12. DNL for 0 to 20mA output range, with 20% overrange.

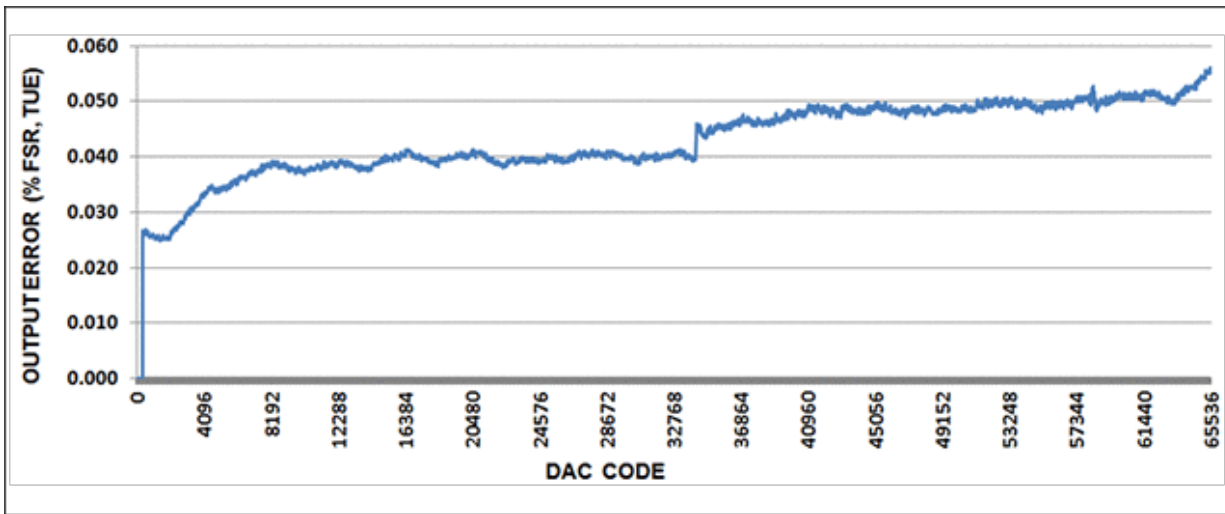Figure 13. INL for 0 to 20mA output range, with 20% overrange.

Figure 14. Output error for 0 to 20mA output range, with 20% overrange.

All Design Files

[Download All Design Files](#)
Hardware Files

[Schematic](#)
[Bill of materials (BOM)](#)
[PCB layout](#)
[PCB Gerber](#)
[PCB CAD (PADS 9.0)](#)
Firmware Files

[LX9 Platform (Spartan-6)](#)
[ZedBoard Platform (Zynq-7000)](#)

Related Parts

MAX14850	Six-Channel Digital Isolator	Free Samples
MAX15500	Industrial Analog Current/Voltage Output Conditioners	Free Samples
MAX1659	350mA, 16.5V Input, Low-Dropout Linear Regulators	Free Samples
MAX17498B	AC-DC and DC-DC Peak-Current-Mode Converters for Flyback/Boost Applications	Free Samples
MAX5134	Pin-/Software-Compatible, 16-/12-Bit, Voltage-Output DACs	Free Samples
MAX6126	Ultra-High-Precision, Ultra-Low-Noise, Series Voltage Reference	Free Samples

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