Low Power 3D Magnetic Sensor with I²C Interface

3D Magnetic Sensor with I²C Interface

TLV493D-A1B6 3D Magnetic Sensor

3D Magnetic Sensor

User's Manual

V 1.02, 2016-05

Sense & Control

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1 Product Description

1.1 Overview

The 3D magnetic sensor TLV493D-A1B6 detects the magnetic flux density in three directions; x, y and z. The magnetic flux density in the z-direction (Bz) is detected by a lateral-Hall plate parallel to the surface of the chip. The magnetic flux density in the x- and y-direction (Bx and By) are detected by vertical-Hall plates perpendicular to the surface of the chip.

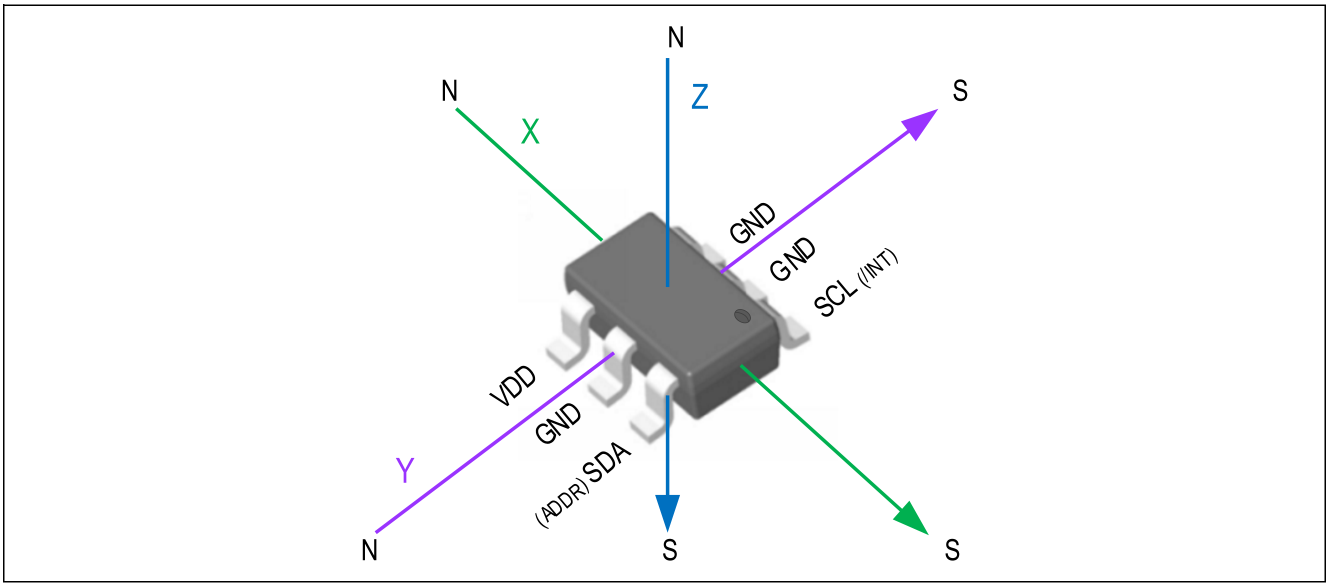

Figure 1 TLV493D-A1B6 measured magnetic field strength directions

With the measured magnetic flux density in the three directions, the TLV493D-A1B6 allows to map the position of a magnet in a 3D space. The magnet is usually glued (e.g. with silicone adhesives) in the moving part in a system. The magnet material (strength) and geometry (shape) will determine the maximum distance that can be measured in each of the three directions as well as the sensibility to position changes.

1.2 Features

- 3D magnetic flux density sensing
- Very low power consumption = 10µA during operation (10Hz, typ)
- Power down mode with 7nA power consumption
- Digtial output via 2-wire standard I^2C interface up to 1MBit/sec
- 12 bit data resolution for each measurement direction
- Bx, By and Bz linear field measurement up to +-130mT
- Excellent matching of X/Y measurement for accurate angle sensing
- Variable update frequencies and power modes (configurable during operation)
- Supply voltage range = 2.8V...3.5V
- Temperature range Tj = -40°C...125°C
- Small, industrial 6 pin TSOP package

- Triggering by external µC possible
- Interrupt signal available to wake up a microcontroller
- Temperature measurement

1.3 Application

The 3D magnetic sensor TLV493D-A1B6 measures three-dimensional, linear and and rotation movements. Therefore the TLV493D-A1B6 is suitable for appliactions such as joysticks, control elements (white goods, multifunction knops, human-machine interfaces or HMI), electric meters (anti tampering) and any other application that requires accurate angular measurements. Due to its low power consumption concept it can also address applications where power consumption is critical.

2 Functional Description

Description of the Block diagram and its functions.

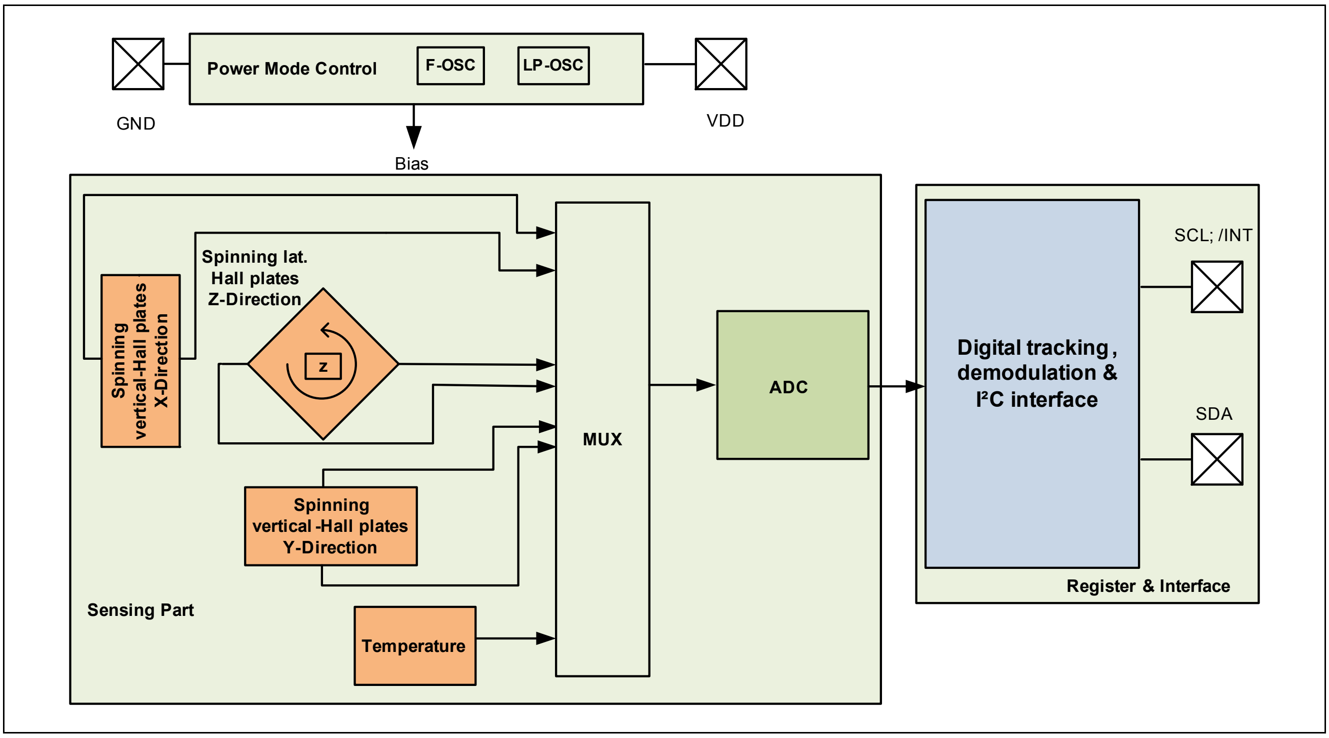

Figure 2 Block Diagram

The IC consists of three main function units containing following building blocks:

- The power mode control system, containing a low-power oscillator, basic biasing, accurate reset, undervoltage detection and a fast oscillator.
- The sensing part, containing the HALL biasing, HALL probes with multiplexers and successive tracking ADC. Furthermore a temperature sensor is implemented.
- The I^2C interface, containing the register file and I/O pads

2.1 Power mode control

The power mode control provides the power distribution in the IC, a power-on reset function and a specialized low-power oscillator as clock source. Additionally it is handling the start-up behavior.

- On start-up this unit:
  - activates the biasing, provides an accurate reset detector and fast oscillator
  - interprets the applied voltage level on ADDR pin as logical “0” or “1”. This determines one of two possible I^2C bus addresses to access the sensor. See also **Chapter 4.2**.
  - sensor enters power down mode (configured via I^2C interface)

Note: After supplying the sensor (= power up) the sensor enters the mode power down by default.

- After re-configuration to one of the operating modes a measurement cycle is performed regularly containing of:
  - starts the internal biasing, checks for reset condition and provides the fast oscillator

- provides the HALL biasing
- the measurement of the three HALL probe channels sequentially incl. temperature (default = activated)
- and enters the configured mode again

In any case functions are only executed if the supply voltage is high enough, otherwise the reset circuit will halt the state machine until the level is reached and continues its operation afterwards. The functions are also restarted if a reset event occurs in between.

2.2 Sensing part

Performs the measurements of the magnetic field in X, Y and Z direction. Each X, Y and Z-HALL probe is connected sequentially to a multiplexer, which is then connected to an Analog to Digital Converter (ADC). Optional, the temperature is determined as well after the three HALL channels. The current consumption decreases by -25% when temperature measurement is deactivated.

3 Measurements

In the next chapters calculation of the magnetic flux and temperatures with 12 bit and 8 bit resolution are shown.

3.1 Calculation of the magnetic flux

The TLV493D-A1B6 provides the Bx, By and Bz signed values based on Hall probes. The magnetic flux values can be found in the registers as documented in the registers chapter. A generic example is calculated next.

Table 1 Conversion table for 12Bit

	MSB	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	LSB
	-2048	1024	512	256	128	64	32	16	8	4	2	1
e.g.	1	1	1	1	0	0	0	0	1	1	1	1

Example for 12Bit read out: 1111 0000 1111: -2048 + 1024 + 512 + 256 + 0 + 0 + 0 + 0 + 8 + 4 + 2 +1 = -241 LSB

Calculation to mT: -241 LSB * 0.098 mT/LSB = -23.6mT

Table 2 Conversion table for 8Bit

	MSB	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5
	-128	64	32	16	8	4	2	1
e.g.	0	1	0	1	1	1	0	1

Example for 8-Bit read out: 0101 1101: 0 + 64 + 0 + 16 + 8 + 4 + 0 + 1 = 93 LSB

Calculation to mT: 93 LSB * 1.56 mT/LSB = 145.1 mT

3.2 Calculation of the temperature

The TLV493D-A1B6 provides the temperature based on a bandgap circuit (reference voltage against ptat junction voltage). The temperature value can be found in two registers as documented in the registers chapter (register 3_H for the MSBs, register 6_H for the LSBs).

The temperature is a signed value. A 340digit offset has to be subtracted as documented in the **TLV493D-A1B6 Data Sheet**. Two examples with 12 and 8 bits follow

Table 3 Conversion table for 12Bit

	MSB	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	LSB
	-2048	1024	512	256	128	64	32	16	8	4	2	1
e.g.	0	0	0	1	0	1	1	0	1	0	1	0

Example for 12Bit read out: 0001 0110 1010: 0 + 0 + 0 + 256 + 0 + 64 + 32 + 0 + 8 + 0 + 2 + 0 = 362 LSB

Offset compensation: 362 LSB - 340 LSB = 22 LSB

Calculation to temperature in degrees Celsius: 22 LSB * 1.1°C/LSB = 24.2°C

4 I²C Interface

The TLV493D-A1B6 uses Inter-Integrated Circuit (I²C) as communication interface with the microcontroller. The I²C interface has two main functions: configure the sensor and receive measurement data. Additionally, I²C also handles the interrupt.

4.1 Interface Description

- The I²C interface requires two pins:
  - A serial clock (SCL) input pin. The clock is generated by the microcontroller.
  - A serial data pin (SDA) for in- & output (open drain). The microcontroller always initiates and concludes the communication.
- Both pins are in open-drain configuration, therefore they usual output is "high". For more details see the application circuit in the **TLV493D-A1B6 Data Sheet**.
- The interface can be accessed in any power mode, even in power down mode, since the internal oscillators do not have to be active.
- The data transmission order is Most-Significant Bit (MSB) first, Last-Significant Bit (LSB) last.
- Data bytes start always with the register address 00_H.
- An acknowladge (ACK) error is indicated as "high" (1_B). No error is indicated at ACK "low" (0_B).
- The values of all three axis (Bx, By, Bz) are stored in separate registers. After a power-on reset these registers will read zero.
- Reset monitoring mechanisms are integrated. Reset levels which only effect the ADC supply during a conversion will lead to an ADC cycle reseting only, and the register values will remain as they are. Deep reset levels detected by the "zero current" reset block which could result in internal flip-flop corruptions will lead into a full reset including all registers (default fuse values to be reloaded) and a power-on cycle will be executed.
- A full reset can be triggered via I²C by sending the address 0x00 to all slaves (sensors). More details are povided on **Chapter 5.6**.
- A two bit frame counter allows to check for a "frozen" sensor functionality (e.g. the power unit did not initiate a measurement cycle or the ADC did not complete a new measurement - which means the frame counter does not get incremented anymore).
- The shortest possible communication (read or write 1 register) requires a start condition, 18 bits transfer and a stop condition. At 400kbit/s this means approximately 50µs.
- A communication reading the top seven registers (from Bx to Temp) requires a start condition, 63 bits transfer and a stop condition. At 400kbit/s this means approximately 165µs.
- A communication writing all four write registers requires a start condition, 36 bits transfer and a stop condition. At 400kbit/s this means approximately 95µs.

The interface conforms to the I²C fast mode specification (400kBit/sec max.) but allows operation up to at least 1 Mbit/sec in case the electrical setup of the bus is lean enough (which means the amount of devices and thus the parasitic load of the bus line is limited to keep rise/fall time conditions small). The allowed max. clock rate above 400kHz has to be defined on demand given a specific electrical setup.

4.2 I²C format description

A I²C communication is always initiated (with a start condition) and concluded (with a stop condition) by the master (microcontroller). During a start or stop condition the SCL line must stay high.

The I²C communication frame consists of the start condition, one addressing byte which corresponds to the slave adress (sensor number), the data transfer bytes (writing to slave or reading from slave) and finally the stop condition. Addressing and data transfer bytes are always followed by an acknowledge (ACK) bit. During the addressing and the data transfer, bit transitions occur with the SCL line at low. If no error occurs during the data transfer, the ACK bit will be driven low. If an error occurs, the ACK bit will be driven high.

- The start condition initiates the communication and consists of a falling edge of the SDA line while SCL stays high. It is the microcontroller that pulls down the SDA line.
- The sensor addressing consists of one byte followed by one ACK bit. The purpose of the addressing is to identify (slave number) the sensor with which the communication should take place. These bits are required independently of whether only one or multiple slaves in bus configuration are connected to the master. The master sends 7 address bits starting with the MSB followed by one read/write bit (read = high, write = low). The slave (sensor) responds with one ACK bit. Every bit in the SDA line is pulled down or up while SCL is low, then SCL is pulled up for a pulse and again down before the SDA line is pulled again down.
- Each data transfer consist of one byte data followed by one ACK bit. If the LSB bit of the sensor addressing byte was a write (low), then the master writes 8 data bits to the slave and the slaves responds with one ACK bit. If the LSB bit of the sensor addressing was a read (high), then the master reads 8 data bits from the slave and the master responds with one ACK bit. Data bytes start always with the register address 00_H and as many bytes will be transfered as the SCL line is generating pulses (following a 9 bit pattern), till the stop condition
- The stop condition concludes the communication and consists of a rising edge of the SDA line while SCL stays high. It is the microcontroller that pulls up the SDA line.

Note: In case an overflow accours at address 9_H (whole bitmap read) the SDA line remains pulled up (no output from the sensor) till the ACK bit, which will also remain high indicating an error (ACK = 1). In case the whole bitmap is written and the master continues sending data, this will be ignored by the sensor, and the ACK will be driven high, indicating an error.

With the described I²C format some overhead used in conventional 7 bit "repeated-start" is avoided, optimizing the TLV493D-A1B6 for fast and power-efficient read out of sensor data. Therefore the master should be implemented to handle the direction switching after the second byte.

The protocol uses a standard 7 bit address followed by data bytes to be sent or received. 12 bit addressing or any sub-addressing is not implemented, so each start condition always begins with writing the address, followed by reading (or writing) the first byte of the bitmap and continues with reading (or writing) the next byte until all bytes are read (or written) or the communication is simply terminated by a stop condition. The basic initiator for the protocol is the falling SDA edge.

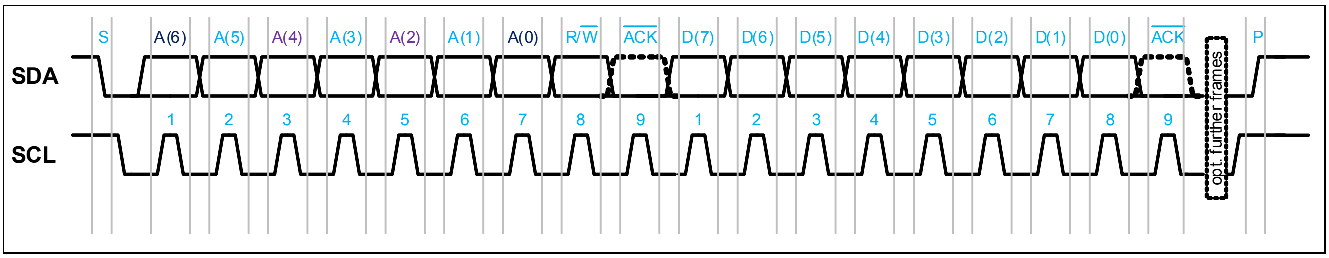

Figure 3 General I²C format

Note: A reset can be triggered with general I^2C address 0x00. After this command the sensor will do an power up sequence. (See ***Chapter 5.1****)*

The default setting after startup for a read operation is shown below for ADDR=1 and ADDR=0. ADDR=1 is defined by Pin SDA at power up to be high according AppCircuit. In order to set ADDR=0 SDA must pulled down to low during power up. To set the address the high or low level must be kept 200us after supplying the sensor.

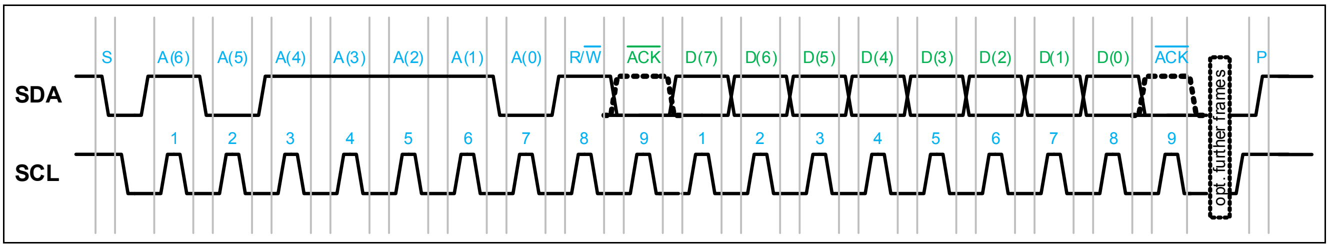

Figure 4 Read example with default setting ADDR=1 (=BD; Write = BC)

For ADDR=1 bit A(6)=1 and A(0)=NOT(Addr) = 0 is used.

After configuration to ADDR=0 following sequence is used.

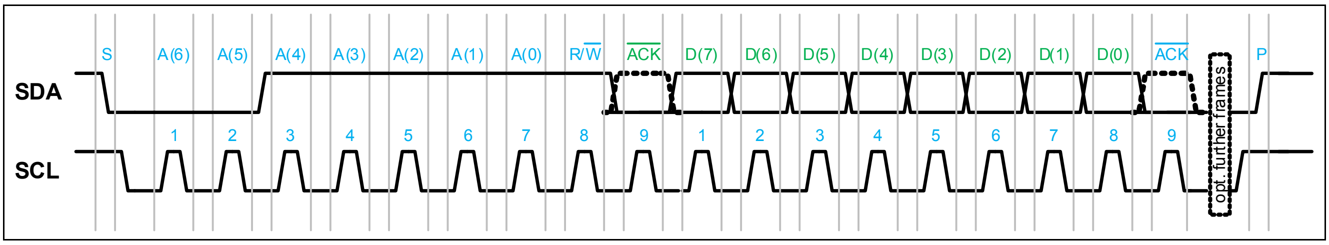

Figure 5 Read example with ADDR=0 (3F; Write = 3E)

For ADDR=0 bit A(6)=0 and A(0)=NOT(Addr) = 1 is used.

Communication examples

An example of a read communication is provided in **Figure 6**. The master generates a start condition followed by the addressing to sensor number ADDR = 1 (1011110_B) and the read bit (1_B). The slave generates an ACK for the addressing and outputs the first register (register 0_H), which corresponds to the Bx value (1011110_B which equals 145.1mT). The master generates an ACK once the register is read. The slave outputs the second register (register 1_H), which corresponds to the By value (11111001_B which equals -10.92mT). The masters generates an ACK and since no more information is required the master generates the stop condition.

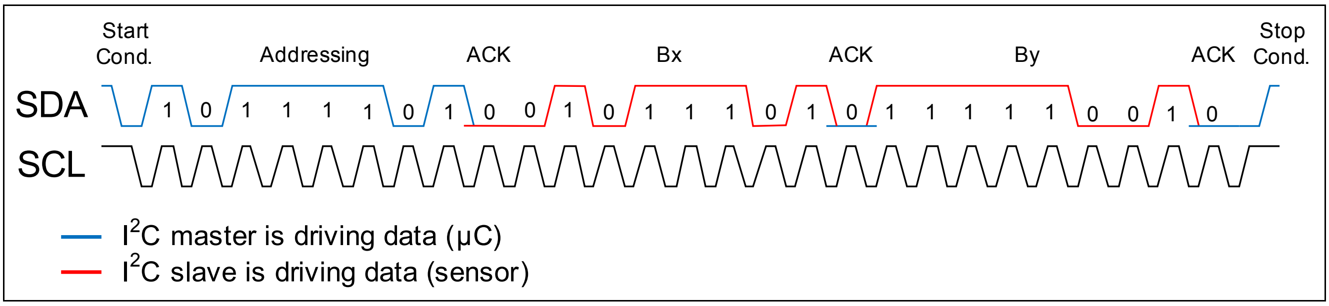

Figure 6 I²C read communication example

An example of a typical write communication at start-up is provided in **Figure 7**. The TLV493D-A1B6 is by default configured in power down and no Bx, By, Bz values are measured. To start Bx, By, Bz conversions at a given update rate the configuration has to be changed to low power mode for example.

In this case after the master generates a start condition followed by the sensor number ADDR = 1 (1011110_B) and a write bit (0_B). The slaves generates an ACK. The master continues the transmission writing 00000000_B at the first writing register (a Reserved register). The slaves generates an ACK. The master writes $0000\ 0101_B$ in the second writing register (configuration register MOD1). The slaves generates an ACK and since no more data need to be written the master finishes the communication with a stop condition.

With this configuration the interrupt pulse bit is enabled (MOD1 register = $xxxx\ x1xx_B$) and the low power mode is enabled (MOD1 register = $xxxx\ xxx1_B$). Every 12ms a Bx, By, Bz conversion will be measured and once the conversion is completed an interrupt pulse will be sent to master. The master can then read the Bx, By and Bz registers.

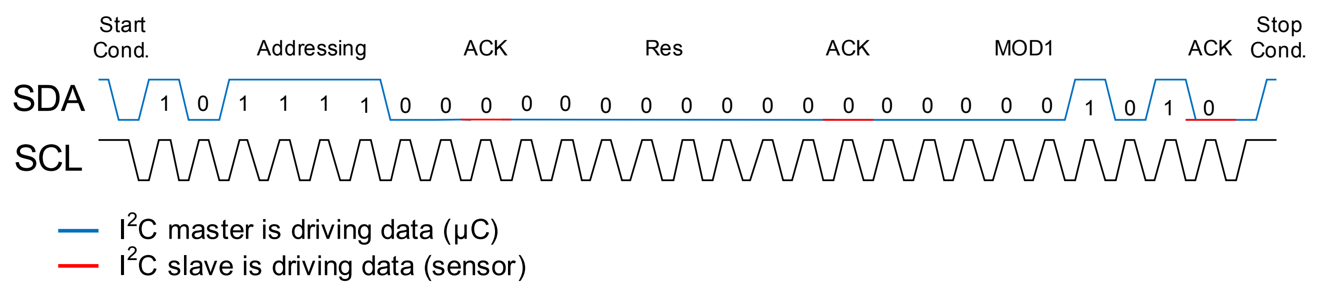

Figure 7 I²C write communication example

4.3 Timing diagrams and access modes

The TLV493D-A1B6 timing requirements are available in the **TLV493D-A1B6 Data Sheet**.

4.3.1 I²C timing

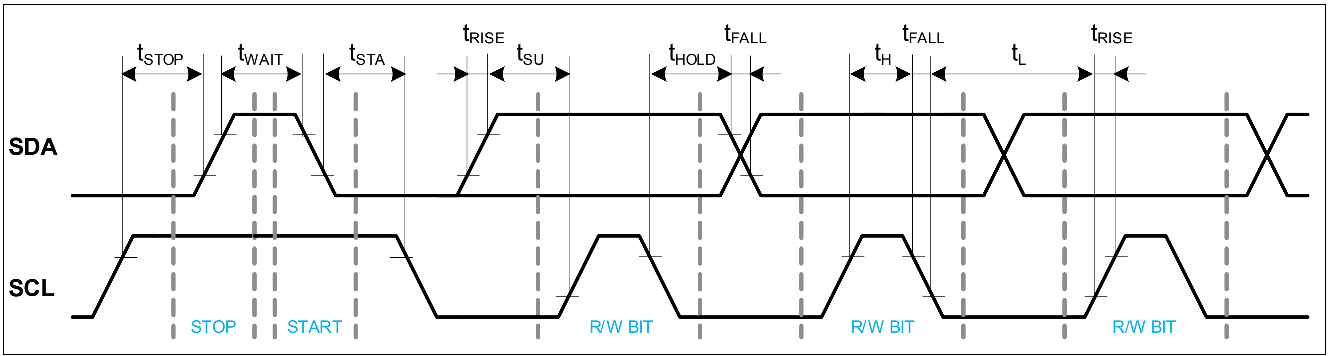

Figure 8 I²C timing diagram

5 Access modes

At power up the TLV493D-A1B6 starts with the factory configuration, in power down mode (default mode). The power down mode allows to access the registers to read (default values) or write (for configuration), but no magnetic field nor temperature values are measured.

To start measurements, one of the following modes has to be configured:

- Fast mode
- Low power mode
- Ultra low power mode
- Master controlled mode (MCM)
- Master controlled low power mode

These modes are described in the next chapters. Be aware that the Fast Mode and the Master Controller Modes are not specified in the **TLV493D-A1B6 Data Sheet**.

5.1 Power Up and Power Down Mode

After power up, the sensor reads out the voltage applied on ADDR pin for 200µs. If the voltage level on ADDR=high than the address is set to “1”. If the voltage level on ADDR = low the address is set to “0”.

SDA and ADDR use the same pin. In case of SDA = low a ZC-Reset may occur and ADDR = 0 will be clocked in.

For a short period of time the power consumption increases to 3.7mA. During this short period all functional blocks are active (but no magnetic measurement nor temperature measurement take place). After this the sensor enters the “power down mode”, and all functional blocks are off.

After that byte 7, 8 & 9 have to be read out at least one time and stored for later use by the user. This is necessary for any write command later on in order not to change the internal configurations accidentally. This means, that the bits transferred at any write command and not used for configuration, needs to be set to the same values as you read them out before, otherwise configuration will be changed (a power down and up will reset the sensor to factory settings again)

For example:

- Read Out Byte 7..9 (factory settings)
- Write Byte 1: configurable are D(0), D(1) & D(2) to set different modes, but not configurable and therefore not to be changed are D(3) .. D(7). Not to change means you have to write back the former read values from Byte 7 D(3) .. D(7) and use them to write for byte 1.

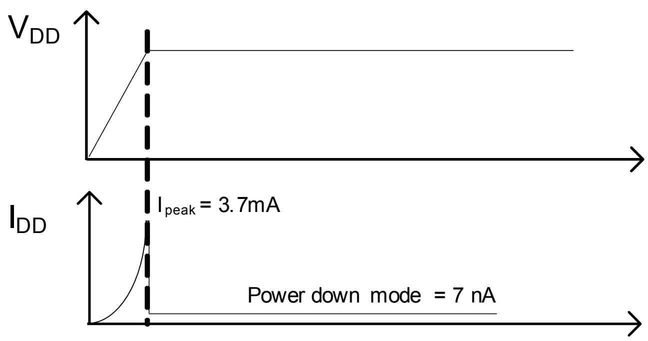

Figure 9 Current consumption during power up

Power Down Mode

Please set in write-register 1_H bit#1=0 (fast = 0) and set bit#0=0 (low=0) to enter power down mode.

5.2 Fast mode (3.3 kHz)

Settings: fastmode=1, lp_mode=0, int_out=1 (byte settings [hex] = 00, x6, xx, xx, keep certain bits)

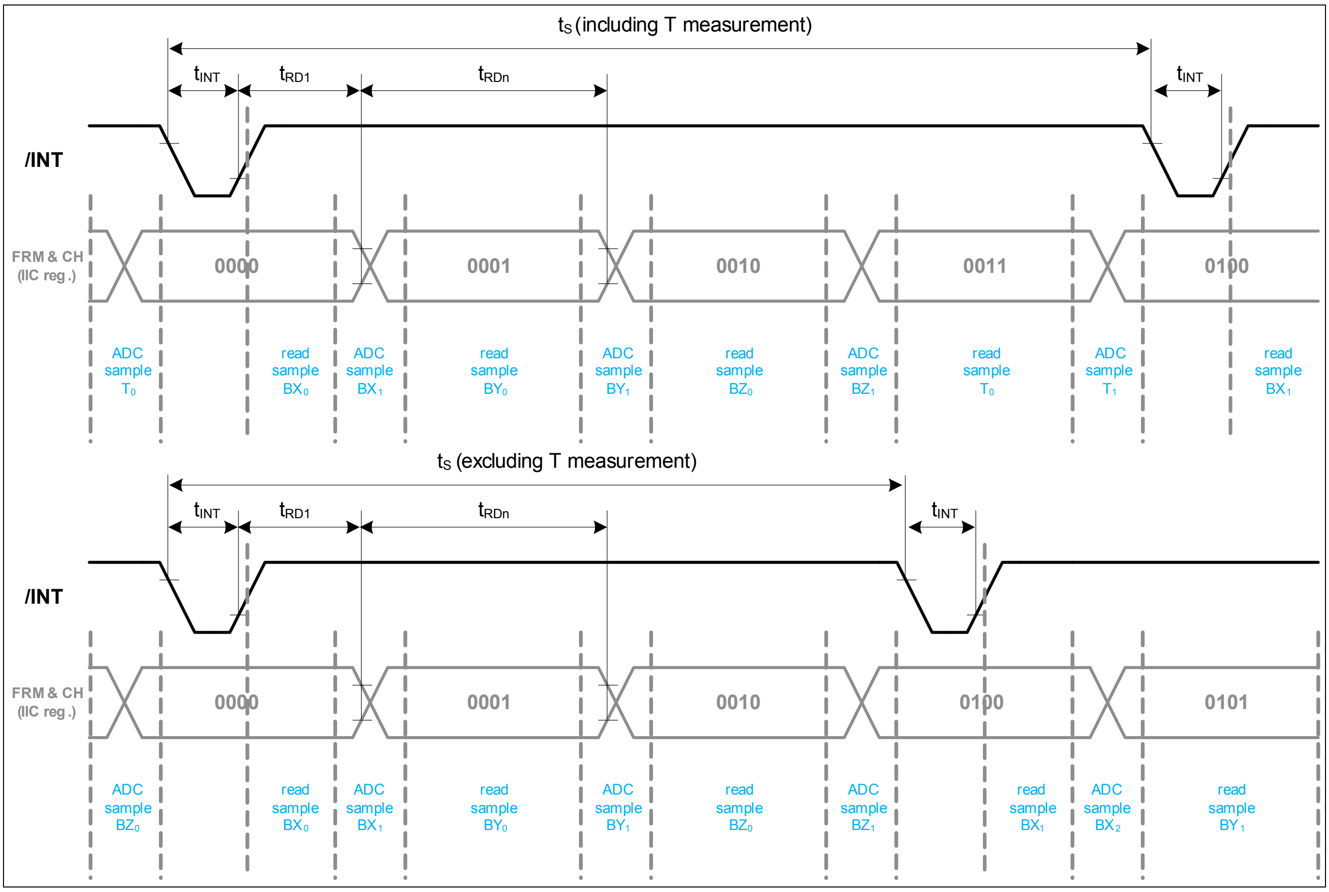

Figure 10 Fast Mode (/w and w/o temp. measurement) in relation to /INT output

It is possible to optimize the readout in a way that the sample of the last conversion can be read while the next conversion is performed. To achieve this, the readout from I^2C has to be done faster than the given time when the next value gets overwritten, including any possible clock variance between sensor and master (µC).

Note: This read mode assumes to read only first three 8 bit values via I^2C after an /INT pulse.

To read out the 8 bit values for Bx, By and Bz the I^2C address write and first byte read needs to be done within tRD1 (minus the w.c. accuracy of the sensor clock and the µC clock) after the rising interrupt clock edge. The next byte needs to be read latest within an additional tRDn timeframe (minus tolerances) and so on. Assuming all 3 values are read directly in one I^2C sequence, the time for readout of the first byte is the most critical (as two I^2C frames are required), reading the remaining bytes should not be a timing issue as here nevertheless more time is available.

Note: Thus, this mode requires a non-standard 1MHz I^2C clock to be used to read the data fast enough.

Table 4 Interface and Timing

Parameter	Symbol	min	typ	max	Unit	Note/Condition
Time window to read first value	tRD1	–	32.8	–	µs	read after rising /INT edge
Time window to read next value	tRDn	–	33.6	–	µs	consecutive reads

5.3 Low Power mode (100 Hz)

Settings: fastmode=0, lp_mode=1, int_out=1 (byte settings [hex]: 00, x5, xx, 4x, keep certain bits)

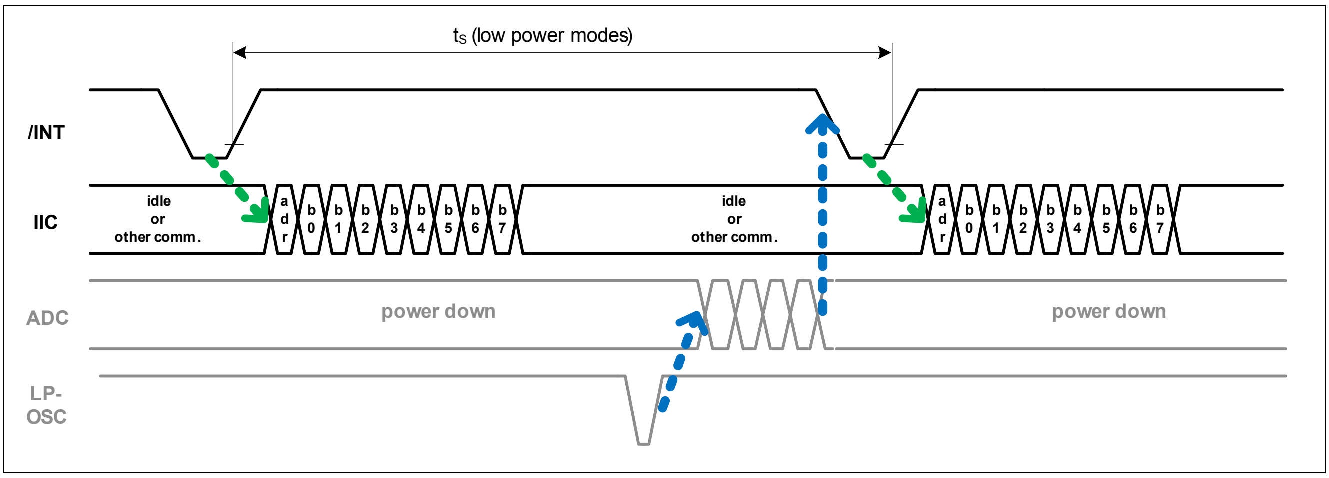

Figure 11 Synchronous, low-power I²C readout using an /INT wake-up pulse

In this low-power mode the sensor goes into power-down mode until it wakes up by itself to perform the next conversion. After the conversion the interrupt line will be pulled (if activated). This means for the low power modes the time window to read out all registers after the rising edge of the /INT pulse is equal one over the sample rate of this low power mode minus the conversion time.

5.3.1 Ultra Low Power Mode (10 Hz)

Settings: fastmode=0, lp_mode=1, int_out=1 (byte settings [hex]: 00, x5, xx, 0x, keep certain bits)

In this mode an excellent combination of ultra low power consumption and internal regular wake up function is reached. The basic function is equal to Low Power Mode, but Low Power Mode has about 8 times higher current consumption than Ultra Low Power Mode. As well the interrupt is available. If an even lower power consumption is needed please refer to **Chapter 5.4.1**.

5.4 Master-controlled Mode (variable to f_{max} = 3.3 kHz)

Settings: fastmode=1, lp_mode=1, int_out=0/1 (byte settings: 00, x7, xx, xx, keep certain bits)

- The fast oscillator is constantly enabled
- One measurement cycle is performed and /INT is pulsed.
- Measurement data is available for read out in the registers.
- The sensor is waiting for read-out and no other measurements are done.
- As soon as the master performs a read-out a new measurement cycle is internally started by the sensor and new values will be stored in the registers. If no further read out takes place no new measurement cycle is initiated.

In the simplest case, periodic read-out of I²C causes a re-run of a new measurement cycle. It only needs to be ensured that the read-out time is larger than the time for the I²C read frame plus the sensor conversion time.

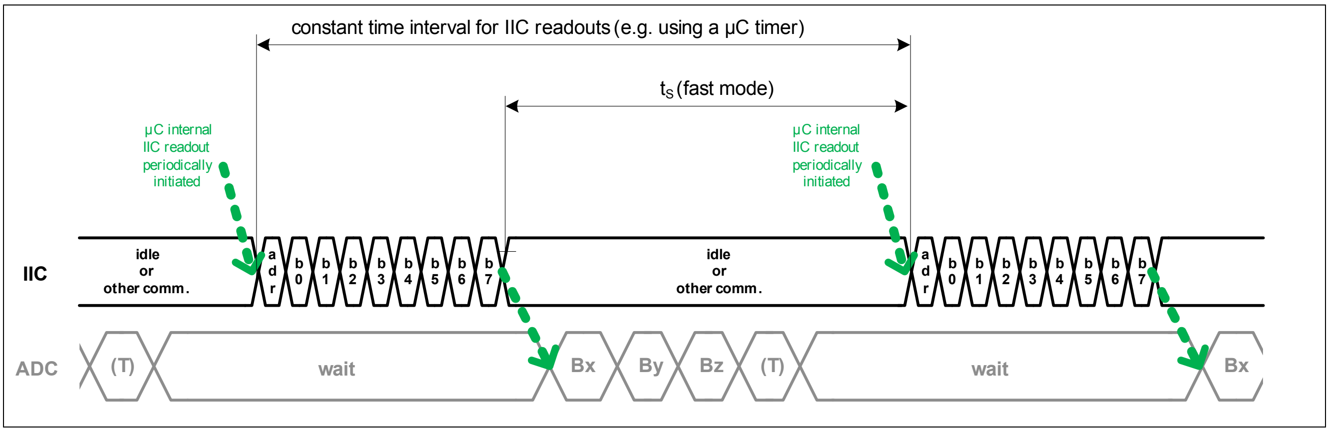

Figure 12 Synchronous, fast I²C access using a periodic I²C read-out

If possible, the /INT output should be activated and used in this mode as well. This will provide the fastest and safest way to read out all axis with a 12bit resolution value, as to be shown next.

This allows a read-out of the sensor to the master (µC) using an interrupt service routine. The sample rate is now basically determined by the ADC conversion time plus the I²C readout time only and fully avoids the read of inconsistent values. The possible sample rate for this mode a regular 400kHz I²C speed is given in the specification section.

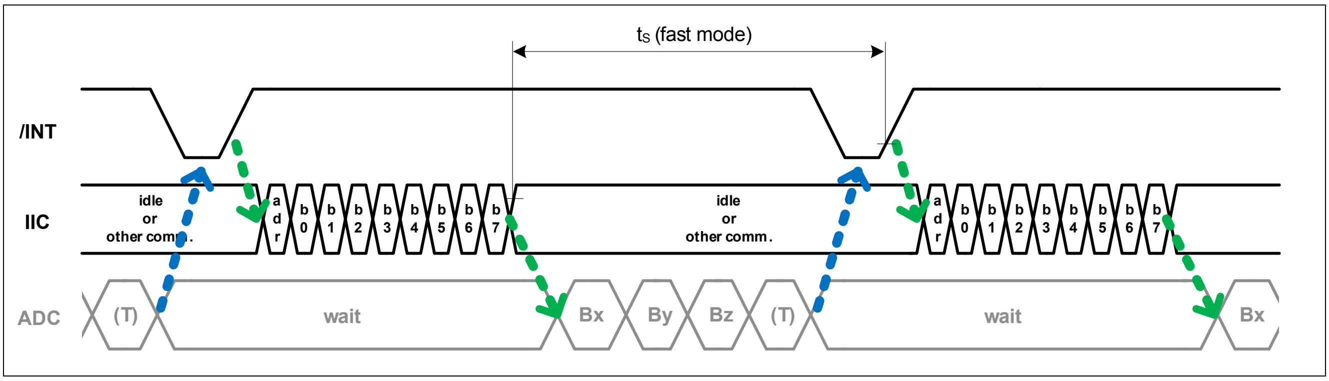

Figure 13 Synchronous, fast I²C access using an /INT trigger for I²C readout

Please be aware that this modes does not switch off the internal biasing and oscillator, it should therefore not be used for low-power operation with large time intervals between measurements. See **Chapter 5.4.1**

5.4.1 User defined configuration (Master controlled Low Power Mode)

If even lower current consumptions compared to “Ultra Low Power Mode” are required this “User defined Configuration” can be used. For this, it is recommended to switch the sensor into “Power Down Mode” for the time interval in which the sensor is not used (fastmode=0, lp_mode=0) and shall only be re-activated for a new measurement and readout (fastmode=1, lp_mode=1) if necessary.

Following example can be used:

1. *Set sensor via I²C in master-controlled mode with /INT (fastmode=1, lp_mode=1, int_out=1)*
2. *Wait until INT/ =0 --> one measurement cycle was done*
3. *Set sensor via I²C in Power Down Mode (fastmode=0, lp_mode=0) --> IDD goes down to power down current consumption*
4. *Read out bytes*
5. *Wait for x ms*
6. *Goto 1*

By using this example the sensor is toggled between two different modes by the I²C interface. The longer the waiting period (step 5) is, the lower is the current consumption. The I²C can always accessed. For example, for an update rate of f = 0.016Hz (update every 60s) the **typical, average current consumption is only 20nA**. See the **TLV493D-A1B6 Data Sheet** for the corresponding current consumption in each mode (sample rate).

This principle described above can be adapted in order to toggle between any other modes.

5.5 ADC hang up in Master Controlled or Fast Mode

Problem Description

In the Master Controlled Mode (MCM) or the Fast Mode (FM) the ADC conversion may hang up. A hang up can be detected by:

- Frame Counter (FRM) counter stucks and does not increment anymore.

Corrective Action

Operating Mode, Sensor used in polling mode[1] / master controlled mode

1. Detect a non incrementing frame counter.
2. Send general address 0x00 to reset the sensor (see also power-up/reset behaviour in product data sheet).
3. Re-configure to Master controlled Mode.

or Operating Mode, Sensor used in Interrupt mode (Fast or Master controlled Mode)

1. Use a system watchdog to detect a missing interrupt.
2. Optional: detect a non incrementing frame counter.
3. Send general address 0x00 to reset the sensor (see also power-up/reset behaviour in product data sheet).
4. Re-configure to desired Fast or Master controlled Mode.

1) polling:= no /Int is issued, uC reads out sensor in fixed periods

5.6 Power supply considerations

The power supply and its circuitries have to be designed to ensure a stable start-up and sensor initialisation as well as a stable operation for correct communication. The sensor can be supplied by the same supply used by the microcontroller or by an alternative supply. The usage of a microcontroller ouput pin is considered an alternative power supply. The following considerations must be covered in any case:

- The bus pins must not have a higher voltage than the supply pins.
- The supply has to cope with the specified DC currents of the sensor and AC current peaks form digital logic operation (from bus interface and from internal sensor logic).
- In-rush current of the supply buffer capacitor must be considered by dimensioning of the power supply.
- The sensor must not be supplied by a voltage higher than 3.5V, which would reduce the operating lifetime or even cause an immediate damage.
- The sensor does not have any internal overvoltage protection.
- The supply power-up ramp has to be as smooth and steady as possible, as no classic reset circuitry is used.
- The sensor does not provide a reverse voltage protection.

5.6.1 General reset

In case of wrong initialization or any other undesired event, it is possible to trigger a general reset. A general reset can also be used to do reconfigure the address.

A general reset is trigged by calling the address 0x00 in the I2C interface. This generates an internal reset, refreshes the fuse register settings and re-reads the SDA/ADR line to initialize the I2C bus address. The SDA state should be keep for at least 200µs after the reset to ensure a proper initialization with the right bus address.

The general reset can also be used after power-on to improve system robustness in case of unstable power supplies.

6 Bus configuration with multiple sensors

It is possible to connect up to eight slaves (sensors) to a master in a bus configuration. To slave addresses are configured sequentially at start-up. Each slave requires an exclusive supply line, therefore the master must provide enough I/O pins capable of driving up to 5mA DC in each line. Two examples with two and eight slaves are presented next.

Configuration with two slaves

Slave #0 is powered up together with the whole system start up, while slave #1 remains powered down. Within the first 200µs after the power up, slave #0 reads the voltage applied on SDA / ADDR pin. If the voltage level on ADDR is high, the address is set to “1” (default case with open drain configuration). If the voltage level on ADDR is low the adress is set to “0”. This configuration remains fixed till the next power down or reset.

Once the 200µs have transcurred, the master powers up slave #1 with one of the I/O lines. The master drives the SDA / ADDR pin to the opposite level at which slave #0 was configured. After 200µs slave #1 is also configured.

Once the slaves are configured, the master can access to read or write any slave by addressing them accordingly to **Table 5**.

Table 5 Addressing with multiple slaves

Slave	SDA / ADDR pin at power-up	Read		Write	
		Bin	Hex	Bin	Hex
0	high (1)	1011 110 1	BD	1011 110 0	BC
1	low (0)	0011 111 1	3F	0011 111 0	3E

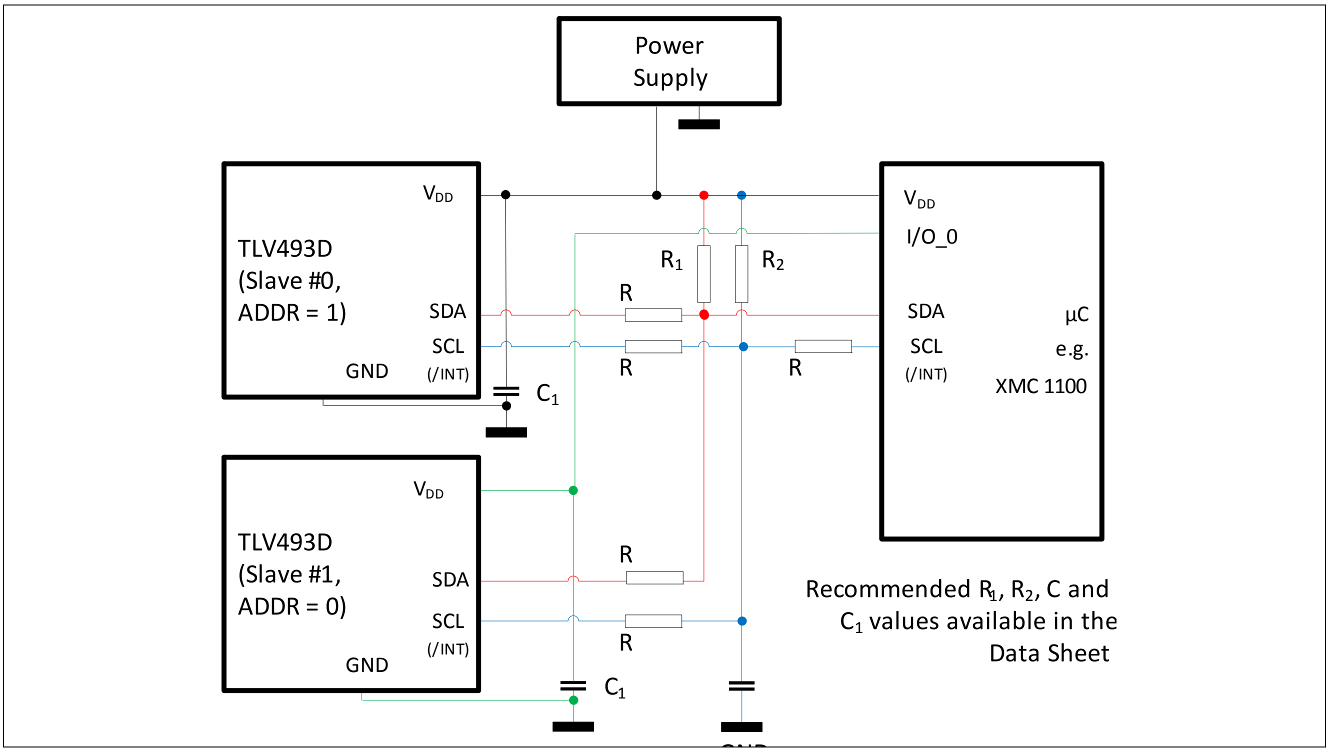

Figure 14 Application circuit for bus configuration with two slaves

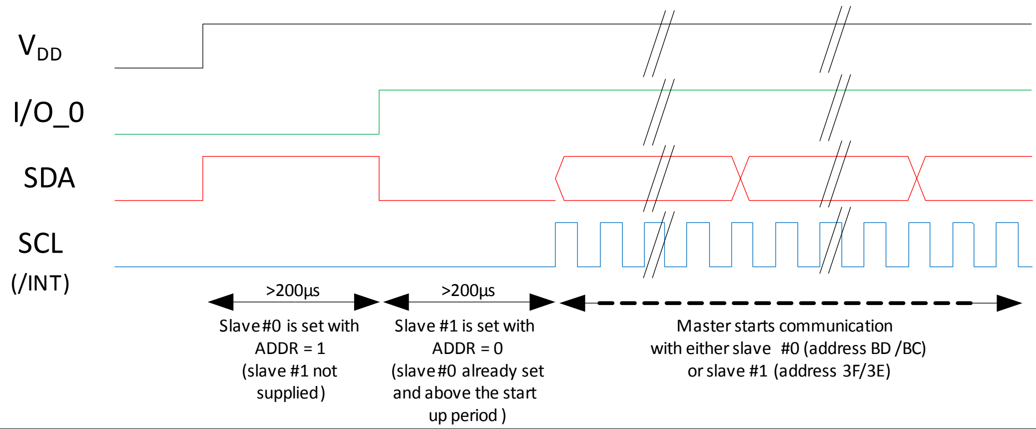

Figure 15 Start-up sequence and timing for bus configuration with two slaves

Configuration with more than two slaves (e.g. eight)

Additionally to the SDA / ADDR pin level to configure the slave number, there are two bits (IICAddr) in the write register MOD1 that allow to set an address. Therefore combining the SDA / ADDR pin levels with the two bits up to eigth slaves can be configured at start up.

In this case the Vdd line plus seven I/O lines will be required to supply the total eight slaves. Slave #0 will be set to ADDR = 1 within the 200µs if SDA / ADDR pin is set to high. Once this is done the IICAddr bits have to be changed from the default "00" to "11". The default address has now been changed from the default 0xBD for read and 0xBC for write to 0x95 for read and 0x94 for write.

Next the I/O_0 line can be driven high to supply slave #1. Setting the SDA / ADDR pin high the default address is set to 0xBD for read and 0xBC for write. After 200µs the address will be changed to 0x9D and 0x9C respectively by writing the IICAddr bits to "10".

The slave #2 is now powered up with the I/O_1 line. SDA / ADDR pin is high for 200µs. The default addresses 0xBD and 0xBC will be changed to 0xB5 and 0xB4 by writing the IICAddr bits to "01". The slave #3 is powered up with the I/O_2 line. SDA / ADDR pin remains high for 200µs. For slave #3 de IICAddr bits remain "00", therefore no need to configure them via I^2C.

For the slaves #4, #5, #6 and #7 the same process described above will be carried, with just one difference, the SDA / ADDR pin will be driven low. Now each of the eight slaves has a specific address (summarized in **Table 6**). The data transfer to any slave will start when the master addresses the desired slave number.

Table 6 Addressing with multiple slaves

Slave	SDA / ADDR pin at power-up	IICAddr bits (Bin)		Read (Bus)		Write (Bus)	
		Default	Bus	Bin	Hex	Bin	Hex
0	high	00	11	1001 010 1	95	1001 010 0	94
1	high	00	10	1001 110 1	9D	1001 110 0	9C
2	high	00	01	1011 010 1	B5	1011 010 0	B4
3	high	00	00	1011 110 1	BD	1011 110 0	BC
4	low	00	11	0001 011 1	17	0001 011 0	16
5	low	00	10	0001 111 1	1F	0001 111 0	1E
6	low	00	01	0011 011 1	37	0011 011 0	36
7	low	00	00	0011 111 1	3F	0011 111 0	3E

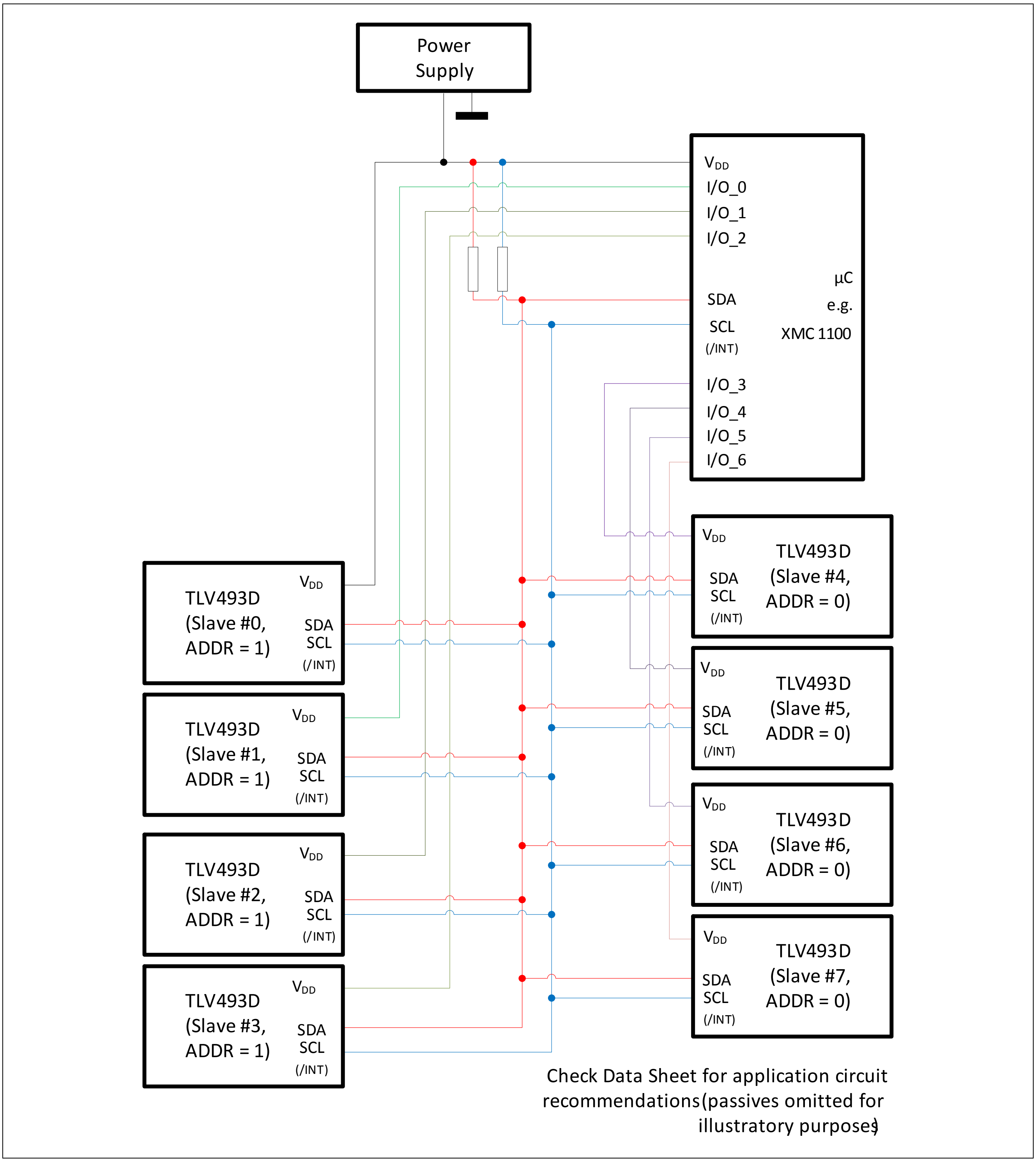

Figure 16 Application circuit for bus configuration with eight slaves

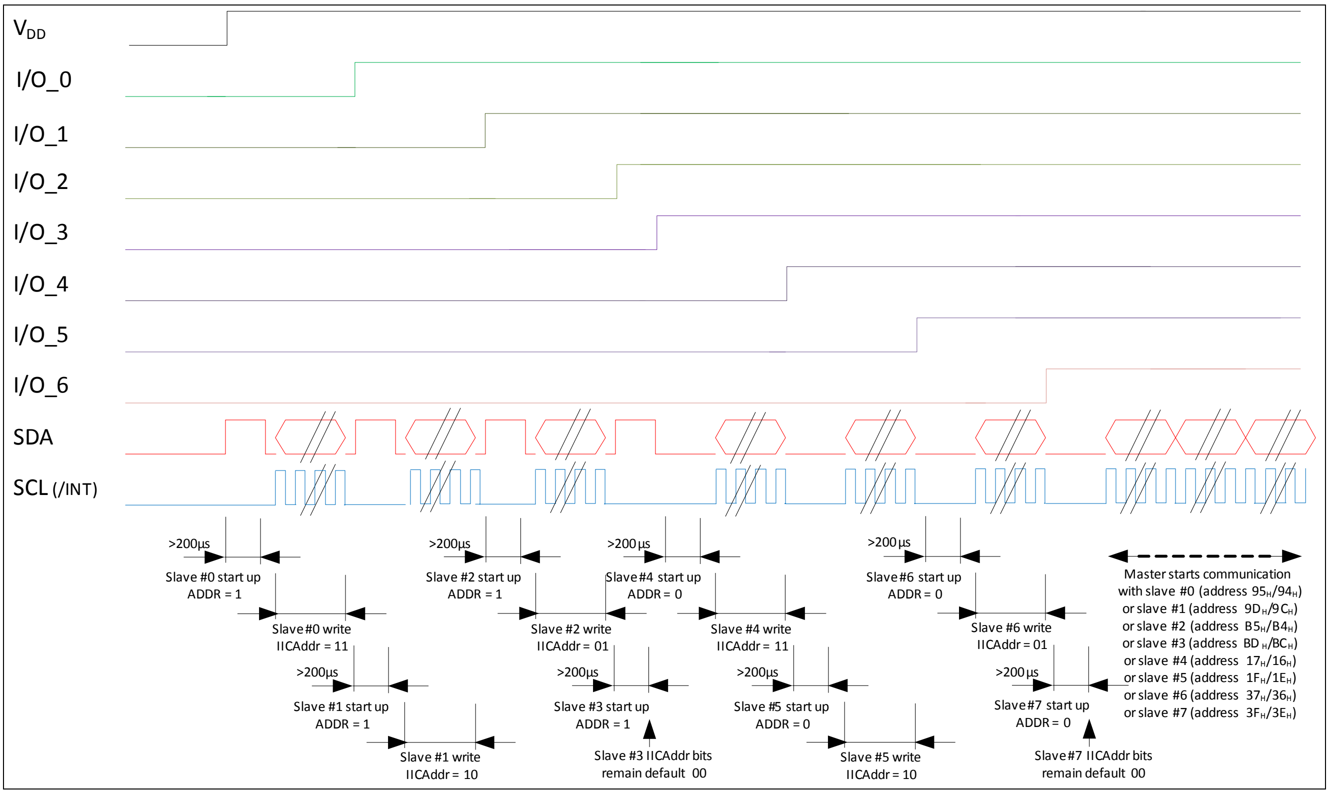

Figure 17 Start-up sequence and timing for bus configuration with eight slaves

Note: it is also possible to configure two slaves by changing the IICAddr bit in the write register MOD1 indepedently of the SDA / ADDR pin at start-up.

7 I²C Registers

The TLV493D-A1B6 includes several registers that can be accessed via Inter-Integrated Circuit interface (I^2C) to read data as well as to write and configure settings. There are ten read registers and four write registers.

7.1 Registers overview

A bitmap overview is presented in **Figure 18**: green bits contain measurement data, orange bits configuration parameters (e.g. power mode) and grey bits are relevant for diagnosis.

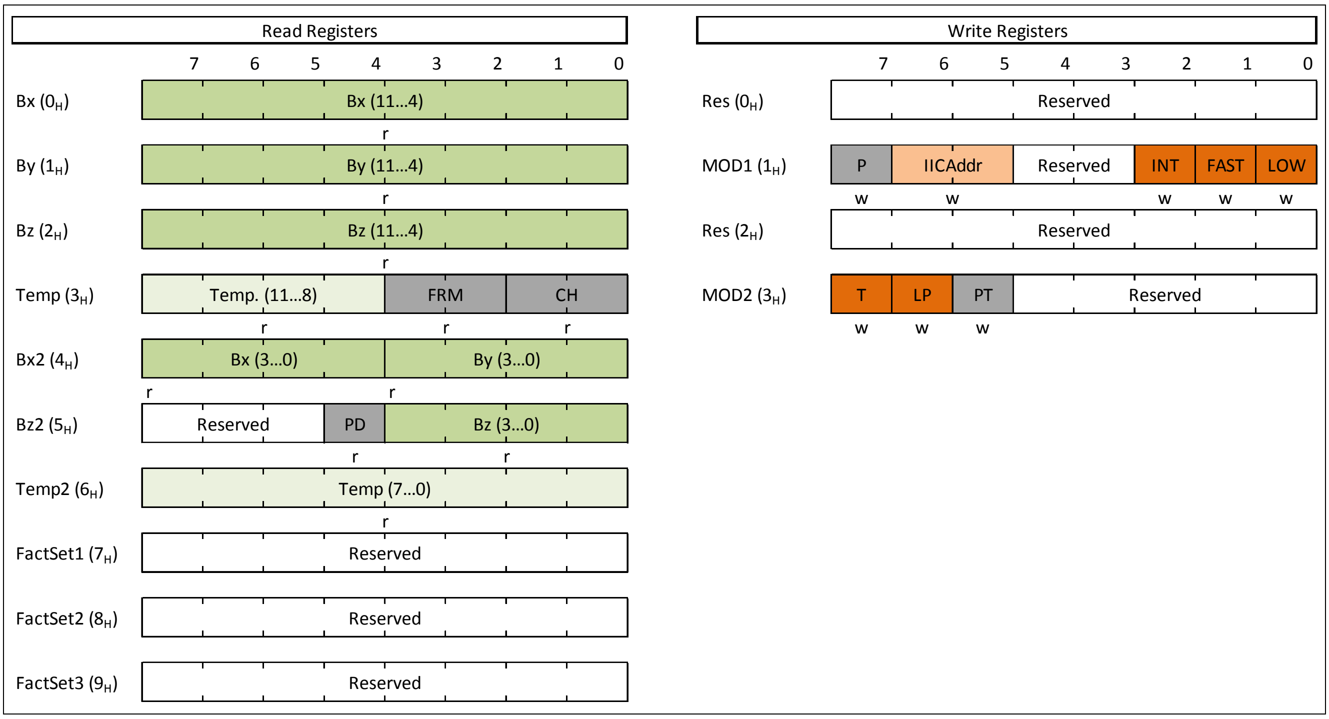

Figure 18 Bitmap

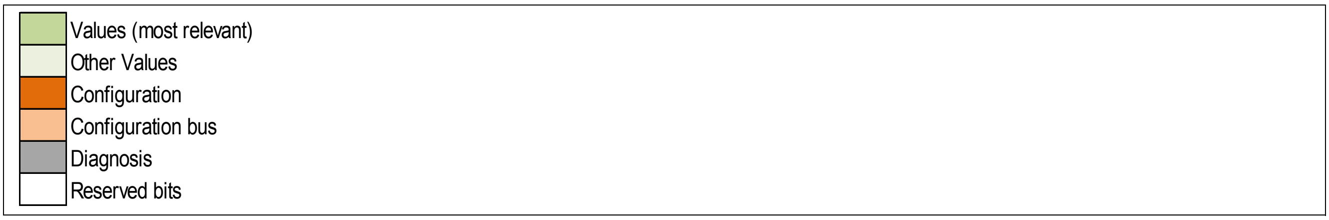

Figure 19 Colour legend for the Bitmap

7.2 Bit Types

The TLV493D-A1B6 contains read bits, write bits and reserved bits.

Table 7 Bit Types

Abbreviation	Function	Description
r	Read	Read only bits
w	Write	Read and write bits for configuration
res	Reserved	Bits that must keep the default values (read prior to write required)

7.2.1 Read Registers

The I²C registers can be read at any time, starting always from address 0_H and as long as the master generates a clock signal (SCL). It is recommended to use the sensor interrupt to read data after an interrupt pulse. This avoids reading inconsistent values, especially when running the fast mode. Additionally, several flags can be checked to ensure the data values are consistent and the ADC was not running at the time of readout.

7.2.1.1 Register Descriptions

Bx register

Bx	**Offset**	**Reset Value**
Bx value register	**0_H**	**00_H**

7 ... 0
Bx (11...4)
r

Field	Bits	Type	Description
Bx	7:0	r	**Bx Value** Signed value from the vertical HALL probe in the x-direction of the magnetic flux. Contains the eight Most Significant bits (bits 11...4). Reset: 00_H

By register

By	**Offset**	**Reset Value**
By value register	**1_H**	**00_H**

7 ... 0
By (11...4)
r

Field	Bits	Type	Description
By	7:0	r	**By Value** Signed value from the vertical HALL probe in the y-direction of the magnetic flux. Contains the eight Most Significant bits (bits 11...4). Reset: 00_H

Bz register

Bz	Offset	Reset Value
Bz value register	2_H	00_H

7 … 0
Bz (11…4)
r

Field	Bits	Type	Description
Bz	7:0	r	**Bz Value** Signed value from the lateral HALL probe in the z-direction of the magnetic flux. Contains the eight Most Significant bits (bits 11...4). Reset: 00_H

Temp register

Temp	Offset	Reset Value
Temperature, counter, channel register	3_H	00_H

7 … 4	3 … 2	1 … 0
Temp (11…8)	**FRM**	**CH**
r	r	r

Field	Bits	Type	Description
Temp	7:4	r	**Temperature Value** Signed temperature value. Below or above the specified operating temperature range non-linearities may occur. If temperature measurement is deactivated during operation, the last value remains in the register. Reset: 0_H
FRM	3:2	r	**Frame Counter** Increments at every update rate, once a X/Y/Z/T conversion is completed. The new Bx, By, Bz and Temperature values have been stored in the registers. Note: if the temperature measurement is disabled, FRM increases as soon as the Z conversion is completed. Reset: 00_B

Field	Bits	Type	Description
CH	1:0	r	**Channel** Must be “00” at readout to ensure X/Y/Z/T come from the same conversion. Else, conversion is running. If “00” no conversion (internal power down) or x-direction conversion started (but value not yet stored in the register) If “01” y-direction conversion ongoing If “10” z-direction conversion ongoing If “11” temperature conversion (if temp. disabled, no If temperature measurement is disabled, no “11” combination possible. The MUX uses the CH bits to select the X/Y/Z/T channel. Note: PD has also to be “1” to indicate a conversion is completed. Reset: 00_B

Bx2 register

Bx2	**Offset**	**Reset Value**
Bx value register	$\mathbf{4_H}$	$\mathbf{00_H}$

7 … 4	3 … 0
Bx (3…0)	**By** (3…0)
r	r

Field	Bits	Type	Description
Bx	7:4	r	**Bx Value** Value from the vertical HALL probe in the x-direction of the magnetic flux. Contains the four Less Significant Bits (bits 3...0). Reset: 0_H
By	3:0	r	**By Value** Value from the vertical HALL probe in the y-direction of the magnetic flux. Contains the four Less Significant Bits (bits 3...0). Reset: 0_H

Bz2 register

Bz2	**Offset**	**Reset Value**
Bz value register	**5_H**	**Device specific**

7 ... 5	4	3 ... 0
Reserved	**PD**	**Bz** (3...0)
	r	r

Field	Bits	Type	Description
PD	4	r	**Power-down flag** Must be "0" at readout. If "0", Bx, By, Bz and Temp conversion completed. If "1" Bx, By, Bz and Temp conversion running. If temperature measurement is disabled, flag toggles after Bz conversion. Reset: 0_B
Bz	3:0	r	**Bz Value** Value from the lateral HALL probe in the z-direction of the magnetic flux. Contains the four Less Significant Bits (bits 3...0). Reset: 0_H

Temp2 register

Temp2	**Offset**	**Reset Value**
Temperature value register	**6_H**	**00_H**

7 ... 0
Temp (7...0)
r

Field	Bits	Type	Description
Temp	7:0	r	**Temperature Value** Temperature value. Below or above the specified operating temperature range non-linearities may occur. If temperature measurement is deactivated during operation, the last value remains in the register. Reset: 00_H

Note: The factory settings (reg 7 .. byte 9) should be read out once and stored. Those values are needed for further writing commands and are not allowed to change.

Reserved register

Res	Offset	Reset Value
Reserved register	7_H	Device specific

7							0
Reserved							

Field	Bits	Type	Description
Reserved	7:0	res	**Factory settings** Bits 6:3 must be written into register 1_H in case of write. Reset: device specific

Reserved register

Res	Offset	Reset Value
Reserved register	8_H	Device specific

7							0
Reserved							

Field	Bits	Type	Description
Reserved	7:0	res	**Factory settings** Bits 7:0 must be written into register 2_H in case of write. Reset: device specific

Reserved register

Res	Offset	Reset Value
Reserved register	9_H	Device specific

7							0
Reserved							

Field	Bits	Type	Description
Reserved	7:0	res	**Factory settings** Bits 4:0 must be written into register 3_H in case of write. Reset: device specific

7.2.2 Write Registers

Registers will be written starting always from address 0_H and as many registers as long as a the master generates a clock signal (SCL).

7.2.2.1 Register Descriptions

Reserved register

Res	**Offset**	**Reset Value**
Reserved register	**0_H**	**00_H**

7							0
Reserved							

Field	Bits	Type	Description
Reserved	7:0	res	**Reserved** Non-configurable bits. Reset: 00_H

Mode 1 register

MOD1	**Offset**	**Reset Value**
Mode 1 register	**1_H**	**Device specific**

7	6	5	4	3	2	1	0
P	**IICAddr**		Reserved		**INT**	**FAST**	**LOW**
w	w				w	w	w

Field	Bits	Type	Description
P	7	w	**Parity bit** Parity of configuration map. Sum of all 32 bits from write registers 0_H, 1_H, 2_H and 3_H must be odd. The parity bit must be calculated by the master prior to execute the write comand. Once the write comand is executed (including the parity bit), the sensor verifies the parity bit with the bits in the registers. If the verification fails, the sensor sets ACK at “high” at the next read command. Reset: device specific
IICAddr	6:5	w	**I2C address bits** Bits can be set to “00”, “01”, “10” or “11” to define the slave address in bus configuration. Reset: 00_B
Reserved	4:3	res	**Factory settings** Bits must correspond to bits 4:3 from read register 7_H. Reset: device specific
INT		w	**Interrupt pad enabled** If “1” INT (interrupt pulse) enabled (default) If “0” INT (interrupt pulse) disabled After a completed conversion, an interrupt pulse will be generated. For bus configurations INT is not recommended, unless timing constraints between I2C data transfers and interrupt pulses are monitored and aligned Reset: 1_B
FAST		w	**Fast mode** If “1” fast mode enabled If “0” fast mode disabled In order to enter power down mode please set FAST=0 and LOW=0 Reset: 0_B
LOW		w	**Low power mode** If “0” disabled If “1” enabled In order to enter power down mode please set FAST=0 and LOW=0 Reset: 0_B

Reserved register

Res	Offset	Reset Value
Reserved register	**2_H**	**Device specific**

7							0
Reserved							

Field	Bits	Type	Description
Reserved	7:0	res	**Factory settings** Bits must correspond to bits 7:0 from read register 8_H. Reset: device specific

Mode 2 register

MOD2	Offset	Reset Value
Mode 2 register	**3_H**	**device-specific $_H$**

7	6	5	4				0
T	**LP**	**PT**	Reserved				
w	w	w					

Field	Bits	Type	Description
T	7	w	**Temperature measurement enabled** If "0" temperature measurement enabled (default) If "1" temperature measurement disabled I_{DD} increases by +33% for enabled temperature measurement. If temperature measurement disabled, last value remains in the bitmap. Reset: 0_B
LP	6	w	**Low Power period** If "0" period is 100ms (ultra low power period) If "1" period is 12ms Reset: 0_B
PT	5	w	**Parity test enabled** If "0" parity test disabled If "1" parity test enabled (default) Reset: 1_B

Field	Bits	Type	Description
Reserved	4:0	res	**Factory setting** Bits must correspond to bits 4:0 from read register 9_H. Reset: device specific

8 Revision History

Revision	Date	Changes
1.02	2016-05	**Chapter 5.1**: added Power Down Mode paragraph. Mode 1 Register: Desciption for P bit, for FAST and LOW bits updated
1.01	2016-04	Features: first feature updated. Mode 1 Register: Desciption for Reserved bits 4:3 updated
1.0	2016-02	Initial version

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