

# BT1306-400D/600D

Logic level triac

Rev. 2 — 14 September 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level sensitive gate triac intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

### 1.2 Features and benefits

- Sensitive gate in all four quadrants
- Low cost package.

### 1.3 Applications

- General purpose bidirectional switching
- Solid state relays
- Phase control applications
- Low power AC fan speed controllers.

### 1.4 Quick reference data

- $V_{DRM} \leq 600$  V (BT1306-600D)
- $V_{DRM} \leq 400$  V (BT1306-400D)
- $I_{TSM} \leq 8$  A
- $I_{T(RMS)} \leq 0.6$  A.

## 2. Pinning information

Table 1. Pinning - SOT54 (TO-92), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	main terminal 2	<p style="text-align: center;">msb033</p>	<p style="text-align: center;">mb1305</p>
2	gate		
3	main terminal 1		

**SOT54 (TO-92)**

### 3. Ordering information

Table 2. Ordering information

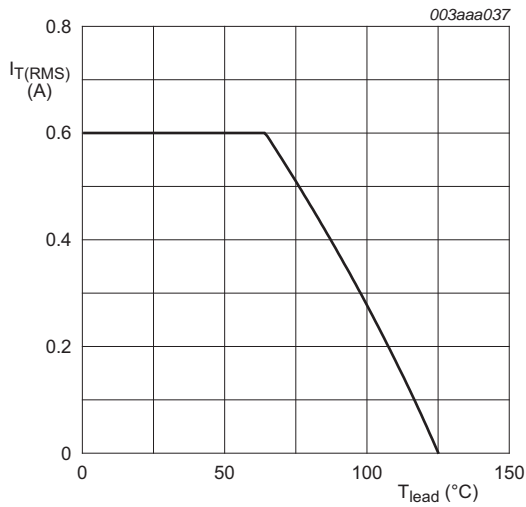
Type number	Package		Version
	Name	Description	
BT1306-600D	TO-92	Plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT1306-400D	TO-92	Plastic single-ended leaded (through hole) package; 3 leads	SOT54

### 4. Limiting values

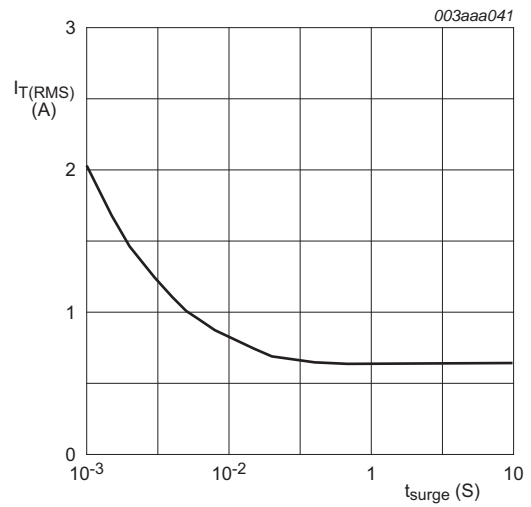
Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DRM}$	repetitive peak off-state voltage					
		BT1306-600D	$25\text{ °C} \leq T_j \leq 125\text{ °C}$	-	600	V
		BT1306-400D		-	400	V
$I_{T(RMS)}$	on-state current (RMS value)	full sine wave; $T_{lead} \leq 65\text{ °C}$ ; <a href="#">Figure 1</a> and <a href="#">2</a>	-	0.6	A	
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_j = 25\text{ °C}$ prior to surge; <a href="#">Figure 3</a> and <a href="#">4</a>				
		$t = 20\text{ ms}$	-	8	A	
		$t = 16.7\text{ ms}$	-	8.8	A	
$I^2t$	$I^2t$ for fusing	$t = 10\text{ ms}$	-	0.32	A <sup>2</sup> s	
$di_T/dt$	repetitive rate of rise of on-state current after triggering	$I_{TM} = 1\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $di_G/dt = 0.2\text{ A}/\mu\text{s}$				
		T2+ G+	-	50	A/ $\mu\text{s}$	
		T2+ G-	-	50	A/ $\mu\text{s}$	
		T2- G-	-	50	A/ $\mu\text{s}$	
		T2- G+	-	10	A/ $\mu\text{s}$	
$I_{GM}$	gate current (peak value)	$t = 2\text{ }\mu\text{s max}$	-	1	A	
$V_{GM}$	gate voltage (peak value)		-	5	V	
$P_{GM}$	gate power (peak value)		-	5	W	
$P_{G(AV)}$	average gate power	$t = 2\text{ }\mu\text{s max}$ ; $T_{case} \leq 80\text{ °C}$	-	0.1	W	
$T_{stg}$	storage temperature		-40	+150	°C	
$T_j$	junction temperature		-40	+125	°C	

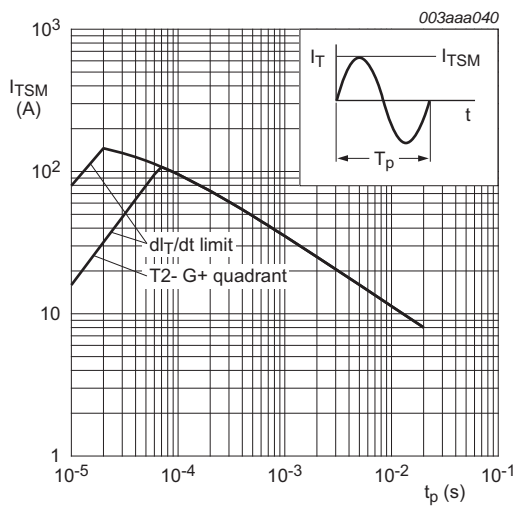


**Fig 1.** Maximum permissible on-state current (RMS value) as a function of lead temperature.



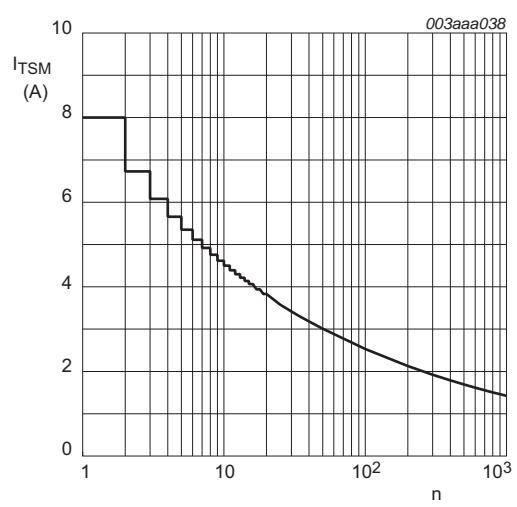
f = 50 Hz  
T<sub>lead</sub> ≤ 65 °C

**Fig 2.** Maximum permissible repetitive on-state current (RMS value) as a function of surge duration for sinusoidal currents.



t<sub>p</sub> ≤ 20 ms  
initial T<sub>j</sub> ≤ 25 °C

**Fig 3.** Maximum permissible non-repetitive peak on-state current as a function of pulse width for sinusoidal currents.



n = number of cycles  
f = 50 Hz  
initial T<sub>j</sub> ≤ 25 °C

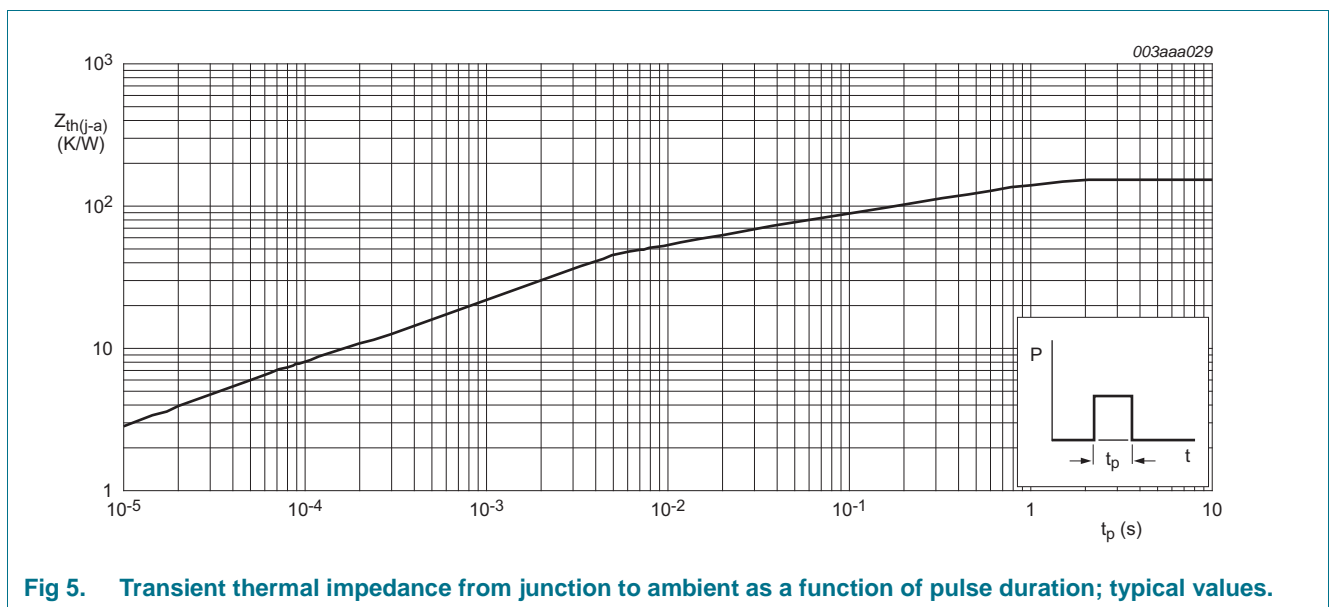
**Fig 4.** Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

## 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	-	-	60	K/W
		half cycle			80	
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; lead length = 4 mm; <a href="#">Figure 5</a>	-	150	-	K/W

### 5.1 Transient thermal impedance

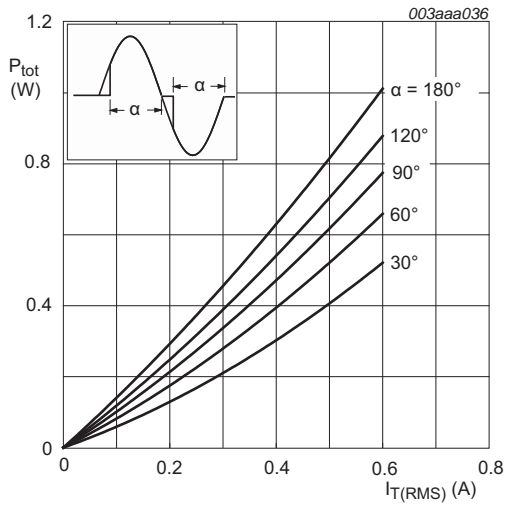


## 6. Characteristics

**Table 5. Characteristics**

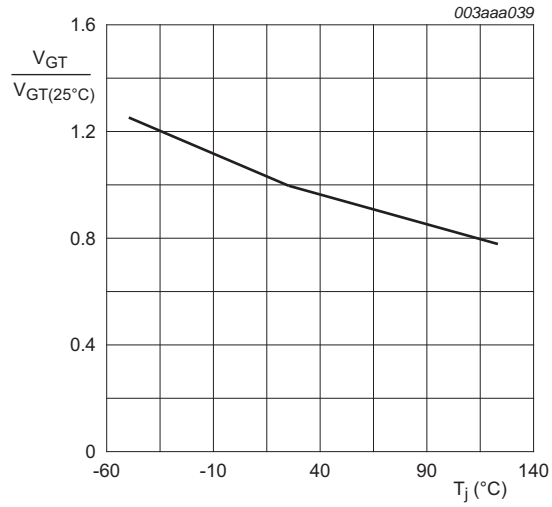
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; <a href="#">Figure 8</a>				
		T2+ G+	-	1	5	mA
		T2+ G-	-	2	5	mA
		T2- G-	-	2	5	mA
		T2- G+	-	4	7	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; <a href="#">Figure 9</a>				
		T2+ G+	-	1	10	mA
		T2+ G-	-	5	10	mA
		T2- G-	-	1	10	mA
		T2- G+	-	2	10	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.1\text{ A}$ ; <a href="#">Figure 10</a>	-	1	10	mA
$V_T$	on-state voltage	$I_T = 0.85\text{ A}$ ; <a href="#">Figure 11</a>	-	1.4	1.9	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; <a href="#">Figure 7</a>	-	0.9	2	V
		$V_D = V_{DRM}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 110\text{ °C}$	0.1	0.7	-	V
$I_D$	off-state leakage current	$V_D = V_{DRM(max)}$ ; $T_j = 110\text{ °C}$	-	3	100	$\mu\text{A}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	critical rate of rise of off-state voltage	$V_D = 67\%$ of $V_{DM(max)}$ ; $T_{case} = 110\text{ °C}$ ; exponential waveform; gate open circuit; <a href="#">Figure 12</a>	30	45	-	$\text{V}/\mu\text{s}$
$dV_{com}/dt$	critical rate of rise of commutation voltage	$V_D = \text{rated } V_{DM}$ ; $T_{case} = 50\text{ °C}$ ; $I_{TM} = 0.84\text{ A}$ ; commutating $di/dt = 0.3\text{ A/ms}$	-	5	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate controlled turn-on time	$I_{TM} = 1.0\text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 25\text{ mA}$ ; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$



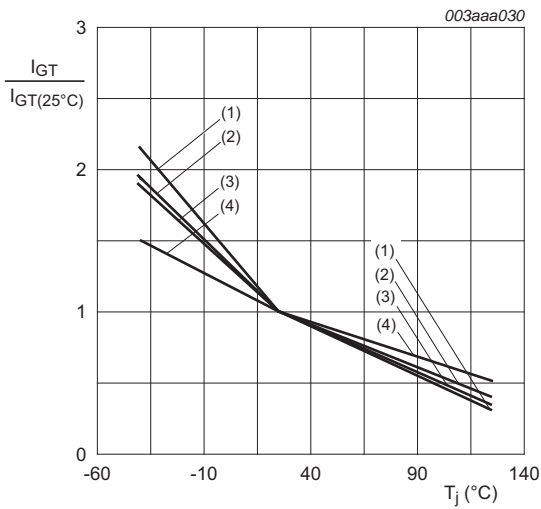
$\alpha$  = conduction angle

**Fig 6. On-state dissipation as a function of on-state current (RMS value); maximum values.**



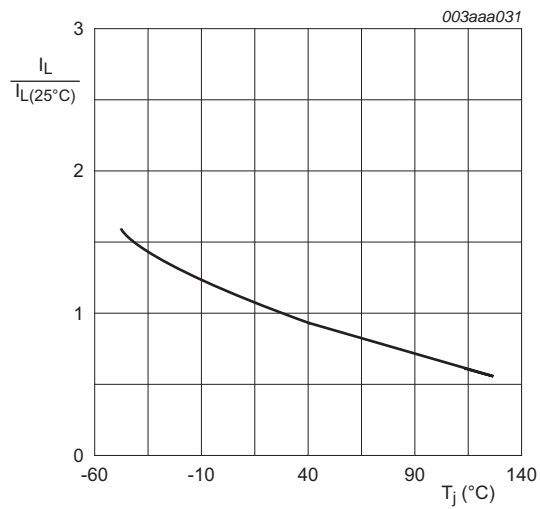
$$a = \frac{V_{GT(T_j)}}{V_{GT(25^\circ C)}}$$

**Fig 7. Normalized gate trigger voltage as a function of junction temperature; typical values.**



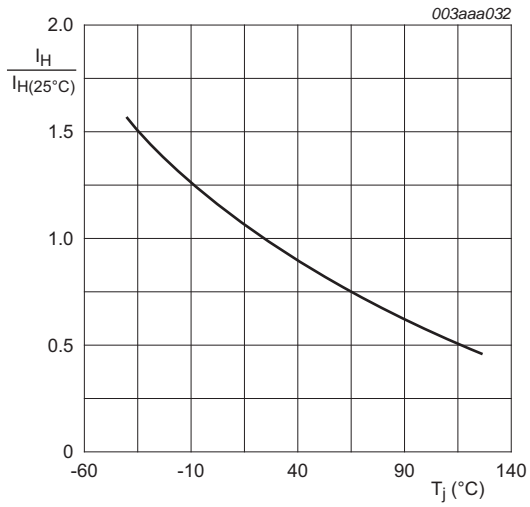
$$a = \frac{I_{GT(T_j)}}{I_{GT(25^\circ C)}}$$

**Fig 8. Normalized gate trigger current as a function of junction temperature; typical values.**



$$a = \frac{I_L(T_j)}{I_L(25^\circ C)}$$

**Fig 9. Normalized latching current as a function of junction temperature; typical values.**



$$a = \frac{I_H(T_j)}{I_H(25^\circ C)}$$

Fig 10. Normalized holding current as a function of junction temperature; typical values.

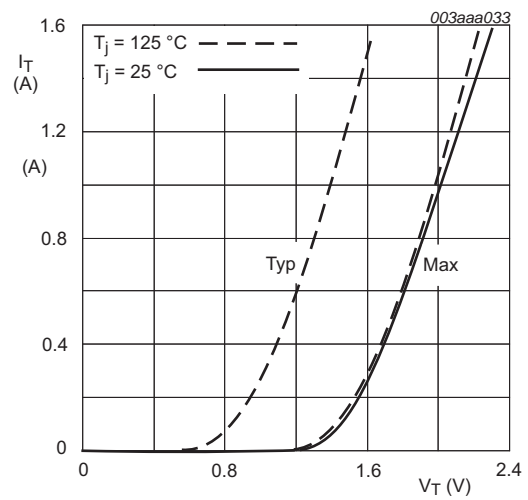


Fig 11. On-state current as a function of on-state voltage; typical and maximum values.

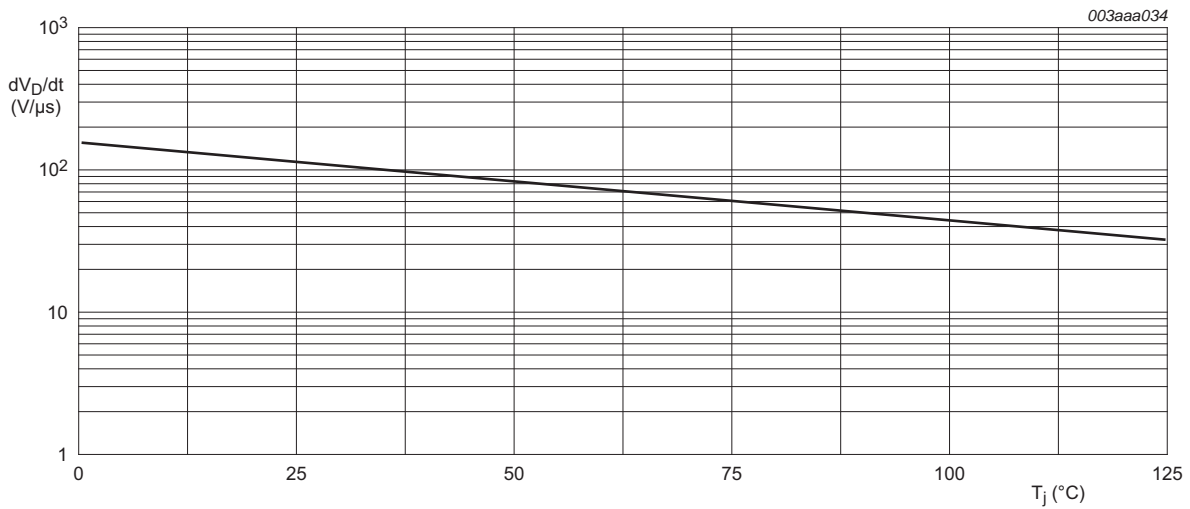


Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values.

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

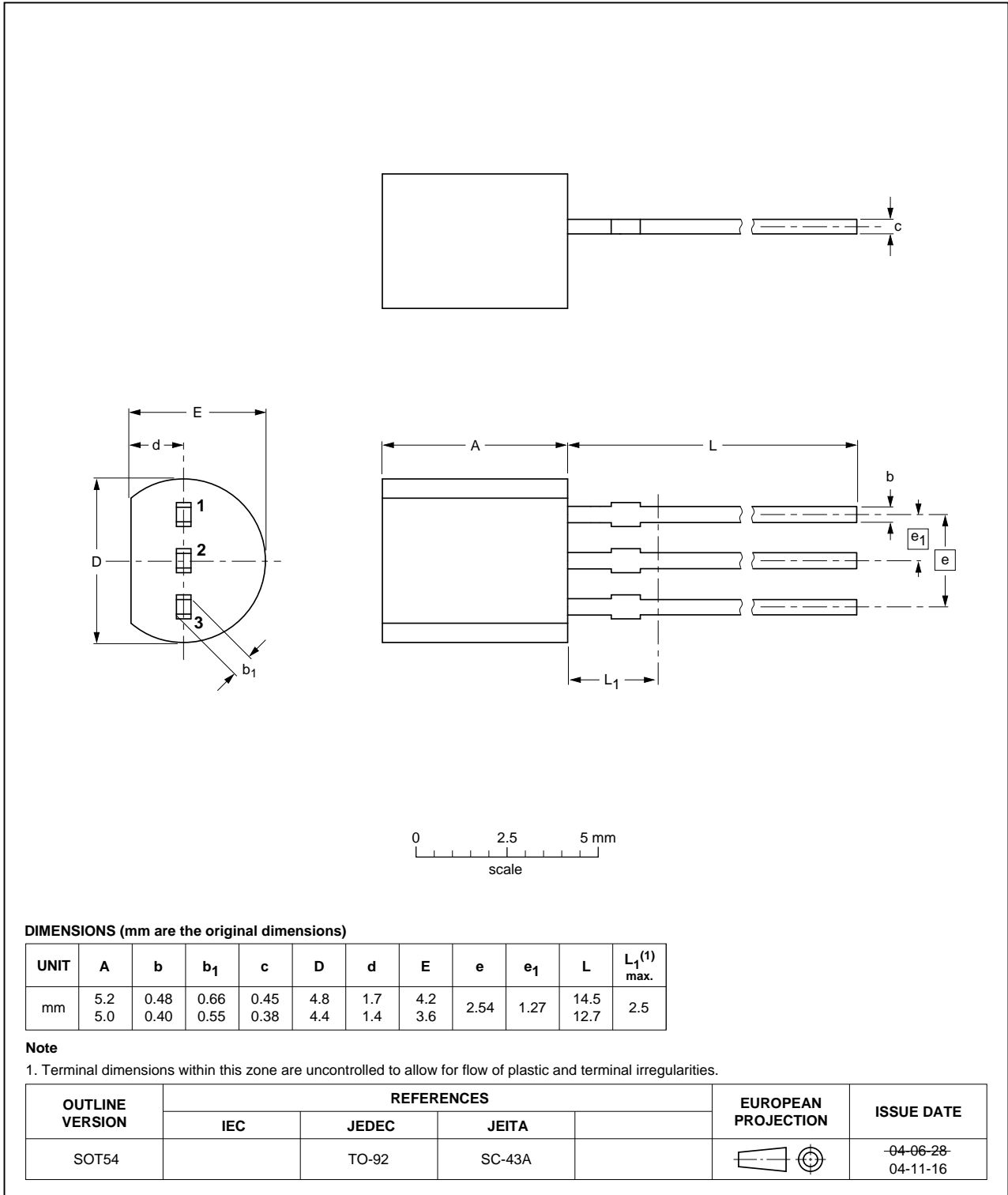


Fig 13. SOT54 (TO-92).



## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT1306_XXXD_SER v.2	20110914	Product data sheet	-	BT1306_XXXD_SER v.1 (9397 750 12593)
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Package outline drawings have been updated to the latest version.</li></ul>		
BT1306_XXXD_SER v.1 (9397 750 12593)	20040219	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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