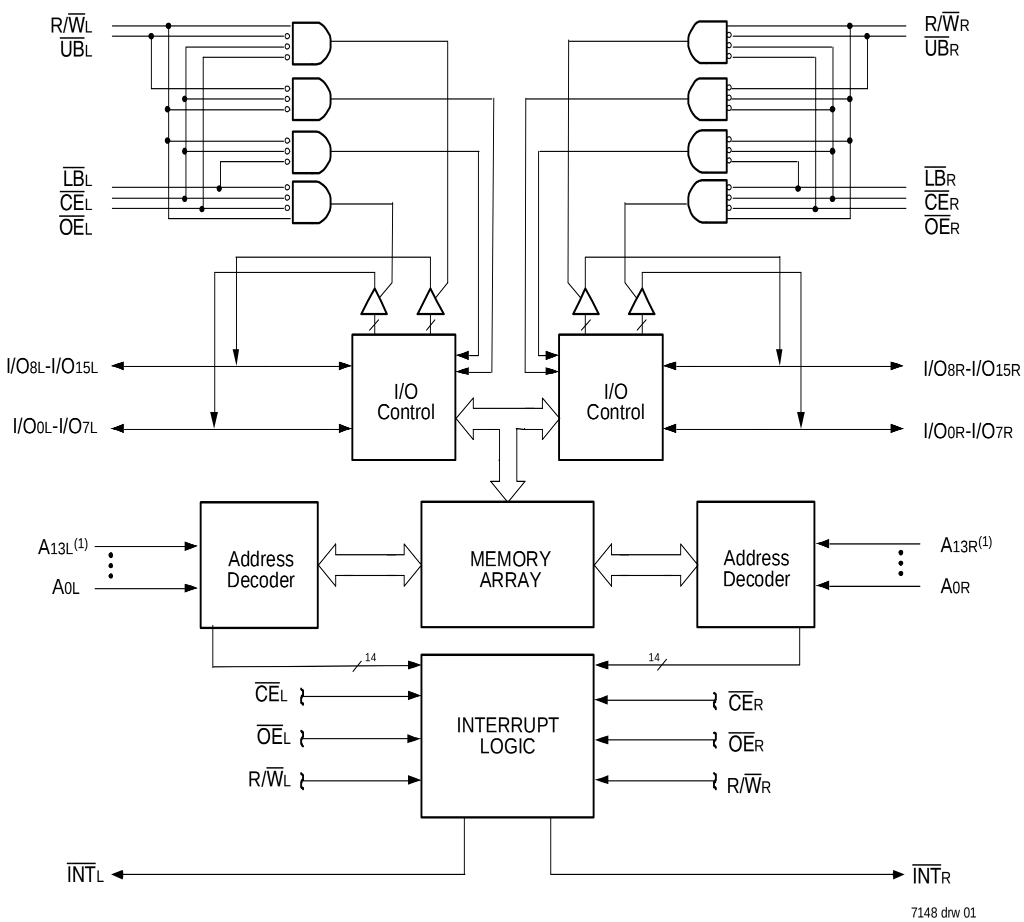
IDT70P264/254/244L DATASHEET

VERY LOW POWER 1.8V 16K/8K/4K x 16 DUAL-PORT STATIC RAM

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - *Industrial: 40/55ns (max.)*
- Low-power operation
  IDT70P264/254/244L
  Active: 27mW (typ.)
  Standby: 3.6µW (typ.)
- On-chip port interrupt logic which supports level shift output
- Fully asynchronous operation from either port
- Power supply isolation functionality to aid system power management
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- Left port is selectable 3.0V, 2.5V or 1.8V
- Right port is 1.8V I/O
- LVTTL-compatible, single 1.8V (±100mV) power supply
- Available in 81 Ball 0.5mm-pitch BGA
- Industrial temperature range (-40°C to +85°C)
- Green parts available, see ordering information

Functional Block Diagram



NOTE:
1. A13X is a NC for IDT70P254. A13X and A12X are NC for IDT70P244.

FEBRUARY 2009

Description

The IDT70P264/254/244 is a very low power 16K/8K/4K x 16 Dual-Port Static RAM. The IDT70P264/254/244 is designed to be used as a stand-alone 256/128/64K-bit Dual-Port SRAM.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 27mW of power.

The IDT70P264/254/244 is packaged in a 81 ball 0.5mm- pitch Ball Grid Array. The package is a 1mm thick and designed to fit in wireless handset applications.

Pin Configurations

70P264/254/244BY
BY-81

81-Ball 0.5mm Pitch BGA
Top View

	1	2	3	4	5	6	7	8	9	
A	A_{2R}	A_{5R}	A_{11R}	$\overline{CE}_R$	V_{SS}	I/O_{14R}	I/O_{12R}	I/O_{10R}	I/O_{8R}	A
B	A_{1R}	A_{7R}	A_{9R}	A_{12R}[1]	A_{13R}[1]	I/O_{13R}	I/O_{11R}	V_{SS}	I/O_{7R}	B
C	A_{0R}	A_{6R}	A_{8R}	A_{10R}	$R/\overline{W}_R$	I/O_{15R}	V_{DD}	I/O_{9R}	I/O_{6R}	C
D	$\overline{UB}_R$	A_{3R}	A_{4R}	$\overline{INT}_R$	$\overline{OE}_R$	I/O_{5R}	I/O_{2R}	I/O_{4R}	I/O_{3R}	D
E	V_{SS}	$\overline{LB}_L$	$\overline{INT}_L$	$\overline{LB}_R$	V_{DD}	I/O_{13L}	I/O_{15L}	I/O_{0R}	I/O_{1R}	E
F	$\overline{UB}_L$	A_{4L}	A_{2L}	A_{3L}	I/O_{3L}	I/O_{5L}	I/O_{12L}	V_{DDQL}	I/O_{14L}	F
G	A_{0L}	A_{1L}	A_{11L}	A_{12L}[1]	$\overline{OE}_L$	I/O_{4L}	I/O_{9L}	I/O_{11L}	I/O_{10L}	G
H	A_{6L}	A_{8L}	A_{9L}	A_{13L}[1]	$\overline{CE}_L$	I/O_{0L}	I/O_{2L}	V_{SS}	I/O_{8L}	H
J	A_{5L}	A_{7L}	A_{10L}	$R/\overline{W}_L$	V_{SS}	I/O_{1L}	V_{DDQL}	I/O_{6L}	I/O_{7L}	J
	1	2	3	4	5	6	7	8	9	

7148 drw 02

NOTE:
1. A_{13X} is a NC for IDT70P254. A_{13X} and A_{12X} are NC for IDT70P244.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable (Input)
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A_{0L} - A_{13L}[1]	A_{0R} - A_{13R}[1]	Address (Input)
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select (Input)
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
V_{DD}		Power for Core + Right Port I/O (1.8V) (Input)
V_{DDQL}		Left Port I/O Supply Voltage (1.8V, 2.5V or 3.0V) (Input)
V_{SS}		Ground (0V) (Input)

7148 tbl 01

NOTE:
1. A_{13X} is a NC for IDT70P254. A_{13X} and A_{12X} are NC for IDT70P244.

Truth Table I: Non-Contention Read/Write Control

Inputs					Outputs		
$\overline{CE}$	$R/\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_{8-15}	I/O_{0-7}	Mode
H	X	X	X	X	High-Z	High-Z	Deselected: Power Down
X	X	X	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	$DATA_{IN}$	High-Z	Write to Upper Byte Only[1]
L	L	X	H	L	High-Z	$DATA_{IN}$	Write to Lower Byte Only[1]
L	L	X	L	L	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes[1]
L	H	L	L	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	H	L	H	L	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	High-Z	High-Z	Outputs Disabled

7148 tbl 02

NOTE:
1. A_{0L} — $A_{13L} \neq A_{0R}$ — A_{13R}

Absolute Maximum Ratings[1]

Symbol	Rating	Industrial	Unit
V_{TERM}	Supply Voltage on V_{DD} with Respect to GND	-0.5 to +2.9	V
V_{TERM}	Supply Voltage on V_{DDQL} with Respect to GND	-0.5 to +3.6	V
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.3[4]	V
T_{BIAS}[3]	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT} (for V_{DDQL} = 3.0V)	DC Output Current	20	mA
I_{OUT} (for V_{DDQL} = 2.5V)	DC Output Current	20	mA

7148 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period over V_{TERM} = V_{DD} + 0.3V.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.
4. V_{DDQL} + 0.3V for left port.

Capacitance
(TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

7148 tbl 07

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	V_{DD}
Industrial	-40°C to +85°C	0V	1.8V ± 100mV

7148 tbl 04

NOTE:
1. This is the parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions (V_{DDQL} = 3.0V±300mV)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDQL}	Left Port Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	0	0	V
V_{IHL}	Input High Voltage (V_{DDQL} = 3.0V)	2.0	—	V_{DDQL} + 0.2	V
V_{ILL}	Input Low Voltage (V_{DDQL} = 3.0V)	-0.2	—	0.7	V
V_{IHR}	Input High Voltage	1.2	—	V_{DD} + 0.2	V
V_{ILR}	Input Low Voltage	-0.2	—	0.4	V

7148 tbl 05

Recommended DC Operating Conditions (V_{DDQL} = 2.5V±100mV)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDQL}	Left Port Supply Voltage	2.4	2.5	2.6	V
V_{SS}	Ground	0	0	0	V
V_{IHL}	Input High Voltage (V_{DDQL} = 2.5V)	1.7	—	V_{DDQL} + 0.3	V
V_{ILL}	Input Low Voltage (V_{DDQL} = 2.5V)	-0.3	—	0.6	V
V_{IHR}	Input High Voltage	1.2	—	V_{DD} + 0.2	V
V_{ILR}	Input Low Voltage	-0.2	—	0.4	V

7148 tbl 06

Recommended DC Operating Conditions (V_{DDQL} = 1.8V±100mV)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDQL}	Left Port Supply Voltage	1.7	1.8	1.9	V
V_{SS}	Ground	0	0	0	V
V_{IHL}	Input High Voltage (V_{DDQL} = 1.8V)	1.2	—	V_{DDQL} + 0.2	V
V_{ILL}	Input Low Voltage (V_{DDQL} = 1.8V)	-0.2	—	0.4	V
V_{IHR}	Input High Voltage	1.2	—	V_{DD} + 0.2	V
V_{ILR}	Input Low Voltage	-0.2	—	0.4	V

7148 tbl 06_5

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{DD} + 0.3V.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8V ± 100mV)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{DD} = 1.8V, V_{IN} = 0V to V_{DD}	-1	1	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{DD}	-1	1	µA
V_{OLL}	Output Low Voltage (V_{DDQL} = 3.0V)	I_{OLL} = +2mA	—	0.4	V
V_{OHL}	Output High Voltage (V_{DDQL} = 3.0V)	I_{OHL} = -2mA	2.1	—	V
V_{OLL}	Output Low Voltage (V_{DDQL} = 2.5V)	I_{OLL} = +2mA	—	0.4	V
V_{OHL}	Output High Voltage (V_{DDQL} = 2.5V)	I_{OHL} = -2mA	2.0	—	V
V_{OLL}	Output Low Voltage (V_{DDQL} = 1.8V)	I_{OLL} = +0.1mA	—	0.2	V
V_{OHL}	Output High Voltage (V_{DDQL} = 1.8V)	I_{OHL} = -0.1mA	V_{DDQL} - 0.2V	—	V
V_{OLR}	Output Low Voltage	I_{OLR} = +0.1mA	—	0.2	V
V_{OHR}	Output High Voltage	I_{OHR} = -0.1mA	V_{DD} - 0.2V	—	V
V_{OLINT}(1,2)	Output Low Voltage Interrupt	I_{OL} = +2mA	—	0.4	V

7148 tbl 08

NOTES:
1. Interrupt can be level shifted to a higher voltage by tieing a resistor (R3) to an external power supply ($VDDINT_X$). The value of R3 is a trade off between t_{INX} and power.
2. $VDDINT_R \geq V_{DD}$, $VDDINT_L \geq V_{DDQL}$

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8V ±100mV)

Symbol	Parameter	Test Condition	Version	70P264/254/244 Ind'l Only 40ns Typ.(1)	40ns Max.	55ns Typ.(1)	55ns Max.	Unit
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_R$ and $\overline{CE}_L$ = V_{IL}, Outputs Open f = f_{MAX}(2)	IND'L L	25	40	15	25	mA
I_{SB1}	Standby Current (Both Ports Inactive)	$\overline{CE}_R$ = V_{DD} - 0.2V and $\overline{CE}_L$ = V_{DDQL} - 0.2V, f = f_{MAX}(2)	IND'L L	2	6	2	6	µA
I_{SB2}	Standby Current (One Port Inactive, One Port Active)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}(3), Active Port Outputs Open f = f_{MAX}(2)	IND'L L	8.5	18	8.5	14	mA
I_{SB3}	Full Standby Current (Both Ports Inactive - CMOS Level Inputs)	$\overline{CE}_L \geq V_{DDQL}$ - 0.2V and $\overline{CE}_R \geq V_{DD}$ - 0.2V, f = 0	IND'L L	2	6	2	6	µA
I_{SB4}	Standby Current (One Port Inactive, One Port Active - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{DDQ} - 0.2V(3), Active Port Outputs Open f = f_{MAX}(2)	IND'L L	8.5	18	8.5	14	mA

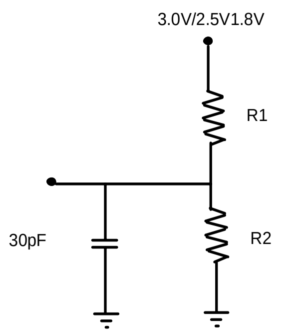
7148 tbl 09

NOTES:
1. V_{DD} = 1.8V, T_A = +25°C, and are not production tested. I_{DD} = 15mA (typ.)
2. At f = f_{MAX}, address and control lines are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC Test Conditions".
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC Test Conditions

Input Pulse Levels	GND to 3.0V/GND to 2.5V/GND to 1.8V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V/1.25V/0.9V
Output Reference Levels	1.5V/1.25V/0.9V
Output Load	Figure 1A

7148 tbl 10



7148 drw 03

	3.0V/2.5V	1.8V
R1	1022Ω	13500Ω
R2	729Ω	10800Ω

7148 tbl 10_5

Figure 1A. AC Output Test Load (5pF for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

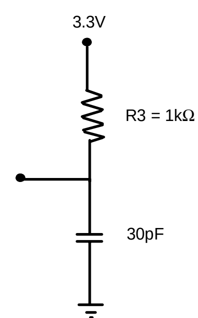


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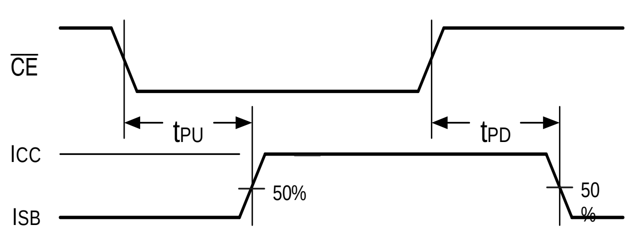
Figure 1B. AC Output Test Load for Interrupt

Timing of Power-Up Power-Down



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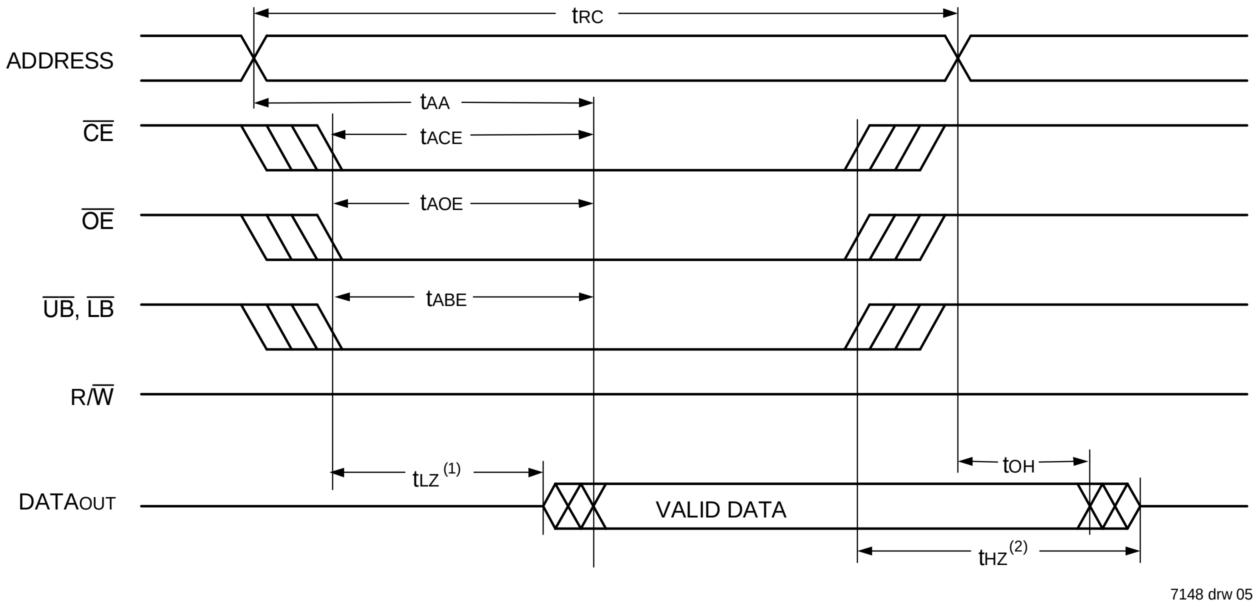
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[2]

Symbol	Parameter	70P264/254/244 Ind'l Only				Unit
		40ns		55ns		
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	40	—	55	—	ns
t_{AA}	Address Access Time	—	40	—	55	ns
t_{ACE}	Chip Enable Access Time	—	40	—	55	ns
t_{ABE}	Byte Enable Access Time	—	40	—	55	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	ns
t_{LZ}	Output Low-Z Time[1,3]	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1,3]	—	10	—	25	ns
t_{PU}	Chip Enable to Power Up Time[1]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1]	—	40	—	55	ns

7148 tbl 11

NOTES:
1. This parameter is guaranteed by device characterization, but is not production tested.
2. The specification for t_{DH} must be met by the device supplying write data to the SRAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
3. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.

Waveform of Read Cycles



NOTES:

1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.

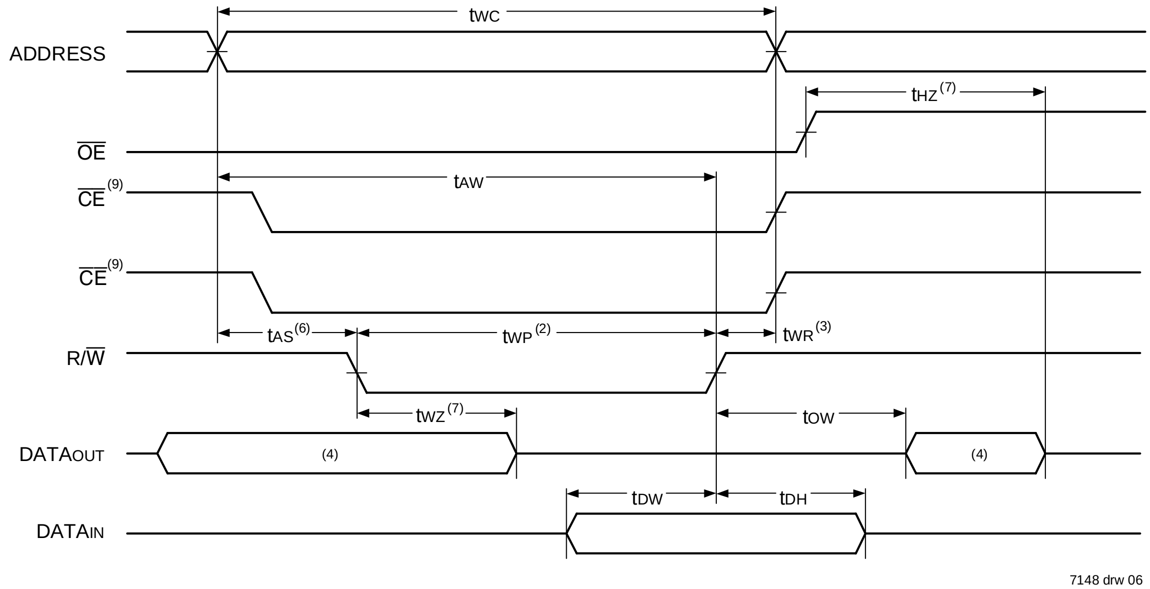
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(3)

Symbol	Parameter	70P264/254/244 Ind'l Only				Unit
		40ns		55ns		
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	40	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write(2)	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time(2)	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	30	—	ns
t_{DH}	Data Hold Time(3)	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1)	—	15	—	25	ns
t_{OW}	Output Active from End-of-Write(1,3)	0	—	0	—	ns

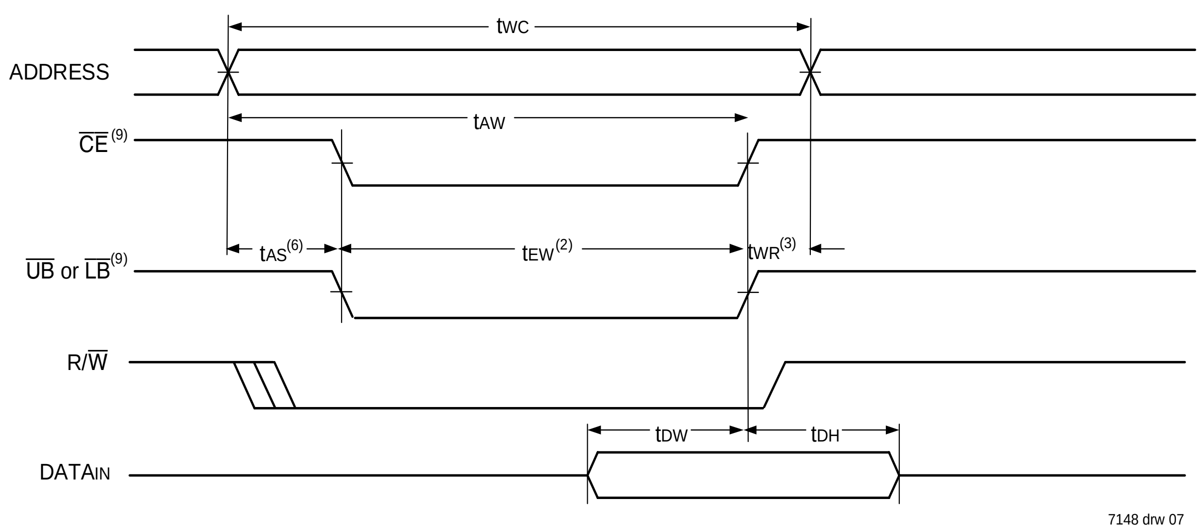
7148 tbl 12

NOTES:
1. This parameter is guaranteed by device characterization, but is not production tested.
2. To access SRAM, $\overline{CE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$.
3. The specification for t_{DH} must be met by the device supplying write data to the SRAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



Timing Waveform of Write Cycle No. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ Controlled Timing(1,5)



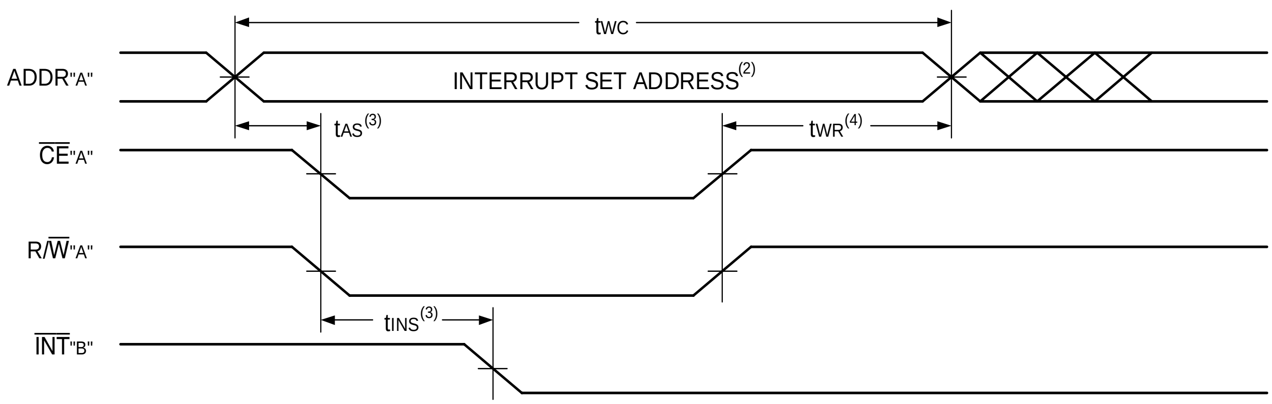
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{UB}$ or $\overline{LB}$ and a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$ or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested.
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access SRAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	70P264/254/244 Ind'l Only 40ns Min.	40ns Max.	55ns Min.	55ns Max.	Unit
INTERRUPT TIMING						
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	35	—	45	ns
t_{INR}	Interrupt Reset Time	—	45	—	45	ns

7148 tbl 13

Waveform of Interrupt Timing(1)



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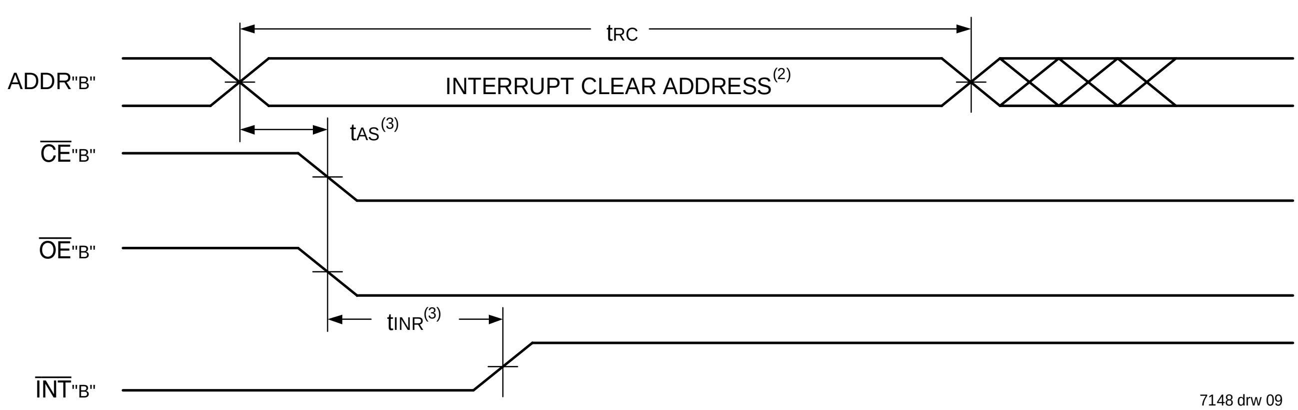

7148 drw 09

NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from “A”.
2. See Interrupt Truth Table II.
3. Timing depends on which enable signal (CE or R/W) is asserted last.
4. Timing depends on which enable signal (CE or R/W) is de-asserted first.

Truth Table II — Interrupt Flag(1)

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{13L}-A_{0L}(1)	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{13R}-A_{0R}(1)	$\overline{INT}_R$	
L	L	X	3FFF	X	X	X	X	X	L	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L	L	L	X	3FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE	H	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

7148 tbl 14

NOTES:
1. A_{13X} is a NC for IDT70P254. A_{13X} and A_{12X} are NC for IDT70P244. Interrupt Addresses are 1FFF and 1FFE for IDT70P254 and FFF and FFE for IDT70P244.

Functional Description

The IDT70P264/254/244 provides two ports with separate control, address and I/O pins that permit independent access to any location in memory. The IDT70P264/254/244 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

Power Supply

Each port can operate on independent I/O voltages. This is determined by what is connected to the V_{DDIOL} and V_{DD} pins. The supported I/O standards are 1.8V/2.5V LVCMOS and 3.0V LVTTL.

The IDT70P264/254/244 includes power supply isolation functionality which aids system power management. V_{DD} and V_{DDIOL} can be independently powered up/down which allows the left port or the right port and core to be powered down when not in use. If V_{DDIOL} is powered down, but V_{DD} remains powered up all inputs to the core from the left port will be forced to deasserted states at full swing DC values to minimize leakage current and active power consumption. If V_{DD} is powered down but V_{DDIOL} remain powered up, all outputs for the left port will remain in the state they were in prior to power down.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FFE (HEX) (1FFE for IDT70P254, FFE for IDT70P244), where a write is defined as the $\overline{CE}$=R/$\overline{W}$=V_{IL} per Truth Table II. The left port clears the interrupt by accessing address location 3FFE (1FFE for IDT70P254, FFE for IDT70P244) when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FFF (HEX) (1FFF for IDT70P254, FFF for IDT70P244) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FFF. The message (16 bits) at 3FFE or 3FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

The interrupt outputs of the IDT70P264/254/244 should be connected to an interrupt power supply ($VDDINT_X$) through an external pull-up resistor. As long as $VDDINT_R \geq VDD$ and $VDDINT_L \geq VDDQ_L$, there will be no current flowing between $VDDINT_X$ and VDD/$VDDQ_L$.

Ordering Information

XXXXX (Device Type) — A (Power) — 999 (Speed) — A (Package) — A — A (Process/Temperature Range)

Process/Temperature Range	I	Industrial (-40°C to +85°C)
	G	Green
Package	BY	81 Ball 0.5mm-pitch BGA(BY81)
Speed	40 55	Industrial Only } Speed in nanoseconds
Power	L	Low Power
Device Type	70P264 70P254 70P244	256K (16K x 16) 1.8V Dual-Port SRAM 128K (8K x 16) 1.8V Dual-Port SRAM 64K (4K x 16) 1.8V Dual-Port SRAM

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Datasheet Document History

09/26/08: Initial Datasheet
02/20/09: Removed Preliminary status from entire datasheet
Page 14 Removed "IDT" from orderable part number

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