Reference Manual

EPIC-2 (Gecko)

AMD GX 500 Based SBC with Ethernet, Video, Audio and Industrial I/O

EPIC-2

AMD GX 500 Based SBC with Ethernet, Video, Audio and Industrial I/O

![VersaLogic Corporation logo]

Product Release Notes

> This page includes recent changes or improvements that have been made to this product. These changes may affect its operation or physical installation in your application. Please read the following information.

Rev 4 Release
- For revision 4.xx boards

Rev 3 Release
- For revision 3.xx boards

Rev 2 Release
- Beta release only.

Rev 1 Release
- Pre-production only. No customer releases.

Support Page

The **EPIC-2 support page**, at **http://www.VersaLogic.com/private/geckosupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for EPIC-2 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

Model EPIC-2
AMD GX 500 SBC with Ethernet,
Video, Audio and Industrial I/O

REFERENCE MANUAL

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Notice:

Table of Contents

Introduction

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1

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Description

The EPIC-2 is a feature-packed single board computer designed for OEM control projects requiring fast processing, industrial I/O, flexible memory options and designed-in reliability and longevity (product lifespan). Its features include:

- AMD GX 500 microcontroller
- Up to 512 MB system RAM
- CS5535 Companion Chip
- CompactFlash site
- 10/100 Ethernet interface
- Flat Panel Display support
- PC/104-Plus expansion site
- ATA-5 IDE controller
- Four USB 1.1 Ports.
- TVS devices
- PCI-based audio
- 4 COM + 1 LPT port
- CPU temperature sensor

- PS/2 keyboard and mouse ports
- Industrial I/O
  - Analog input
  - 16 channel Digital I/O
  - Two RS232 COM ports
  - Two 422/485 selectable COM ports
- Watchdog timer
- Vcc sensing reset circuit
- EPIC-compliant 4.5" x 6.50" footprint
- Field upgradeable BIOS with OEM enhancements
- Latching I/O connectors
- Customizing available
- Low-power fanless version

This EPIC-2-compliant single board computer accepts AMD GX 500 Processors. The board is compatible with popular operating systems such as Windows, QNX, VxWorks and Linux.

A full complement of standard I/O ports is included on the board. Additional I/O expansion is available through the high-speed PCI-based PC/104-Plus expansion site (which supports both PC/104 and PC/104-Plus expansion modules).

System memory expansion is supported with a high-reliability latching 200-pin SODIMM sockets. Low power 2.5V 200-pin SODIMM modules up to 512 MB maximum.

The EPIC-2 features high reliability design and construction, including latching I/O connectors. It also features a watchdog timer, voltage sensing reset circuits and self-resetting fuse on the 5V supply to the keyboard, mouse and USB.

EPIC-2 boards are subjected to 100% functional testing and are backed by a limited two-year warranty.

Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 115 x 165 mm (4.53 x 6.5 ") EPIC compliant

Storage Temperature: -40° C to 85° C

Operating Temperature:
> 0° C to +60° C free air, no airflow, standard version
> -40° C to +85° C ("e" version)

Power Requirements: *(with 512 MB DDR SODIMMS, keyboard and mouse, Running Win XP)*
> EPIC-2b AMD CPU 5V $\pm$ 5% @ 1.0 A (5.0 W) typ.
> EPIC-2c AMD CPU 5V $\pm$ 5% @ 1.0 A (5.0 W) typ., pass-though connectors
> EPIC-2e AMD CPU 5V $\pm$ 5% @ 1.0 A (5.0 W) typ.
> +3.3V or ±12V may be required by some expansion modules

System Reset:
> V_{cc} sensing, resets below 4.70V typ.
> Watchdog timeout

DRAM Interface:
> One 200-pin DDR SODIMM sockets
> Up to 512 MB, PC2700 or PC2100

Video Interface:
> High Performance. Standard monitor support
> 3.3V LVDS flat panel display interface

IDE Interface:
> One-channel, 44-pin. 2mm connectors. Supports up to and including UDMA5
> Supports up to two IDE devices (hard drives, CD-ROM, etc.)

CompactFlash:
> Shares IDE channel, master or slave

Ethernet Interface:
> Intel 82551ER based Fast Ethernet Controller

Audio Interface:
> Standard Line Out and Line In supported

Analog Input:
> 8-channel, 12-bit, single-ended, 75 ksps, 0 to 4.095V input range

COM1–2 Interface:
> RS-232, 16C550 compatible, 115k baud max.

COM3–4 Interface:
> RS-422/485, 16C550 compatible, 921k baud max.

LPT Interface:
> Bi-directional/EPP/ECP compatible. Floppy disk interface with CBL/CBR-2501

Digital Interface:
> 16-line TTL I/O port

BIOS: General Software Embedded BIOS© 2000 with OEM enhancements
> Field-upgradeable with Flash BIOS Upgrade Utility

Bus Speed:
> DRAM: 244 MHz
> PC/104-*Plus (PCI)*: 33MHz
> PC/104: 8MHz

Compatibility:
> PC/104 – Partial compliance (See PC/104 expansion bus)
> Embedded-PCI (PC/104-*Plus*) – full compliance, 3.3V signaling
> EPIC – full compliance

Weight:
> EPIC-2b – 0.20 kg (0.45 lbs)
> EPIC-2c – 0.22 kg (0.48 lbs)
> EPIC-2e – 0.23 kg (0.50 lbs)

Specifications are subject to change without notice.

EPIC-2 Block Diagram
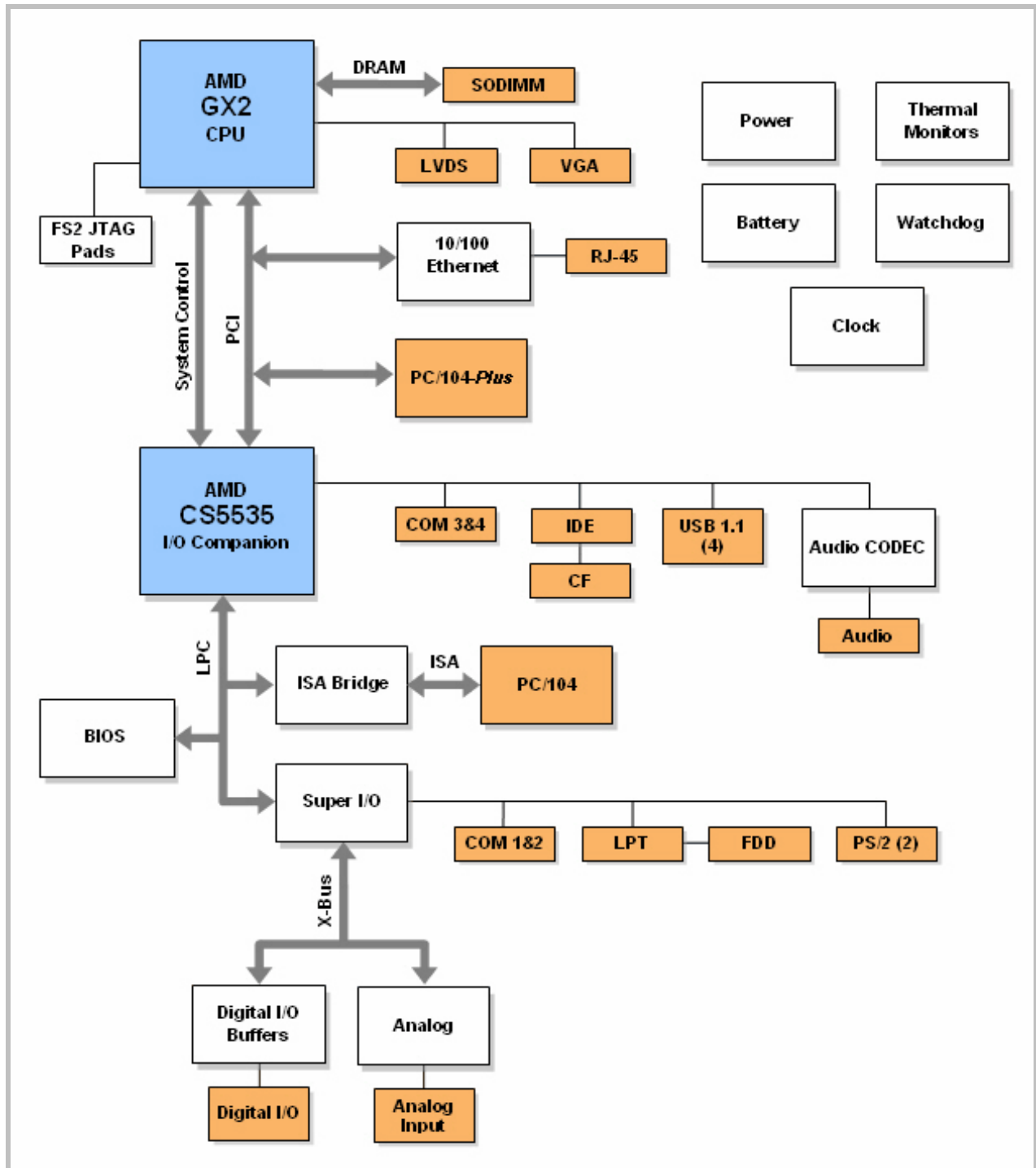
Figure 1. EPIC-2 Block Diagram

Technical Support

If you are unable to solve a problem with this manual please visit the EPIC-2 Product Support web page at **http://www.VersaLogic.com/private/geckosupport.asp**. If you have further questions, contact VersaLogic technical support at (541) 485-8575. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

EPIC-2 Support Website

0Hhttp://www.VersaLogic.com/private/geckosupport.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575.

Please provide the following information:

- Your name, the name of your company and your phone number

- The name of a technician or engineer that can be contact if any questions arise.

- Quantity of items being returned

- The model and serial number (barcode) of each item

- A detailed description of the problem

- Steps you have taken to resolve or recreate the problem

- The return shipping address

Warranty Repair   All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

Overview

ELECTROSTATIC DISCHARGE

Warning!   Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EPIC-2.

LITHIUM BATTERY

Warning!   To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

MOUNTING SUPPORT

Warning!   The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty. See page 11 for more details.

Initial Configuration and Setup

The following list describes the recommended components and gives an abbreviated outline for setting up a typical development system.

RECOMMENDED COMPONENTS

- EPIC-2 Single Board Computer
- 200-pin DDRSODIMM PC2700 or PC2100
- ATX Power Supply
- SVGA Video Monitor
- Keyboard with PS2 Connector or USB Connector
- LPT 3.5" Floppy Disk Drive or USB Floppy Disk Drive (optional)
- IDE Hard Drive (optional)
- IDE CD ROM Drive (optional)

DRAM MODULE

- Insert DRAM module into the SODIMM socket and latch into place.

CABLES / PERIPHERAL DEVICES

- Plug video adapter cable (p/n CBL/CBR-1007) into socket J2, and attach video monitor.
- Plug floppy data cable (p/n CBL/CBR-2501) into LPT port, and attach floppy drive.
- Plug power adapter cable (p/n CBL/CBR-2022) into socket J7, and attach ATX power supply.
- Attach power supply cables to external drives.
- Set hard drive jumpers for master device operation.

CMOS Setup / Boot Procedure

- Turn power on.
- Press the DEL key the instant that video is displayed (during the memory test).
- Verify correct CMOS setup information. See table below.
- Insert bootable floppy disk into floppy drive or allow the system to boot from the hard drive.
- See VT1474 – EPIC-2 CMOS Setup Reference for more information.

Basic CMOS Configuration

```
+------------------------------------------------------------------------------+
|                  System Bios Setup – Basic CMOS Configuration                |
|            (C) 2004 General Software, Inc. All rights reserved               |
+--------------------------+---------------------+-----------------------------+
| DRIVE ASSIGNMENT ORDER:  | Date:>Jan 01, 2005  | Typematic Delay  : 250 ms   |
| Drive A: Floppy 0        | Time: 00 : 00 : 00  | Typematic Rate   : 30 cps   |
| Drive B: (None)          | NumLock:  Disabled  | Seek at Boot     : None     |
| Drive C: Ide 0/Pri Master +--------------------+ Show "Hit Del"   : Enabled  |
| Drive D: (None)          | BOOT ORDER:         | Config Box       : Enabled  |
| Drive E: (None)          | Boot 1st: Drive C:  | F1 Error Wait    : Enabled  |
| Drive F: (None)          | Boot 2nd: (None)    | Parity Checking  : (Unused) |
| Drive G: (None)          | Boot 3rd: (None)    | Memory Test Tick : Enabled  |
| Drive H: (None)          | Boot 4th: (None)    | Debug Breakpoints: (Unused) |
| Drive I: (None)          | Boot 5th: (None)    | Debugger Hex Case: Upper    |
| Drive J: (None)          | Boot 6th: (None)    | Memory Test :StdLo FastHi   |
| Drive K: (None)          +---------------------+-----------------+-----------+
| Boot Method: Boot Sector | ATA DRV ASSIGNMENT:  Sect  Hds  Cyls | Memory    |
+--------------------------+ Ide 0: 3 = AUTOCONFIG, LBA           |  Base:    |
| FLOPPY DRIVE TYPES:      | Ide 1: 3 = AUTOCONFIG, LBA           |   633KB   |
| Floppy 0: Not installed  | Ide 2: 3 = AUTOCONFIG, LBA           |  Ext:     |
| Floppy 1: Not installed  | Ide 3: 3 = AUTOCONFIG, LBA           |   503MB   |
+--------------------------+--------------------------------------+-----------+
```

Features Configuration

```
+------------------------------------------------------------------------------+
|                  System BIOS Setup – Features Configuration                  |
|            (C) 2004 General Software, Inc. All rights reserved               |
+------------------------------------+-----------------------------------------+
| System Management Mode   : Enabled | Graphical/Audio POST     : Disabled     |
| System Management BIOS   : Enabled | System Management Bus    : Disabled     |
| Console Redirection      : Auto    | Quick Boot               : Disabled     |
| Primary IDE UDMA         : Enabled | Secondary IDE UDMA       : Disabled     |
+------------------------------------+-----------------------------------------+
```

Custom Configuration

```
+---------------------------------------------------------------------------+
|                 System BIOS Setup - Advanced Configuration                |
|            (C) 2004 General Software, Inc. All rights reserved             |
+------------------------------------+--------------------------------------+
| PCI INT A Assignment   : IRQ 11    | PCI INT B Assignment    : IRQ 11     |
| PCI INT C Assignment   : IRQ 11    | PCI INT D Assignment    : IRQ 11     |
| COM1 (0x3F8) Enable/IRQ : IRQ4     | COM2 (0x2F8)Enable/IRQ  : IRQ3       |
| COM3 (0x3E8) Enable/IRQ : Disabled | COM4 (0x2E8)Enable/IRQ  : Disabled   |
| Parallel Port Mode     : SPP       | LPT1 (0x378)Enable/IRQ  : No IRQ     |
| Video device mode      : TFT 640   | Video refresh rate      : 60 Hz      |
| Video data width       : 24 bit    | Video panel type        : TFT        |
| Legacy USB support     : Enabled   | BIOS Extension          : Disabled   |
| OS type                : Other OS  | Digital I/O 14          : No IRQ     |
| Digital I/O 15         : No IRQ    | A/D Conversion Done     : No IRQ     |
| ISA IRQ 3              : Disabled   | ISA IRQ 4               : Disabled   |
| ISA IRQ 5              : Disabled   | ISA IRQ 10              : Disabled   |
| CPU Temp Thresh        : 100°C     | CPU Over Temp IRQ       : No IRQ     |
| Write Protect BIOS     : Disabled  |                                      |
+------------------------------------+--------------------------------------+
|                                    |                                      |
| CPU temp / Board temp   : 57°C/48°C|                                      |
|                                    |                                      |
+------------------------------------+--------------------------------------+
```

Shadow Configuration

```
+---------------------------------------------------------------------------+
|                System BIOS Setup - Shadow/Cache Configuration             |
|            (C) 2004 General Software, Inc. All rights reserved            |
+------------------------------------+--------------------------------------+
| Shadowing              : Chipset   | Shadow 16KB ROM at C000  : Enabled   |
| Shadow 16KB ROM at C400 : Enabled  | Shadow 16KB ROM at C800  : Disabled  |
| Shadow 16KB ROM at CC00 : Disabled | Shadow 16KB ROM at D000  : Disabled  |
| Shadow 16KB ROM at D400 : Disabled | Shadow 16KB ROM at D800  : Disabled  |
| Shadow 16KB ROM at DC00 : Enabled  | Shadow 16KB ROM at E000  : Enabled   |
| Shadow 16KB ROM at E400 : Enabled  | Shadow 16KB ROM at E800  : Enabled   |
| Shadow 16KB ROM at EC00 : Enabled  | Shadow 64KB ROM at F000  : Enabled   |
+------------------------------------+--------------------------------------+
```

Note: Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above**.**

Operating System Installation

The standard PC architecture used on the EPIC-2 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EPIC-2 Product Support web page at **http://www.VersaLogic.com/private/geckosupport.asp**.

Dimensions and Mounting

The EPIC-2 complies with all EPIC standards which provide for specific mounting hole and PC/104-*Plus* stack locations as shown in the diagram below.

Caution The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.
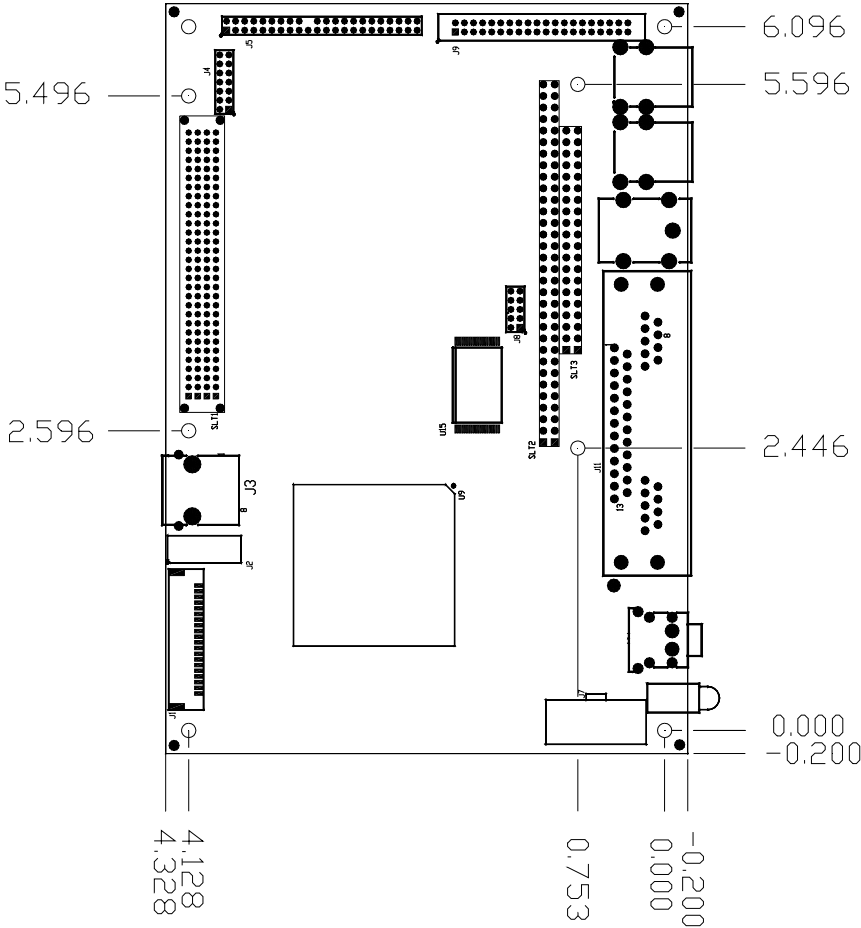
Figure 2. Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

SIDE PROFILE
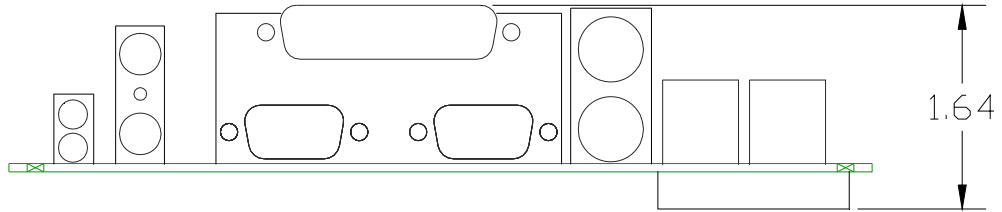
Figure 3. Side Profile

(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The EPIC-2 mounts on four hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using pan head screws.

Four additional standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and demated. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the PC/104 stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing. See page 11 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack.

Note: Standoffs and screws are available as part number VL-HDW-101.

STANDOFF LOCATIONS

Figure 4. Standoff Locations

External Connectors

CONNECTOR LOCATION DIAGRAM

Figure 5. Connector Location Diagram

External Connectors Bottom Side

CONNECTOR LOCATION DIAGRAM BOTTOM SIDE

Figure 6. Connector Location Diagram Bottom Side

External Connectors Peripheral Devices

CONNECTOR LOCATION DIAGRAM PERIPHERAL DEVICES
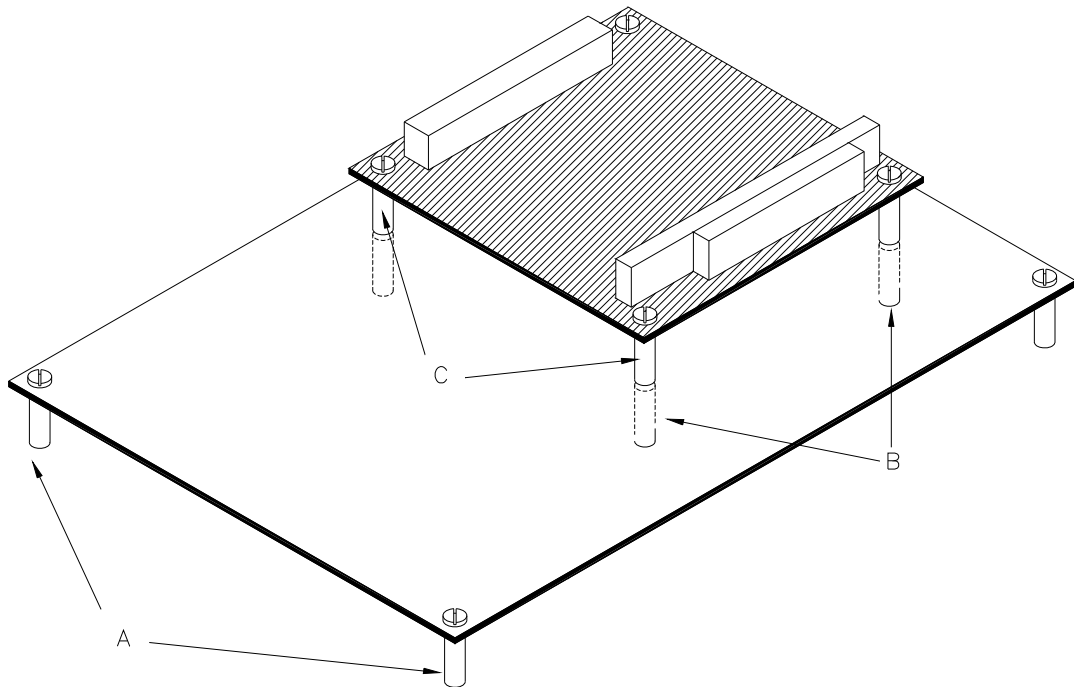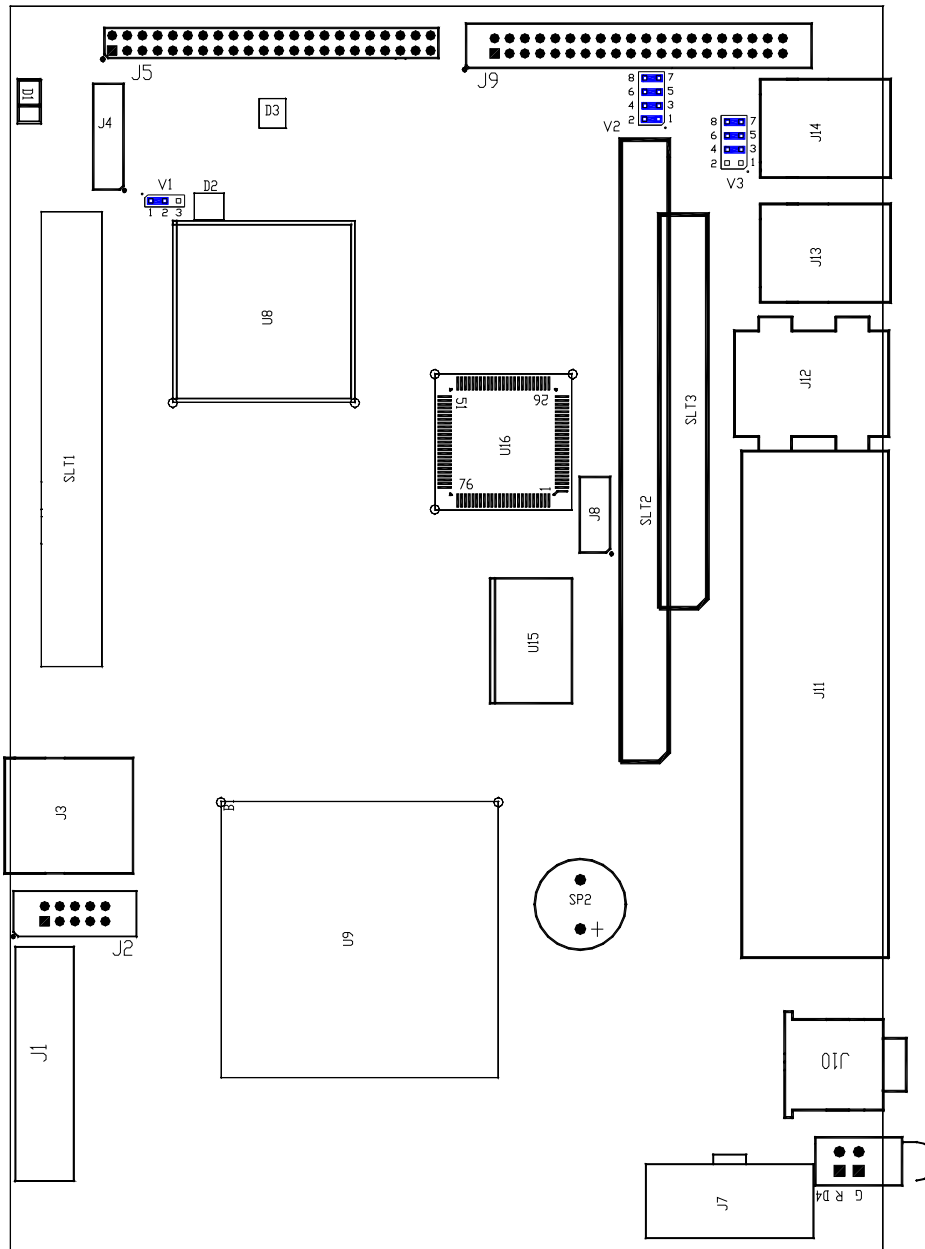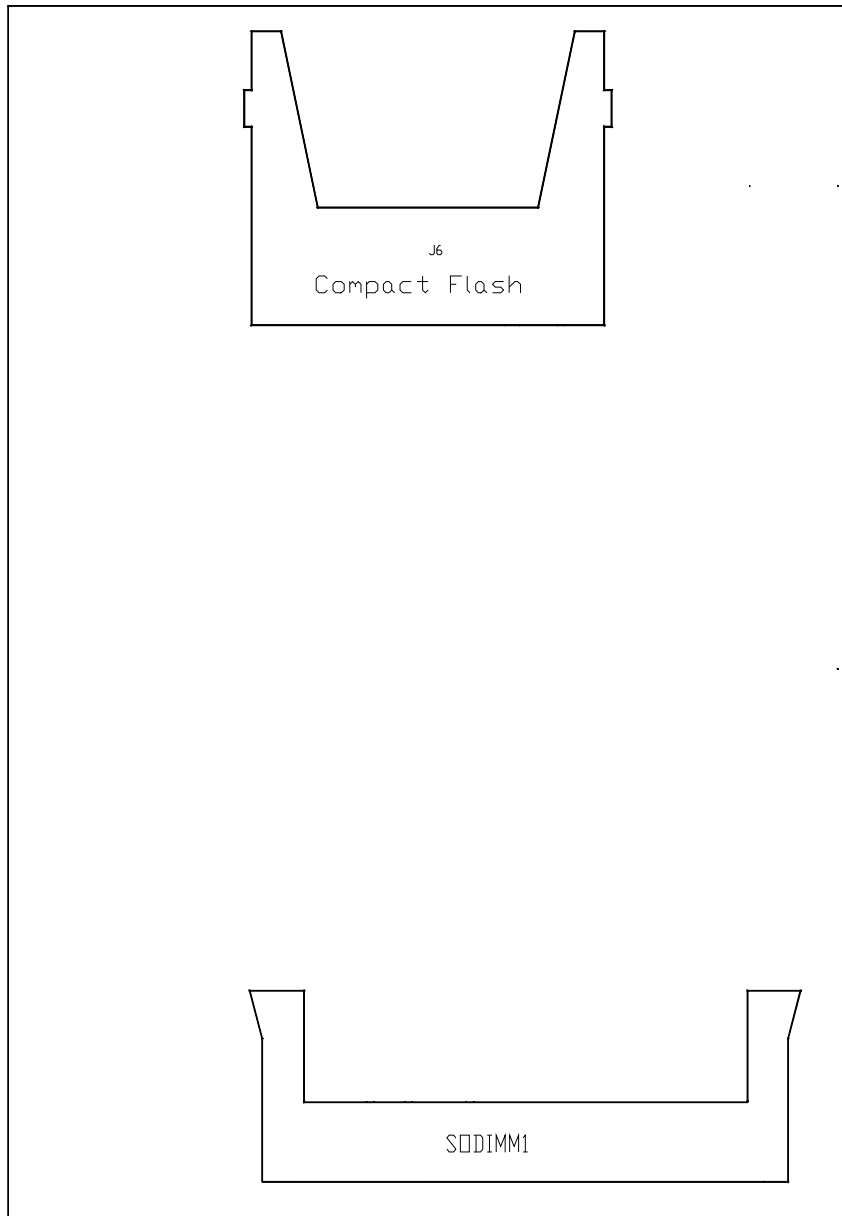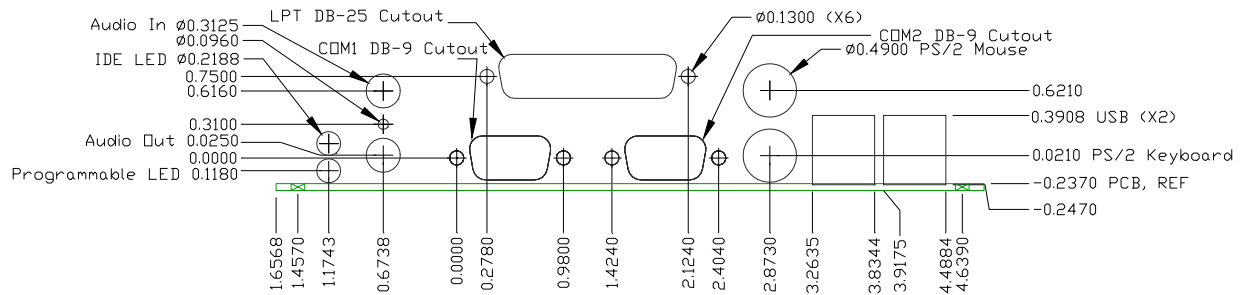

Figure 7. Connector Location Diagram Peripheral Devices

Connector Functions and Interface Cables

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Note: VersaLogic adapter cables are available in RoHS compliant and RoHS noncompliant versions. Compliance or noncompliance is indicated by the part number prefix. "CBR" indicates RoHS compliance. "CBL" indicates RoHS noncompliance. For applications that do not require RoHS compliance, either cable can be used.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page	*Pin 1 Location X Coord.	Y Coord.
J1	LVDS	Molex 51146-2000 Molex 50641-8041 Hirose DF19G-20S-1C Hirose DF19-2830SCFA JAE FI-S20S JAE FI-C3-A1-15000	CBL/CBR-2010 CBL/CBR-2011	18-bit TFT FPD using 20-pin Hirose conn. 18-bit TFT FPD using 20-pin JAE conn.	32	1.255	4.040
J2	Video Output	—	CBL/CBR-1007	1' 10-pin 2mm/15-pin VGA	31	1.530	4.150
J3	Ethernet	RJ-45 Crimp-on Plug	—	—	34	2.255	3.847
J4	Process JTAG DBUG	2mm			—	5.380	3.780
J5	IDE Hard Drive Channel 1	—	CBL/CBR-4404	1' 44-pin 2mm/two 44-pin 2mm	28	6.065	3.800
J6	CompactFlash	Type I or Type II CompactFlash	—	—	—	4.674	2.662
J7	Main Power Input	Molex 39-01-2100	CBL/CBR-2022	0.5 foot ATX to EPIC power cable	20	-0.035	0.260
J8	PLD Reprogramming Port	—	—	—	—	3.490	1.255
J9	Digital, Analog, COM3 , COM4	FCI 89947-740 ribbon FCI 90311-040 wire crimp	CBL/CBR-4004	12" 2mm 40-pin cable/board: dig/analog, I/O	38	6.050	1.815
J10	Audio In – Top Audio Out - Bottom	2mm Audio Jack	—	—	35	0.537	0.230
J11	LPT, COM1, COM2	DB25m, DB9f	—	—	24	3.314	0.436
J12	PS/2 mouse - Top, Keyboard - Bottom	PS/2	—	—	29	4.381	0.080
J13	USB	—	—	—	30	4.872	0.267
J14	USB	—	—	—	30	5.522	0.267

*   *Note:* .The PCB Origin is the mounting hole next to the LED, same as Figure 2.

Jumper Block Locations

JUMPERS AS-SHIPPED CONFIGURATION.
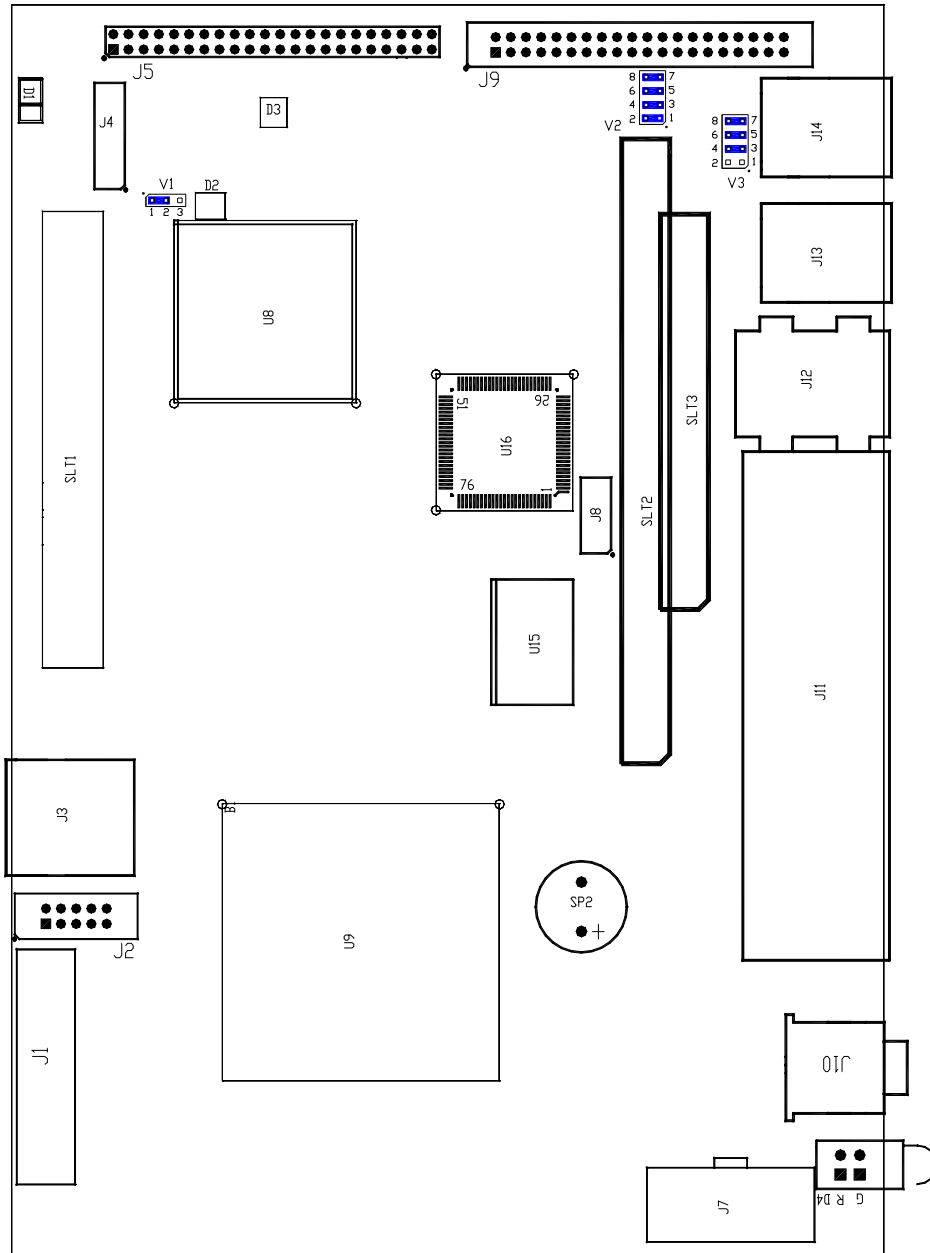
Figure 8. Jumper Block Location

JUMPER SUMMARY

Table 2: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1	**Battery Power Jumper** Erase CMOS Memory Standard Operation □ ■■ ■ ■ ■■ □ ● 1 2 3 ● 1 2 3	1-2 In	—
V2[1-2] [3-4]	**COM3 RS-422/485 Termination** In — Line A and B terminated with 127 Ohms Out — No termination 2 4 ● 1 3 1-2 is COM 3 RS-422 Transmit 3-4 is COM 3 RS-422 Receive, RS-485 Transmit and Receive	In	32
V2[5-6] [7-8]	**COM4 RS-422/485 Termination** In — Line A and B terminated with 127 Ohms Out — No termination 6 8 ● 5 7 5-6 is COM 4 RS-422 Transmit 7-8 is COM 4 RS-422 Receive, RS-485 Transmit and Receive	In	—
V3[1-2]	**SDMASTER** In — CompactFlash Master Device Out — CompactFlash Slave Device	Out	28
V3[3-4]	**General Purpose Input Bit** In — CPU reads bit as 1 Out — CPU reads bit as 0	In	23
V3[5-6]	**Video BIOS Selector** In — Primary Video BIOS selected Out — Secondary Video BIOS selected **Note** *The secondary Video BIOS is field-upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/geckosupport.asp for further information*	In	23
V3[7-8]	**System BIOS Selector** In — Run time system BIOS selected Out — Master system BIOS selected **Note** *The Run time System BIOS is field upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/geckosupport.asp for further information.*	In	21

Power Supply

POWER CONNECTORS

Main power is applied to the EPIC-2 through an EPIC-style 10-pin polarized connector.

See page 14 for connector pinout and location information.

Warning!   To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5VDC pins and all ground pins to prevent excess voltage drop.

Table 3: Main Power Connector Pinout

J7 Pin	Signal Name	Description
1*	GND	Ground
2	GND	Ground
3	GND	Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6**	NC	Not Connected
7	+5VDC	Power Input
8	+5VDC	Power Input
9	-12VDC	Power Input
10	GND	Ground

* Pin 1 is typically used in EPIC-style power cables as a PS-ON # signal. Since the EPIC-2 does not support soft-off, pin 1 is internally connected to ground.

** Pin 6 is typically used in EPIC style power cables as a 5VSB (5V Stand By) signal. Since the EPIC-2 does not support soft-off, pin 6 is an internal no connect.

Note: The +3.3VDC, +12VDC and -12VDC inputs on the main power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require the voltages.

POWER REQUIREMENTS

The EPIC-2 requires only +5 volts (±5%) for proper operation. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the EPIC-2 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, PS/2 keyboards typically draw their power directly from the EPIC-2, and driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning!   To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number T-HB3/5-3). The life expectancy under normal use is approximately 10 years.

Note: The EPIC-2 is designed to boot even with a dead or removed battery. See page 22 for further information.

System RAM

COMPATIBLE MEMORY MODULES

The EPIC-2 accepts one 200-pin SODIMM memory module with the following characteristics:

- Size   Up to 512 MB
- Voltage   2.5V
- Error Detection   Non-Parity
- Type   Unbuffered PC2100 (DDR266) or PC2700 (DDR333)

CPU

The Geode GX 500 microcontroller has a 32-bit, low-voltage AMD x86 microprocessor at its core. The maximum clock rate is 366 MHz actual, with 500 MHz performance. Extended temperature ("e") versions of the EPIC-2 are clocked down to 333 MHz actual, 450 MHz performance. It features 32 kb of level 1 cache, DDR SDRAM support, and an integrated display controller. The CPU has a typical power consumption of 1.1W.

CMOS RAM

CLEARING CMOS RAM

A jumper may be installed into V1[2-3] to erase the contents of the CMOS RAM and the Real-Time Clock. When clearing CMOS RAM: 1) Power off the EPIC-2. 2) Install the jumper on V1[2-3] and leave it for four seconds. 3) Move the jumper to back to V1[1-2]. 4) Power on the EPIC-2.

CMOS Setup Defaults

The EPIC-2 permits users to modify the CMOS Setup defaults. This allows the system to boot up with user-defined settings from cleared or corrupted CMOS RAM, battery failure or battery-less operation. All CMOS setup defaults can be changed, except the time and date. The CMOS Setup defaults can be updated with the BIOS Upgrade Utility. (See product support page for details)

> ***Warning!***   If the CMOS Setup defaults settings make the system unbootable and prevent the user from entering CMOS Setup, the EPIC-2 needs to be serviced by the factory.

DEFAULT CMOS RAM SETUP VALUES

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

USER DEFAULT CMOS RAM SETUP VALUES

To save CMOS Setup parameters to custom defaults, you will need a DOS bootable floppy with the Flash BIOS Update (FBU) utility on it. FBU is available from the BIOS Information page.

1. Boot the EPIC-2 and enter CMOS Setup by pressing Delete during the early boot cycle.
2. Change the CMOS parameters as desired and configure the floppy drive as the first boot device:

   ```
   Basic CMOS Configuration | BOOT ORDER | Boot 1st = Drive A:
   ```
3. Save the settings and exit CMOS Setup.
4. Reboot the system from the DOS boot floppy.
5. Run FBU and select Save CMOS contents. A file named CMOS.BIN is created and saved to the floppy.
6. Select the FBU option Load Custom CMOS defaults. A directory of the floppy is displayed.
7. Select the CMOS.BIN file and press the P key to program the new CMOS defaults.
8. Reboot from the hard disk. The custom CMOS parameters are now saved as defaults.

Real Time Clock

The EPIC-2 features a year 2000-compliant, battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real-time clock.

Serial Ports

The EPIC-2 features four on-board 16550-based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports. IRQ lines are chosen in the CMOS Setup.

COM3 and COM4 can be operated in RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 115k baud. IRQ lines are chosen in the CMOS Setup.

Each COM port can be independently enabled or disabled in the CMOS setup screen.

COM PORT CONFIGURATION

There are no configuration jumpers for COM1 and COM2 because they only operate in RS-232 mode.

Use the CMOS setup to select interrupts for the COM ports. Jumper block V2 is for termination of the RS-422/485 differential pairs. See the Jumper Summary for details on termination configuration.

COM3 / COM4 RS-485 MODE LINE DRIVER CONTROL

COM3 and COM4 can be configured in RS-422 or RS-485 interfaces. As an RS-422 interface two twisted pairs will be used per COM port, and for RS-485 only one twisted pair will be used, see Table 6.

To control the line drivers use board control register 1DAh.

RS-422/485 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
—	COM4TE485	COM4RE4XX	COM4TE422	—	COM3TE485	COM3RE4XX	COM3TE422

Table 4: RS-422/485 Bit Assignments

Bit	Mnemonic	Description
D7	—	**Reserved** — This bit has no function.
D6	COM4TE485	1 Enable COM4 RS-485 Transmitter on J9 pins 8 and 9. 0 Disable COM4 RS-485 Transmitter. ***Note** On an RS-485 system the transmitter needs to be turned off after transmission of the last byte so another device on the bus can communicate.*
D5	COM4RE4XX	1 Enable COM4 RS-485/422 Receiver on J9 pins 8 and 9. 0 Disable COM4 RS-485/422 Receiver. ***Note** For many systems this can be left always enabled. For RS-485 systems the same bytes transmitted will be received if this bit is enabled. This can be used for collision detection.*
D4	COM4TE422	1 Enable COM4 RS-422 Transmitter on J9 pins 6 and 7. 0 Disable COM4 RS-422 Transmitter.
D3	—	**Reserved** — This bit has no function.
D2	COM3TE485	1 Enable COM3 RS-485 Transmitter on J9 pins 3 and 4. 0 Disable COM3 RS-485 Transmitter. ***Note** On an RS-485 system the transmitter needs to be turned off after transmission of the last byte so another device on the bus can communicate.*
D1	COM3RE4XX	1 Enable COM3 RS-485/422 Receiver on J9 pins 3 and 4. 0 Disable COM3 RS-485/422 Receiver. ***Note** For many systems this can be left always enabled. For RS-485 systems the same bytes transmitted will be received if this bit is enabled. This can be used for collision detection.*
D0	COM3TE422	1 Enable COM3 RS-422 Transmitter on J9 pins 1 and 2. 0 Disable COM3 RS-422 Transmitter.

The following code example shows how to set the line driver for COM3 and COM4 to RS-422 mode. The control base address for the BCRs (Board Control Registers) is set to 1DAh.

```
MOV    DX,1DAH    ; POINT TO BCR[A]
MOV    AL,33H     ; SET TO RS-422 MODE
OUT    DX,AL      ; WRITE VALUE
```

SERIAL PORT CONNECTORS

See the *Connector Location Diagram* on pages 14, 15 and 16 for connector and cable information.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 5: Connectors J11 — Serial Port Pinout

COM1, COM2 DB9 J11 Pin	RS-232
1	DCD
2	RXD
3	TXD
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

Table 6: Connector J9 — Serial Port Pinout

	Gecko J9 Pin	RS-422	RS-485	I/O Board
COM3	1	TXD+	Unused	IO1
	2	TXD–	Unused	IO2
	3	RXD+	TXD/RXD+	IO3
	4	RXD–	TXD/RXD–	IO4
	5	GND	GND	GND1
COM4	6	TXD+	Unused	IO5
	7	TXD–	Unused	IO6
	8	RXD+	TXD/RXD+	IO7
	9	RXD–	TXD/RXD–	IO8
	10	GND	GND	GND1

Note: See page 38 for full J9 CBL/CBR-4004 pinout.

Parallel Port

The EPIC-2 includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via the CMOS setup screen. The LPT mode is also set via the CMOS setup screen.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 7: LPT1 Parallel Port Pinout

J11 Pin	Centronics Signal	Floppy Signal	Signal Direction
1	Strobe	DS0	Out
2	Data bit 1	INDEX	In/Out
3	Data bit 2	TRK0	In/Out
4	Data bit 3	WP	In/Out
5	Data bit 4	RDATA	In/Out
6	Data bit 5	DSKCHG	In/Out
7	Data bit 6	N.C.	In/Out
8	Data bit 7	MTR0	In/Out
9	Data bit 8	N.C.	In/Out
10	Acknowledge	DS1	In
11	Port Busy	MTR1	In
12	Paper End	WDATA	In
13	Select	WGATE	In
14	Auto feed	RPM	Out
15	Printer error	HDSEL	In
16	Reset	FDIR	Out
17	Select input	STEP	Out
18	Ground	GND	—
19	Ground	GND	—
20	Ground	GND	—
21	Ground	GND	—
22	Ground	GND	—
23	Ground	GND	—
24	Ground	GND	—
25	Ground	GND	—

PARALLEL PORT FLOPPY DISK

The parallel port on the EPIC-2 can be used as a floppy disk interface. Select "FDD" as the LPT mode in the CMOS setup and connect a floppy disk drive to the parallel port via the CBL/CBR-2501 cable to use this feature.
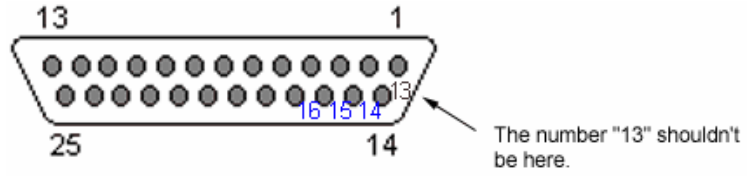
DB-25 FEMALE CONNECTOR

Figure 9. DB-25 Female Connector

The large outer numbers are correct. The manufacturer's marking for pin 13 is incorrectly placed.

IDE Hard Drive / CD-ROM Interfaces

The IDE interface is available to connect up to two IDE devices, such as hard disks, CD-ROM drives or CompactFlash. Connector J5 is the primary IDE controller with a 44-pin 2 mm connector. Use the CMOS setup to specify the drive parameters of the drive. If you use the on-board CompactFlash device, only one other IDE device can be connected to the IDE controller.

Cable length must be 18" or less to maintain proper signal integrity.

This interface supplies power to 2.5" IDE drives. If you are connecting a 3.5" drive to the interface (using the CBL/CBR-4405 44-pin to 40-pin IDE adapter), you must supply external power to the drive. The power cable attached to a 3.5" drive must be properly grounded so that motor current is not returned via the grounds in the data cable.

Table 8: IDE Hard Drive Connector Pinout

J5 Pin	Signal Name	EIDE Signal Name	Function	J5 Pin	Signal Name	EIDE Signal Name	Function
1	HRST*	Host Reset	Reset signal from CPU	23	HWR*	HOST IOW*	I/O write
2	Ground	Ground	Ground	24	Ground	Ground	Ground
3	IDE7	DATA 7	Data bit 7	25	HRD*	HOST IOR*	I/O read
4	HD8	DATA 8	Data bit 8	26	Ground	Ground	Ground
5	HD6	DATA 6	Data bit 6	27	IVORY	Ready	Wait control
6	HD9	DATA 9	Data bit 9	28	HAEN	ALE	Address latch enable
7	HD5	DATA 5	Data bit 5	29	IDACK	IDACK	DMA/Ack.
8	HD10	DATA 10	Data bit 10	30	Ground	Ground	Ground
9	HD4	DATA 4	Data bit 4	31	HINT	HOST IRQ14	IRQ14
10	HD11	DATA 11	Data bit 11	32	NC	NC	No Connection
11	HD3	DATA 3	Data bit 3	33	HA1	HOST ADDR1	Address bit 1
12	HD12	DATA 12	Data bit 12	34	CBLID	CBLID	Cable Identification
13	HD2	DATA 2	Data bit 2	35	HA0	HOST ADDR0	Address bit 0
14	HD13	DATA 13	Data bit 13	36	HA2	HOST ADDR2	Address bit 2
15	HD1	DATA 1	Data bit 1	37	HCS0*	HOST CS0*	Reg. access chip select 0
16	HD14	DATA 14	Data bit 14	38	HCS1*	HOST CS1*	Reg. access chip select 1
17	HD0	DATA 0	Data bit 0	39	LED	LED	LED
18	HD15	DATA 15	Data bit 15	40	Ground	Ground	Ground
19	Ground	Ground	Ground	41	5V	Power	Power
20	NC	NC	Key	42	5V	Power	Power
21	IDEDERQ	IDEDERQ	DMA Request	43	Ground	Ground	Ground
22	Ground	Ground	Ground	44	NC	NC	No Connection

Keyboard and Mouse

A standard PS/2 keyboard and mouse interface is accessible through connector J12.The 5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 9: Connector

J12 Pin Top	External Connector	Signal Description
4	MKPWR	Protected +5V
1	MSDATA	Mouse Data
3	GND	Ground
5	MSCLK	Mouse Clock
J12 Pin Bottom	**External Connector**	**Signal Description**
4	MKPWR	Protected +5V
1	KBDATA	Keyboard Data
3	GND	Ground
5	KBCLK	Keyboard Clock

Mouse Connector

Keyboard Connector

Programmable LED

D4 includes an output signal for attaching a software controlled LED. An on-board resistor limits the current to 15 mA when the circuit is turned on.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h. When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off. Refer to page 48 for further information:

```
LED On                  LED Off
MOV    DX,1D0H          MOV    DX,1D0H
IN     AL,DX            IN     AL,DX
OR     AL,80H           AND    AL,7FH
OUT    DX,AL            OUT    DX,AL
```

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code. The BIOS also flashes the LED in sync with "Beep Codes" when an error occurs.

Internal Speaker

The EPIC-2 uses a Piezo electric speaker.

Push-Button Reset

Connector J9 includes an input for a push-button reset switch. Shorting J9, pin 25 to ground causes the EPIC-2 to reboot.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

IDE LED

D4 outputs signal for IDE Activity LED. An on-board resistor limits the current to 15 mA when the circuit is turned on. D4 top LED is for IDE, D4 bottom LED is for the programmable LED.

USB Interface

The USB interface on the EPIC-2 is UHCI (Universal Host Controller Interface) compatible, which provides a common industry software/hardware interface. There are four USB 1.1 ports on J13 and J14 these are real world connectors.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Video Interface

An on-board video controller integrated into the chipset provides high performance video output for the EPIC-2.

CONFIGURATION

The EPIC-2 uses a shared-memory architecture. This allows the video controller to use 16 Megabytes of system DRAM for video RAM.

The EPIC-2 supports two types of video output, SVGA and LVDS Flat Panel Display.

VIDEO BIOS SELECTION

Jumper V3[5-6] can be removed to allow the system to boot off of the Secondary Video BIOS. Unlike the Primary Video BIOS, the Secondary Video BIOS can be reprogrammed in the field.

SVGA OUTPUT CONNECTOR

See the *Connector Location Diagram* on page 14 for pin and connector location information. An adapter cable, part number CBL-1007, is available to translate J2 into a standard 15-pin D-Sub SVGA connector.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 10: Video Output Pinout

J2 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	CRED	Red video	1
3	GND	Ground	7
4	CGRN	Green video	2
5	GND	Ground	8
6	CBLU	Blue video	3
7	GND	Ground	5
8	CHSYNC	Horizontal Sync	13
9	GND	Ground	10
10	CVSYNC	Vertical Sync	14

LVDS FLAT PANEL DISPLAY CONNECTOR

The integrated LVDS Flat Panel Display in the EPIC-2 is a ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 85 MHz.

The 3.3V power provided to pins 19 and 20 of J1 is protected by a 1 Amp fuse.

See the *Connector Location Diagram* on page 14 for pin and connector location information.

Table 11: LVDS Flat Panel Display Pinout

J1 Pin	Signal Name	Function
J1[1]	GND	Ground
J1[2]	NC	No Connection
J1[3]	LVDSA3	Diff. Data 3 (+)
J1[4]	LVDSA3#	Diff. Data 3 (−)
J1[5]	GND	Ground
J1[6]	LVFSCLK0	Differential Clock (+)
J1[7]	LVDSCLK0#	Differential Clock (−)
J1[8]	GND	Ground
J1[9]	LVDSA2	Diff. Data 2 (+)
J1[10]	LVDSA2#	Diff. Data 2 (−)
J1[11]	GND	Ground
J1[12]	LVDSA1	Diff. Data 1 (+)
J1[13]	LVDSA1#	Diff. Data 1 (−)
J1[14]	GND	Ground
J1[15]	LVDSA0	Diff. Data 0 (+)
J1[16]	LVDSA0#	Diff. Data 0 (−)
J1[17]	GND	Ground
J1[18]	GND	Ground
J1[19]	+3.3V	Protected Power Supply
J1[20]	+3.3V	Protected Power Supply

COMPATIBLE LVDS PANEL DISPLAYS

The following list of flat panel displays is reported to work properly with the integrated graphics video controller chip used on the EPIC-2:

Manufacture	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4"	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4"	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4"	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4"	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx141X01 series	14.1"	1024 x 768 18-bit	LVDS	TFT

Ethernet Interface

The EPIC-2 features an on-board Ethernet controller. This controller is the Intel 82551ER Fast Ethernet controller. While this controller is not NE2000-compatible, it is widely supported. Drivers are readily available to support a variety of operating systems. See VersaLogic website for latest OS support.

STATUS LED

The Ethernet controller has a two-colored LED connector to provide an indication of the Ethernet status as follows:

Green LED (Link/Activity)

- Solid ON   A link is established, and there is no network activity

- Blinking   A link is established, and there is network activity

- Solid OFF   No link is established or no cable is plugged in

Yellow LED (Speed)

- ON   Link mode is set to 100BASE-TX

- OFF   Link mode is set to 10BASE-T

ETHERNET CONNECTOR

A board-mounted RJ-45 connector is provided to make a connection with a Category 5 Ethernet cable. The 82551ER Ethernet controller autodetects 10BaseT/100Base-TX connections.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Audio

The audio interface on the EPIC-2 is implemented using the Analog Devices AD1981B Audio Codec. This interface is AC '97 2.x compatible. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the EPIC-2 product support page at **www.VersaLogic.com/private/geckosupport.asp.**

J10 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt "INTB#". The CMOS setup screen is used to select the IRQ line routed to INTB#.

The audio controller can be disabled within the CMOS setup. Accepts a 1/8" audio jack connector.

Table 12: Audio Connector

J10 Pin Top	Signal Name	Function
1	AUDINL	Line-In Left
2	AUDINR	Line-In Right
3	Ground	Ground
J10 Pin Bottom	**Signal Name**	**Function**
4	AUDOUTL	Line-Out Left
5	AUDOUTR	Line-Out Right
6	Ground	Ground

Watchdog Timer

A watchdog timer circuit is included on the EPIC-2 to reset the CPU if proper software execution fails or a hardware malfunction occurs.

ENABLING THE WATCHDOG

Bit D0 in I/O port 1D0h is used to enable or disable the watchdog from resetting the CPU on timer expiration. When changing the contents of the register, make sure not to alter the value of the other bits. The following procedure should be used when enabling the watchdog to prevent erroneous resets.

The following code example enables the watchdog reset:

```
        MOV    DX,1D2H   ;CLEAR BIT D2 (WDOGSTA) IN THE JSR REGISTER
        IN     AL,DX
        OR     AL,04H
        OUT    DX,AL

  LOOP: IN     AL,DX     ;LOOP WHILE BIT D2 (WDOGSTA) = 0
        AND    AL,04H
        JZ     LOOP
        IN     AL,DX     ;CLEAR BIT D2 (WDOGSTA) IN THE JSR REGISTER
        OR     AL,04H
        OUT    DX,AL

        MOV    DX,1D0H   ;ENABLE THE WATCHDOG (RESET MODE)
        IN     AL,DX
        OR     AL,01H
        OUT    DX,AL
```

NOTE: The watchdog is disabled when the EPIC-2 is powered on or reset.

DISABLING THE WATCHDOG

The watchdog may be disabled at any time by clearing the above mentioned bits; no special procedure is required.

REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1.0 sec minimum). Outputting a 5Ah to the *Watchdog Timer Hold-Off Register* at 1D1h resets the watchdog time-out period, see page 49 for additional information.

There is no provision for selecting a different timeout period using software.

The following code example refreshes the watchdog:

```
    MOV    DX,1D1H
    MOV    AL,5AH
    OUT    DX,AL
```

CPU Temperature Monitor

A thermometer circuit constantly monitors the die temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from fan or heat sink failure or excessive ambient temperatures.

The CMOS setup is used to set the temperature detection threshold. A status bit in the *Special Control Register* bit D5 if I/O port 1D0h, can be read to determine if the die temperature is above the threshold.

Contact the factory for information on clearing the status bit or reading and writing to the thermometer circuit. See page 48 for additional information.

Analog Input

The EPIC-2 analog input uses a 12-bit A/D converter that accepts up to eight single-ended input signals. The converter features fast 75 KSPS samples per seconds (KSPS) conversion time, with input range of 0 to +4.095V with 4096 steps at 0.001V each. A/D input impedance is 33 pF, so it expects low impedance source. Maximum input voltage is 4.395V (4.095V + 0.300V) and minimum input voltage -0.300V.

Warning!   Application of analog voltages greater than +4.395V can physically damage the converter.

Note: The A/D converter is not designed to accept high impedance signals. It requires low source impedance signals, in the range of 1500 ohms, to avoid data corruption from transient signals.

SOFTWARE CONFIGURATION

The EPIC-2 can be configured to issue an interrupt when the analog-to-digital converter has completed a conversion. IRQ selection is done in CMOS Setup.

EXTERNAL CONNECTIONS

Single-ended analog voltages are applied to connector J9 as shown in the following table.

Table 13: J9 Connector Pinout

J9 Pin	CBR-4004 J5 Pin	Interface	Signal		CBR-4004 Connector	CBR-4004 Pin
			RS-422	**RS-485**		
1	1	**COM3**	TXD+	Unused	**J1**	5 (IO1)
2	2		TXD–	Unused		4 (IO2)
3	3		RXD+	TXD/RXD+		3 (IO3)
4	4		RXD–	TXD/RXD–		2 (IO4)
5	5		GND	GND		1 (GND1)
6	6	**COM4**	TXD+	Unused	**J2**	5 (IO5)
7	7		TXD–	Unused		4 (IO6)
8	8		RXD+	TXD/RXD+		3 (IO7)
9	9		RXD–	TXD/RXD–		2 (IO8)
10	10		GND	GND		1 (GND1)
11	11	**Digital I/O**	Digital I/O 0		**J3**	5 (IO9)
12	12		Digital I/O 1			4 (IO10)
13	13		Digital I/O 2			3 (IO11)
14	14		Digital I/O 3			2 (IO12)
15	15		GND			1 (GND2)
16	16		Digital I/O 4		**J4**	5 (IO13)
17	17		Digital I/O 5			4 (IO14)
18	18		Digital I/O 6			3 (IO15)
19	19		Digital I/O 7			2 (IO16)
20	20		GND			1 (GND2)
21	21	**Digital I/O**	Digital I/O 8		**J6**	1 (IO17)
22	22		Digital I/O 9			2 (IO18)
23	23		Digital I/O 10			3 (IO19)
24	24		Digital I/O 11			4 (IO20)
25	25		Pushbutton Reset			5 (GND3)
26	26		Digital I/O 12		**J7**	1 (IO21)
27	27		Digital I/O 13			2 (IO22)
28	28		Digital I/O 14			3 (IO23)
29	29		Digital I/O 15			4 (IO24)
30	30		GND			5 (GND3)
31	31	**Analog In**	Analog Input 0		**J8**	1 (IO25)
32	32		Analog Input 1			2 (IO26)
33	33		Analog Input 2			3 (IO27)
34	34		Analog Input 3			4 (IO28)
35	35		AGND			5 (GND4)
36	36		Analog Input 4		**J9**	1 (IO29)
37	37		Analog Input 5			2 (IO30)
38	38		Analog Input 6			3 (IO31)
39	39		Analog Input 7			4 (IO32)
40	40		AGND			5 (GND4)

Warning!   Application of analog voltages greater than +4.395V can physically damage the converter. Such damage is not covered under warranty.

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

ANALOG CONTROL REGISTER

ACR (WRITE) 1D8h (or 1E8h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	—	A2	A1	A0

Table 14: Analog Control Register Bit Assignments

Bit	Mnemonic	Description
D7, D3	—	**Reserved** — These bits have no function.
D2-D0	A2, A1, A0	**Input Channel Address** — These bits select which input channel you wish to convert. **A2 A1 A0 Channel** 0 0 0 Channel 0 0 0 1 Channel 1 0 1 0 Channel 2 0 1 1 Channel 3 1 0 0 Channel 4 1 0 1 Channel 5 1 1 0 Channel 6 1 1 1 Channel 7

INDUSTRIAL I/O CONTROL REGISTER

IIOCR (READ/WRITE) 1D3H

D7	D6	D5	D4	D3	D2	D1	D0
DONE	—	—	—	—	—	DOEN1	DOEN0

Table 15: Industrial I/O Control Register Bit Assignments

Bit	Mnemonic	Description
D7	DONE	**Analog Input Conversion Complete** — This status bit is used to determine when it is alright to read data from the A/D converter. DONE = 0 — Conversion underway, data not yet available DONE = 1 — Analog input conversion has completed. Valid data is available to read from the ADCLO and ADCHI registers. Done value is reset to "0" when a new conversion is started. *Note This bit is cleared by reading either ADCHI or ADCLO registers or by writing to the ACR register.*
D6-D2	—	**Reserved** — These bits have no function.
D1	DOEN1	**Direction Control for Digital I/O Port** — This bit controls the input/output direction of the digital I/O signals DIO15 – DIO8. DOEN1 = 0 — Input DOEN1 = 1 — Output
D0	DOEN0	**Direction Control for Digital I/O Port** — This bit controls the input/output direction of the digital I/O signals DIO7 – DIO0. DOEN0 = 0 — Input DOEN0 = 1 — Output

ADC DATA **H**IGH **R**EGISTER

ADCHI (READ) 1D9h

D7	D6	D5	D4	D3	D2	D1	D0
—	—	—	—	AD11	AD10	AD9	AD8

The ADCHI register is a read register containing the upper four bits of data from the A/D conversion results. It is used in conjunction with the ADCLO register to read the complete 12-bit data word.

When reading data, it is normal convention to read the ADCLO register first, followed by the ADCHI register.

Table 16: ADCHI Bit Assignments

Bit	Mnemonic	Description
D7-D4	—	**Reserved** — These bits have no function.
D3-D0	AD11-AD8	**A/D Input Data (Most Significant Nibble)** — These bits contain data bits AD11 through AD8 of the conversion results. *Note These are read-only bits.*

ADC DATA **L**OW **R**EGISTER

ADCLO (READ) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

The ADCLO register is a read register containing the lower eight bits of data from the A/D conversion results. It is used in conjunction with the ADCHI register to read the complete 12-bit data word.

After a conversion is complete (as reported by the DONE bit in the 1D3h register) the ADCLO register should be read first, followed by the ADCHI register. A word-wide input instruction from the ADCLO register (in ax,dx) fetches data from both registers in the proper sequence.

The data registers are located on an even address boundary to facilitate efficient single-cycle reading of the A/D data.

Table 17: ADCLO Bit Assignments

Bit	Mnemonic	Description
D7-D0	ADCDATA	**A/D Input Data (Least Significant Byte)** — These bits contain data bits AD7 through AD0 of the conversion results. *Note These are read-only bits.*

BINARY FORMAT (0 TO +4.095V ONLY)

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 Volts (ground). All codes are considered positive.

The following formulas are used for calculating analog and digital values:

$$Digital = \left\lceil \frac{Analog}{Step} \right\rceil \qquad Analog = Step \text{ x } Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.001V

Sample values are shown in the following table.

Table 18: Binary Data Format

0 to +4.096V Input Voltage	Hex	Decimal	Comment
+4.096V	—	—	Out of range
+4.095V	0FFFh	4095	Maximum voltage
+2.048V	0800h	2048	Half scale
+1.024V	0400h	1024	Quarter scale
+0.001V	0001h	1	1 LSB
0.000000	0000h	0	Zero (ground input)

ANALOG INPUT CODE EXAMPLE

The following code example illustrates the procedure for reading analog voltage from channel 0:

```
        MOV    AL,00        ;Set channel 0
        MOV    DX,1D8
        OUT    DX,AL        ;Select channel 0 and begin conversion
LOOP:
        MOV    DX,1D3       ;
        In     AL, DX       : Read Done bit
        CMP    AL,00        : Check if set
        JZ     LOOP
        MOV    DX,1D9       : Read two 8-bit values
        IN     AL,DX
        MOV    AH,AL
        MOV    DX,1D8
        IN     AL,DX
```

Digital I/O Interface

The EPIC-2 includes a 16-channel digital I/O interface. The digital lines are grouped as two 8-bit bi-directional ports. The direction of each port is controlled by the DIOEN0 and DIOEN1 bits in the IIOCR register (see Industrial I/O Control Register), and each signal is pulled up to +5V with a 10K ohm resistor. The digital I/O ports are powered up in the input mode.

The 24 mA source/sink drive and short protected outputs are an excellent choice for industrial TTL interfacing.

For external connections, see Table 13.

INTERRUPT GENERATION

The EPIC-2 can be configured to issue interrupts on the transition (high to low or low to high) of DIO14 and DIO15. IRQ selection is done in CMOS Setup.

DIGITAL I/O DATA PORTS

DIOB1 (READ/WRITE) 1D5h

D7	D6	D5	D4	D3	D2	D1	D0
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8

DIOB0 (READ/WRITE) 1D4h

D7	D6	D5	D4	D3	D2	D1	D0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

Table 19: Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	DIO15 – DIO8 DIO7 – DIO0	**Digital I/O Data** — Data written to these register is driven onto the Digital I/O port signals when the port direction is set to output mode. When the port is in input mode, these bits reflect the input state of the signal lines. DIO = 0 Signal low (GND) DIO = 1 Signal high (+5V)

PC/104 Expansion Bus

EPIC-2 has limited support of the PC/104 bus. Most PC/104 cards will work but be sure to check the requirements of your PC/104 card against the list below.

PC/104 I/O SUPPORT

I/O ranges supported:

- 0x100-0x370 excluding the following ports:
- COM ports: COM1 (0x3F8-0x3FF), COM2 (0x2F8-0x2FF), COM3 (0x3E8-0x3EF), COM4 (0x2E8-0x2EF)
- LPT ports: LPT1 (0x378-0x37F)
- FDC ports: 0x3F0-0x3F7
- Digital I/O: 0x1D0-0x1E0
- Fixed disk controller: 0x1F0-0x1FF

Note: Rev 4.04 boards and later support 16-bit I/O transfers. On Rev 4.03 and earlier boards, all 16-bit I/O reads and writes were converted into two 8-bit cycles (low byte, then high byte) on the PC/104 bus.

PC/104 MEMORY SUPPORT

Memory ranges supported: CC000h-DBFFFh, 8-bit transfers only.

IRQ SUPPORT

The following IRQs are available on the PC/104 bus: IRQ 3, IRQ 4, IRQ 5, IRQ 10. Each of the four IRQs must be enabled in the CMOS setup screen before they can be used on the ISA bus.

DMA SUPPORT

The current revision of the board does not support PC/104 DMA.

Memory and I/O Map

MEMORY MAP

The lower 1 MB memory map of the EPIC-2 is arranged as shown in the following table.

Various blocks of memory space between C0000h and FFFFFh can be shadowed. The CMOS setup is used to enable or disable this feature.

Table 20: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
DC000h	DFFFFh	Reserved
D0000h	DBFFFh	PC/104
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System RAM

I/O MAP

The following table lists the common I/O devices in the EPIC-2 I/O map. User I/O devices should be added using care to avoid the devices already in the map as shown in the following table.

Table 21: On-Board I/O Devices

I/O Device	Standard I/O Addresses
Special Control Register	1D0h
Watchdog Hold-Off Register	1D1h
Jumper and Status Register	1D2h
Industrial I/O Control Register	1D3h
Digital I/O Data Register Byte 0	1D4h
Digital I/O Data Register Byte 1	1D5h
Analog Control / ADC Low Register	1D8h
ADC High Data Register	1D9h
Reserved	1E0h
Primary Hard Drive Controller	1F0h − 1F7h
COM4 Serial Port	2E8h − 2EFh
COM2 Serial Port	2F8h − 2FFh
LPT1 Parallel Port	378h − 37Fh
COM3 Serial Port	3E8h − 3EFh
Floppy Disk Controller	3F0h − 3F7h
COM1 Serial Port	3F8h − 3FFh

* User selectable via CMOS setup

Note: The I/O ports occupied by on-board devices are freed up when the device is disabled in the CMOS setup.

Interrupt Configuration

The EPIC-2 has the standard complement of PC type interrupts. Four non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines can be allocated as needed to PCI devices.

There are no interrupt configuration jumpers. All configuration is handled through the CMOS setup. The switches in Figure 10 indicate the various CMOS setup options. Closed switches show factory default settings.

Note: If your design needs to use interrupt lines on the PC/104 bus, IRQ5, and/or IRQ10 are recommended. (IRQ3 and IRQ4 are normally used by COM1 and COM2 on the main board)
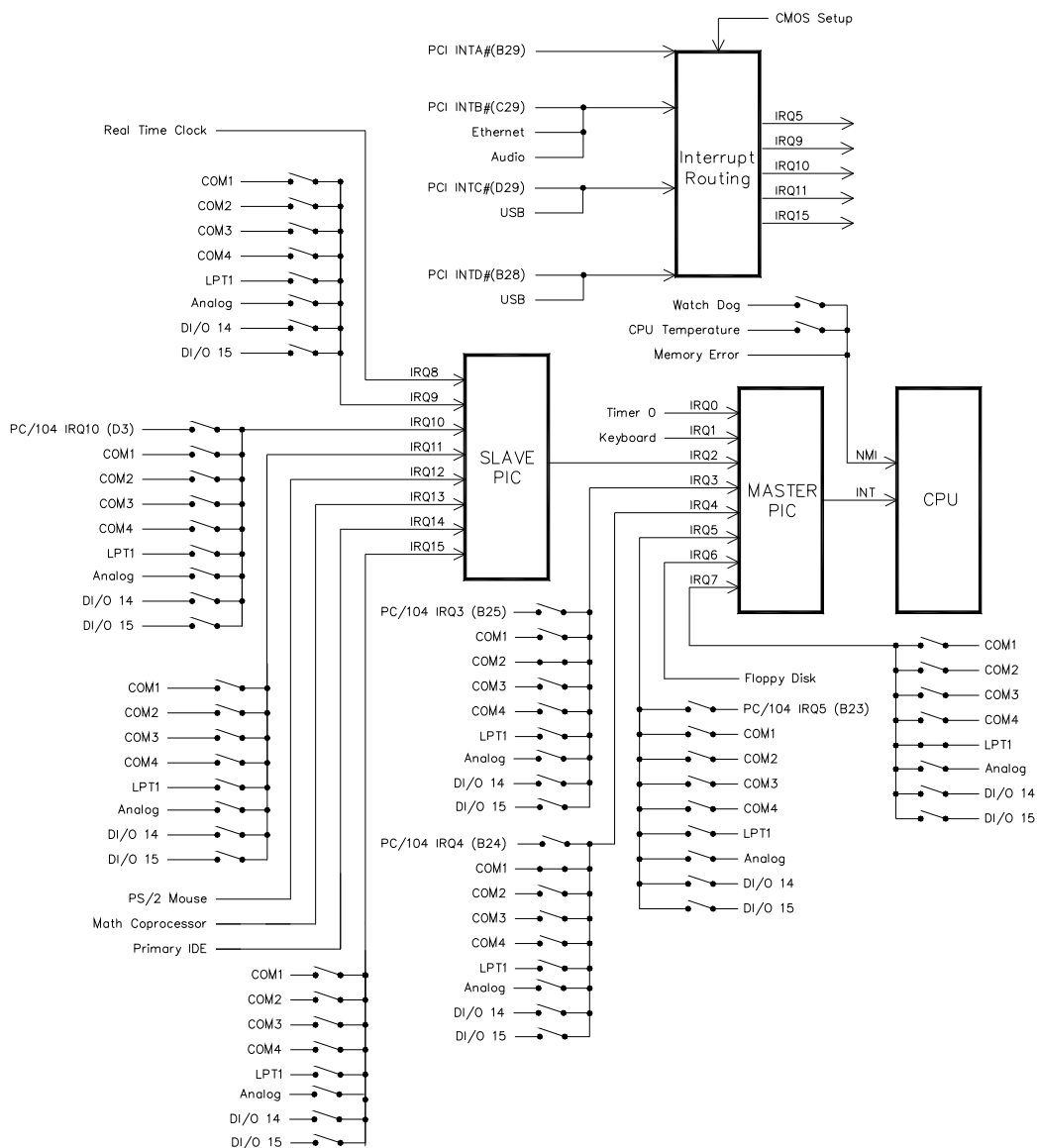

Figure 10. Interrupt Circuit Diagram

Special Control Register

SCR (READ/WRITE) 1D0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	Reserved	OVERTEMP	Reserved	Reserved	Reserved	Reserved	WDOG_RST

Table 22: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J4 LED = 0 Turns LED off LED = 1 Turns LED on
D6	Reserved	**Reserved** — This bit has no function.
D5	OVERTEMP	**Temperature Status** — Indicates CPU temperature. TEMP = 0 CPU temperature is below value set in the CMOS setup TEMP = 1 CPU temperature is above value set in the CMOS setup ***Note** This bit is a read-only bit.*
D4-D1	Reserved	**Reserved** — This bit has no function.
D0	WDOG_RST	**Watchdog Reset Enable** — Enables and disables the watchdog timer reset circuit WDOGEN = 0 Disables WDOGEN = 1 Enables

Revision Indicator Register

REVIND (READ ONLY) 1D1h

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	EXT	REV1	REV0

This register is used to indicate the revision level of the EPIC-2.

Bit	Mnemonic	Description
D7-D3	PC4-PC0	**Product Code** — These bits are hard-coded to represent the product type. The EPIC-2 always reads as 00011. Other codes are reserved for future products. **PC4 PC3 PC2 PC1 PC0 Product Code** `0    0    0    1    1      EPIC-2` ***Note*** *These bits are read-only.*
D2	EXT	**Extended Temperature** — Indicates operating temperature range. EXT = 0 Standard temperature range EXT = 1 Extended temperature range ***Note*** *These bits are read-only.*

D1-D0	REV1-REV0	**Revision Level** — These bits represent the EPIC-2 circuit revision level.
		REV1 REV0 Revision Level
		`0        0      Initial product release, Rev 3.xx`
		`0        1      Rev 4.xx`
		`1        0      Rev 4.03 and higher`
		Note *These bits are read-only.*

Possible REVIND values are:

`00011000`	EPIC-2 Rev 2.xx and 3.xx
`00011001`	EPIC-2 Rev 4.00, 4.01, 4.02 "b" and "c" versions
`00011101`	EPIC-2 Rev 4.00, 4.01, 4.02 "e" version (D2 = Extended temperature bit)
`00011010`	EPIC-2 Rev 4.03 and above "b" and "c" versions
`00011110`	EPIC-2 Rev 4.03 and above "e" version (D2 = Extended temperature bit)

Watchdog Timer Hold-Off Register

WDHOLD (WRITE ONLY) 1D1h

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the EPIC-2 board to reset the CPU if proper software execution fails or a hardware malfunction occurs. The watchdog timer is controlled by the SCR.

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1000 ms minimum). Writing 5Ah to WDHOLD resets the watchdog timeout period.

Jumper and Status Register

JSR (READ/WRITE) 1D2h

D7	D6	D5	D4	D3	D2	D1	D0
GPI	VB-SEL	SB-SEL	Reserved	SDMASTER	WDOG_STA	DINTHI_REQ	DINTLO_REQ

Table 23: Jumper and Status Register Bit Assignments

Bit	Mnemonic	Description
D7	GPI	**General Purpose Input** — Indicates the status of jumper. GPI = 0 Jumper Out GPI = 1 Jumper In ***Note*** *This is a read-only bit.*
D6	VB-SEL	**Video BIOS Selection** — Indicates the status of jumper. VB-SEL = 0 Jumper out, Secondary Video BIOS selected. VB-SEL = 1 Jumper in, Primary Video BIOS selected. ***Note*** *This is a read-only bit.*
D5	SB-SEL	**System BIOS Selection** — Indicates the status of jumper. SB-SEL = 0 Jumper out, Master System BIOS selected. SB-SEL = 1 Jumper in, Run Time System BIOS selected. ***Note*** *This is a read-only bit.*
D4	Reserved	**Reserved** — This bit has no function.
D3	SDMASTER	
D2	WDOG_STA	**WDOG STATUS** — Indicates if the watchdog timer has expired WDOGSTAT = 0 Timer has not expired WDOGSTAT = 1 Timer has expired ***Note*** *Clear bit by writing a 1 to it.*
D1	DINTHI_REQ	**Digital Interrupt High** — Indicates if a transition was detected on DIO 15 0 = No Transition Detected 1 = Transition Detected ***Note*** *Clear bit by writing a 1 to it.*
D0	DINTLO_REQ	**Digital Interrupt Low** — Indicates if a transition was detected on DIO 14 0 = No Transition Detected 1 = Transition Detected ***Note*** *Clear bit by writing a 1 to it.*

Appendix A — Other References

A

PC Chipset *GX 500 Chipset*	[Advanced Micro Devices](http://www.amd.com/us-en/), (http://www.amd.com/us-en/)
Ethernet Controller *Intel 82551ER*	[Intel Corporation](http://www.intel.com/design/index.htm) (http://www.intel.com/design/index.htm)
Video Controller	In chipset
PC/104 Specification	[VersaLogic Corporation](www.VersaLogic.com) (www.VersaLogic.com)
PC/104-*Plus* Specification	[VersaLogic Corporation](www.VersaLogic.com) (www.VersaLogic.com)
General PC Documentation *The Programmer's PC Sourcebook*	[Microsoft Press](http://www.microsoft.com/learning/books/) (http://www.microsoft.com/learning/books/)
General PC Documentation *The Undocumented PC*	[Powell's Books](http://www.powells.com/) (http://www.powells.com/)