MAX II Device Family

Errata Sheet

Introduction

This errata sheet provides updated information on MAX® II devices, addresses known device issues, and includes a workaround for those issues. Refer to Table 1.

Table 1. MAX II Device Family Issues

Issue	Affected Devices	Fixed Devices
Failed power-up into user mode for slow VCCINT rise times or VCCINT rise profiles with dips or noise near the power-on reset (POR) trip voltage.	EPM240 revision F and earlier EPM240G revision G and earlier EPM570 revision C and earlier EPM570G revision D and earlier EPM1270/1270ES revision G and earlier EPM1270G revision H and earlier EPM2210 revision C and earlier EPM2210G revision D and earlier	EPM240 revision H and later EPM240G revision I and later EPM570 revision E and later EPM570G revision F and later EPM1270 revision I and later EPM1270G revision J and later EPM2210 revision E and later EPM2210G revision F and later *(1)*
Extreme AC current activity can cause the V_{CCINT} POR brown-out trigger voltage to rise up to 1.7-V during DEV_OE de-assertion or before in-system programming.	EPM2210G Devices EPM1270G Devices	*(2)*
The user flash memory (UFM) block does not support program/write or erase operations from the logic array interface.	EPM1270 ES Devices	EPM1270 Production Devices
The optional Schmitt trigger inputs may glitch for falling input signal edge rates greater than 1 μs.	EPM1270 ES Devices	EPM1270 Production Devices
The UFM block optional oscillator output port may exhibit a single high or low pulse after power-up	EPM1270 ES Devices	EPM1270 Production Devices
The 144-pin thin quad flat pack (TQFP) package (T144) may exhibit glitches on the TCK Joint Test Action Group (JTAG) input pin for falling edge rates slower than 50 ns.	EPM1270 ES Devices	EPM1270 Production Devices
May not operate for V_{CCINT} brown-out conditions at or below 2.1 V.	EPM1270 ES Devices	EPM1270 Production Devices
Does not support Serial Vector File (**.svf**) format programming.	EPM1270 ES Devices	EPM1270 Production Devices

Table 1. MAX II Device Family Issues (Continued)

Issue	Affected Devices	Fixed Devices
EPM1270 engineering sample (ES) devices are not compatible with EPM1270 production device Programming Object Files (**.pof**).	EPM1270 ES Devices	*(3)*

Notes to Table 1:
(1)   See the "MAX II Power-up Issue"section for information on distinguishing revision codes.
(2)   Altera is offering permanent recommendations and workarounds for this issue.
(3)   This issue is a permanent programming file compatibility restriction.

MAX II Power-up Issue

The MAX II devices may not power-up and enter user mode correctly for either of the following conditions:

1. V_{CCINT} rises slower than the times shown in Table 2.

2. V_{CCINT} rise profile exhibits any non-monotonic dips or noise within the voltage regions shown in Table 2.

This power-up issue is only affected by the V_{CCINT} supply; V_{CCIO} rise times or profiles do not affect the MAX II device behavior for this issue. This issue affects all MAX II devices shown in Table 1.

The failed power-up condition results in all I/O pins remaining tri-state with weak pull-up resistors even though V_{CCINT} has been fully powered. While in this state, the JTAG port is unresponsive for programming or boundary scan operations. User mode operation does not begin unless V_{CCINT} power to the MAX II device is recycled.

To ensure successful power-up, Altera recommends (as shown in Table 2) that you provide a sufficient rise time with a monotonic V_{CCINT} rise profile that contains no dips within the voltage windows.

Table 2. Recommended V_{CCINT} Rise Times and V_{CCINT} Noise/Dip Free Window

Device and VCCINT Operating Voltage	Recommended V_{CCINT} Rise Time *(1)*	Recommended POR Dip/Noise Free Window
MAX II (3.3V V_{CCINT})	<= 1.0 ms	1.5-1.8V
MAX II (2.5V V_{CCINT})	<= 750 µs	1.5-1.8V

Table 2. Recommended V_{CCINT} Rise Times and V_{CCINT} Noise/Dip Free Window (Continued)		
Device and VCCINT Operating Voltage	**Recommended V_{CCINT} Rise Time** *(1)*	**Recommended POR Dip/Noise Free Window**
MAX IIG	<= 540 µs	1.3-1.65V

Note to Table 2:

(1) Rise times are measured from 10% to 90% of the stead-state operating voltage.

The MAX II POR circuitry is enhanced in later revisions to withstand non-monotonic, slow rise times in the revision codes that are shown in Table 1. The die revision is identified by the alphanumeric character (Z) before the fab code (first two alphanumeric characters) in the data code printed on the top side of the device. Figure 1 shows a MAX II device's top side date code.

Figure 1. MAX II Device Top Side

A Xβ*Z* ## ####

Die Revision

EPM2210G & EPM1270G Brown-out Voltage Issue

The POR circuitry monitors V_{CCINT} (but not V_{CCIO}) voltage to detect brown-out conditions. During normal user-mode operation, the POR circuit resets the SRAM configuration and tri-states the device I/O pins when V_{CCINT} falls approximately to or below 1.4 V. This POR circuit brown-out trigger voltage rises to 1.55 V on MAX IIG devices when the optional DEV_OE feature/pin is de-asserted or during in-system programming.

For more information on POR trip voltages and diagrams, see the *Hot-Socketing & Power-On Reset in MAX II Devices* chapter of the *MAX II Handbook*.

For EPM2210G and EPM1270G devices, if the AC switching current on the device's V_{CCINT} supply (I_{CCINT}) is more than the thresholds shown in Table 3 immediately before DEV_OE de-asserts (tri-state all I/O pins) or before in-system programming begins, the brown-out trigger voltage can rise as high as 1.7 V. This value is near the minimum operating voltage (1.71 V) of the 1.8-V EPM2210G and EPM1270G devices and can lead to unintended device reset during user-mode operation or a failed in-system programming attempt. I_{CCINT} is a function of logic element (LE)

utilization, clock frequency, and toggle factors. You can estimate the I_{CCINT} value by using the MAX II PowerPlay Early Power Estimator and/or the Quartus® II Power Analyzer.

Table 3. EPM2210G & EPM1270G I_{CCINT} Thresholds for Brown-Out Trigger Voltage Issue with DEV_OE & In-System Programming		
Device	Current Threshold	Units
EPM2210G	500	mA
EPM1270G	300	mA

For DEV_OE use with EPM2210G and EPM1270G devices, you should only use this feature if you can guarantee your design's I_{CCINT} is less than the thresholds shown in Table 3. When enabled by the Quartus II software, the DEV_OE feature does not use global resources but instead uses dedicated circuitry to control the output enable on all design I/O pins. For designs that cannot guarantee I_{CCINT} is less the threshold, you can use one of the four global signals to control device-wide output enable (OE) control. Using a global signal OE instead of the DEV_OE pin prevents the increase in POR trip voltage. The global signal OE requires that you instantiate a tri-state buffer and connect an OE signal to all the I/O pins in your design and assign the OE pin to a global signal in the Quartus II software.

For in-system programming with EPM2210G and EPM1270G devices, you should only use this feature if you can guarantee I_{CCINT} is less than the threshold shown in Table 3 for the running design immediately before in-system programming begins. For designs that can operate with I_{CCINT} greater than the threshold, you must either ensure within the system that the AC activity of the EPM2210G or EPM1270G device is reduced before in-system programming begins or instead use the real-time ISP feature. The real-time ISP feature does not raise the POR brown-out trigger voltage, thus it will not be susceptible to failed in-system programming during high switching current conditions. Using real-time ISP means the design continues to run during the in-system programming process.

For more information on the real-time ISP feature, see the *Using Real-time ISP & ISP Clamp* chapter of the *MAX II Handbook*.

EPM1270 ES Device Issues

The following issues and support constraints affect the MAX II EPM1270 ES devices:

- UFM block does not support program/write or erase operations from the logic array interface

- UFM block optional oscillator output port can exhibit a single high or low pulse after power-up
- Optional Schmitt trigger inputs may glitch for falling input signal edge rates greater than 1 µs
- 144-Pin TQFP package (T144) devices may exhibit glitches on the TCK JTAG input pin for falling edge rates slower than 50 ns
- May not operate for V_{CCINT} brown-out conditions at or below 2.1 V
- Do not support SVF format programming
- Are not compatible with the EPM1270 production device POF

☞ All of the device issues listed above are corrected in production EPM1270 devices.

UFM Block Logic Array Interface Support

The EPM1270 ES UFM block does not support write/program and erase operations from the logic array interface. The EPM1270 ES UFM block does support read operations from the logic array interface. The UFM can still be initialized or programmed through the JTAG interface using the Quartus II software with POF, Jam™ (**.jam**), or Jam Byte-Code (**.jbc**) files.

When using the altufm megafunction to instantiate the UFM block, the Quartus II software issues an error for the following cases:

- For the interface protocol, choosing **None** in the MegaWizard® Plug-In Manager (called the altufm_none megafunction) and connecting the program or erase ports of your instantiation to signals or pins in your design results in a compilation error.
- If you choose **Parallel** or **Serial Peripheral Interface (SPI)** in the MegaWizard® Plug-In Manager (called the altufm_parallel and altufm_spi megafunctions), the read/write option results in a compilation error. The read-only option will compile successfully.

☞ Production devices will fully support the UFM erase and program/write operations from the logic array.

UFM Block Oscillator Output Port Pulse

The EPM1270 ES device's optional UFM oscillator (OSC) output port, may pulse once (high or low) at power-up when first entering into user mode even though the oscillator enable port (OSCENA) is de-asserted at power-up in the design. The OSC output can be ANDed with the OSCENA port in the design to ensure that this port starts clocking when expected after power-up.

If the `OSCENA` port is asserted at the power-up condition in the design, the `OSC` output port does not exhibit a high or low pulse, but instead immediately starts clocking upon entry into user mode. For the asserted or de-asserted `OSCENA` power-up possibilities, it is undetermined whether the `OSC` output starts with a rising or falling edge. You should assume an unknown "X" on the `OSC` output port for all power-up conditions in your design with EPM1270 ES devices.

☞   Production devices do not exhibit the high or low pulse after power-up for the de-asserted `OSCENA` signal. For these devices, `OSC` stays high at power-up and does not clock until enabled with `OSCENA`.

Schmitt Trigger Slow Falling Input Edge Glitch

The Schmitt trigger input buffer is an optional feature on each I/O pin in MAX II devices to help maximize noise immunity on input pins. For EPM1270 ES devices, the 3.3-V or 2.5-V Schmitt trigger input option may glitch when driven by high-to-low signal transitions with fall times greater than 1 μs. Low-to-high signal transitions are not susceptible to glitch and reliably accept signals with rise times up to 200 ms.

The workaround to improve the Schmitt trigger falling edge input performance beyond 1-μs fall times is to enable the programmable input delay for that particular pin. Enabling the programmable input delay for the input pin allows the Schmitt trigger to accept fall times up to 200 ms. The programmable input delay adds a delay to the input delay path of ~2.1 ns for -4 speed grade and ~2.6 ns for -5 speed grade. This option can be set in the Assignment Editor (Assignments menu) on a pin-by-pin basis. The procedure to set this in the Quartus II software for a pin is shown below:

1. Select input pin name in the design file.

2. Right-click and select **Locate in Assignment Editor**.

3. Double-click the cell under Assignment Name and select **Input Delay from Pin to Internal Cells** in the drop-down list.

4. Double-click the **Value** cell to the right of the assignment name just made and enter 1.

5. Click **Save** (File menu).

This procedure turns on the input delay for the selected input pin.

☞ Production devices do not exhibit this input glitch for slow input fall times greater than 1 μs.

144-Pin TQFP Package TCK JTAG Input Glitching

The EPM1270 ES device in the 144-pin TQFP package can exhibit a high pulse glitch on the TCK input as a result of coupling from the adjacent TDO output pin. This can lead to double clocking and failed boundary scan and in-system programming operations. The TCK input is susceptible to high pulse glitches when its input signal fall time is greater than 50 ns for 3.3-V or 2.5-V V_{CCIO}. The JTAG pin I/O voltage is controlled by the bank 1 V_{CCIO} (V_{CCIO1}). The I/O voltage for Altera download cables is determined by pin 4 of the 10-pin header. This affects the voltage level of TCK driving the MAX II device. See the respective Altera download cable data sheet for more information.

This issue can be avoided by ensuring that the download cable or third-party programming/JTAG hardware supplies a TCK fall time less than 50 ns when driving the combined load capacitance of the cable, JTAG header, and trace for TCK.

Table 4 shows the approximate TCK fall times of the Altera download cables with no load. All the cables shown exhibit fall times less than 50 ns for no load conditions.

Table 4. Altera Download Cable TCK Fall Times	*Notes (1)*, *(2)*	
Altera Download Cable	**3.3-V Fall Times**	**2.5-V Fall Times**
USB Blaster	2	7
Byteblaster™ II Cable	12	20
ByteblasterMV™ Cable	25	*(3)*
MasterBlaster™ Cable	15	*(3)*

Notes to Table 4:
(1) Numbers are approximate and do not represent specifications.
(2) This is the edge rate at the cable edge connector before driving the load of the board JTAG header and board trace.
(3) These cables do not support 2.5-V operation.

If using third-party tool hardware or if excessive loading on TCK does not meet the 50 ns fall time requirement for EPM1270 ES devices, Altera recommends that you add a buffer device with sufficient edge rates to buffer TCK, TDI, and TMS near the EPM1270 ES device.

☞ Production devices do not exhibit this TCK glitch.

POR & Brown-Out Reset Voltage Levels

EPM1270 devices have POR circuits to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic maintaining tri-state of the I/O pins before and during this process. When the EPM1270 device enters user mode, the POR circuit releases the I/O pins to user functionality and continues to monitor the V_{CCINT} (not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CCINT} voltage sag below the EPM1270 operational level during user mode, the POR circuit resets the device and re-triggers an SRAM download. For EPM1270 ES devices, the POR re-trigger voltage level for a V_{CCINT} sag or brown-out condition, can be as high as 2.1 V, allowing for 275 mV of V_{CCINT} sag below the 2.375 V minimum. EPM1270 ES device users should ensure that the power supply noise does not lead V_{CCINT} to dip or ring at or below 2.1 V.

☞ Production devices have a V_{CCINT} POR re-trigger voltage for brown-out conditions down to 1.4 V.

Also, during power-up, production devices have a lower POR release voltage and increased configuration time (t_{CONFIG}) compared to EPM1270 ES devices. The *MAX II Handbook* specification for instant-on time (t_{CONFIG}) is referenced from 2.375-V minimum V_{CC}. Actual device operation begins before this specified worst-case period of time and voltage because the POR release voltage for internal configuration occurs below 2.375 V. This actual configuration start voltage and the t_{CONFIG} time differs between EPM1270 ES and EPM1270 production devices. Table 5 shows the POR release and trip voltages and t_{CONFIG} for EPM1270 production and ES devices.

| Table 5. t_{CONFIG}, POR Release, & V_{CCINT} Brown-Out Voltage in EPM1270 ES & Production Devices			
Device	t_{CONFIG}	**POR Release Voltage During Power-Up** (1)	**POR Trip Voltage During Brown-Out** (1)
EPM1270 (ES)	200 μs	2.2 V	2.1 V
EPM1270 (Production)	300 μs	1.7 V	1.4 V

Note to Table 5:
(1)   Numbers are approximate and do not represent specifications.

Figure 2 shows the relative power-up and the power-down characteristics of EPM1270 ES devices compared to EPM1270 production devices.

Figure 2. Power-Up & Down Characteristics of EPM1270 ES & Production Devices   *Notes (1), (2), (3)*
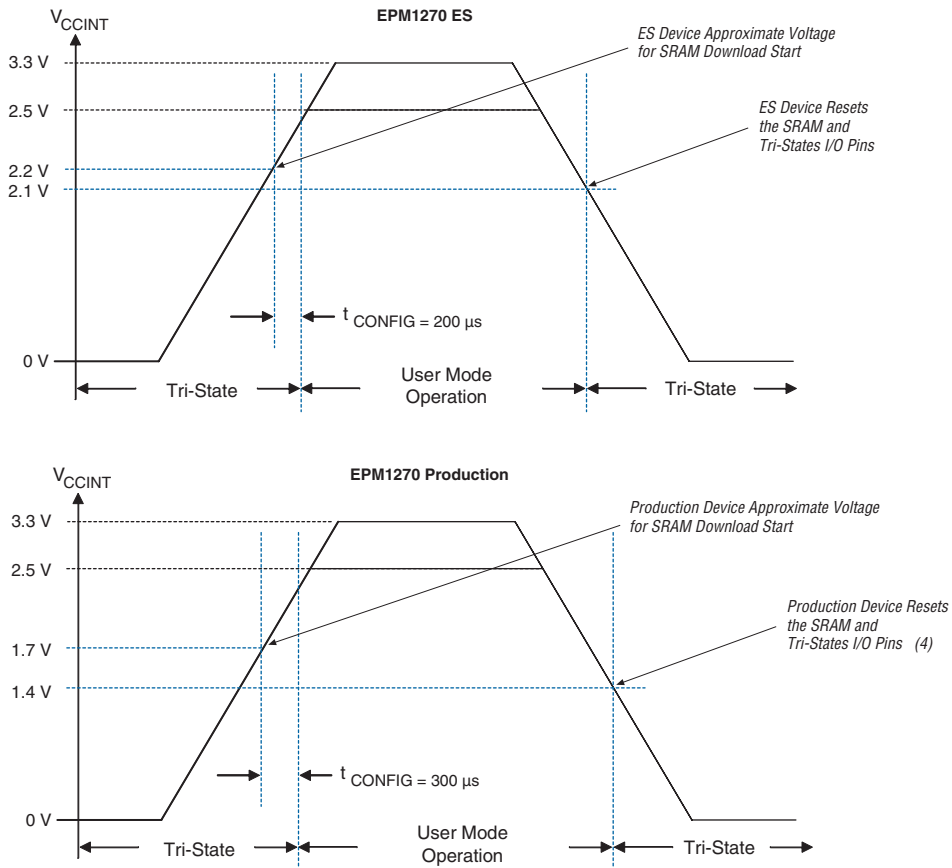
Notes to Figure 2:
(1)   Time scale is relative.
(2)   Figure 2 assumes all V_{CCIO} banks power simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.
(3)   Voltages for t_{CONFIG} are approximations of actual device behavior. The t_{CONFIG} specification is still referenced from 2.375 V.
(4)   This brown-out POR trigger voltage rises to 1.55 V during `DEV_OE` de-assertion or in-system programming.

Serial Vector File Support

EPM1270 ES devices do not support SVF format for programming. The devices do support POF, Jam, and JBC file formats for programming with the Quartus II software.

☞ Production devices will support SVF format and programming flow.

Device Programming Object File Compatibility

The POF generated for EPM1270 ES devices is compatible with EPM1270 ES and EPM1270 production devices. Recompilation and regeneration of POFs is not required when moving from EPM1270 ES to EPM1270 production devices. However, POFs generated for EPM1270 production devices do not support ES devices. Therefore, if you are using an EPM1270 ES device, you must be sure to use a POF generated for the EPM1270 ES device in the Quartus II software. Table 6 shows POF compatibility between ES and production devices.

Table 6. POF Compatibility Between EPM1270 ES & Production Devices	
Device & Generated POF	**Target Device**
EPM1270 ES POF	EPM1270 ES EPM1270 Production
EPM1270 Production POF	EPM1270 Production

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