ANALOG DEVICES

EVAL-AD7492SDZ User Guide
UG-371

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Evaluation Board for the AD7492 1.25 MSPS, 16 mW Internal REF and CLK, 12-Bit Parallel ADC

FEATURES

Full-featured evaluation board for the AD7492
PC control in conjunction with the System Demonstration Platform (EVAL-SDP-CB1Z)
PC software for control and data analysis (time and frequency domain)
Standalone capability (when designing boards ensure that digital lines can be disconnected from everything else on the board to ensure operation)

EVAL-AD7492SDZ CONTENTS

EVAL-AD7492SDZ evaluation board
Evaluation software CD for the AD7492
9 V mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

System demonstration platform (EVAL-SDP-CB1Z)
Precision analog signal source
SMB cable
USB cable

EVALUATION BOARD DESCRIPTION

The EVAL-AD7492SDZ is a full-featured evaluation board, designed to allow the user to easily evaluate all features of the AD7492. The evaluation board can be controlled via the system demonstration platform (SDP) connector (J1). The SDP board allows the evaluation board to be controlled via the USB port of a PC using the AD7492 evaluation software.

On-board components include the AD8597 ultralow distortion, ultralow noise operational amplifier (single); the AD8021 low noise, high speed amplifier for 16-bit systems; the ADP1613 650 kHz/1.3 MHz step-up PWM dc-to-dc switching converter with 2.0 A current limit; the ADP3303-5 high accuracy anyCAP™ 200 mA low dropout linear regulator; and the ADP2301 1.2 A, 20 V, 1.4 MHz nonsynchronous step-down switching regulator.

The evaluation board features analog bias-up circuitry. Bipolar signals are input via the SK3 SMB connector and are biased up by the on-board bias-up buffer circuit. The biased up signal is available at the VIN SMB and can be applied to the VIN input of the AD7492 device by placing the LK10 link in Position A.

Various link options are described in the Evaluation Board Hardware section. The Parallel Interface section of this user guide should be consulted when configuring the board for standalone operation.

Complete specifications for the AD7492 are provided in the AD7492 data sheet, available from Analog Devices, Inc., which should be consulted in conjunction with this user-guide when using the AD7492 evaluation board.

FUNCTIONAL BLOCK DIAGRAM

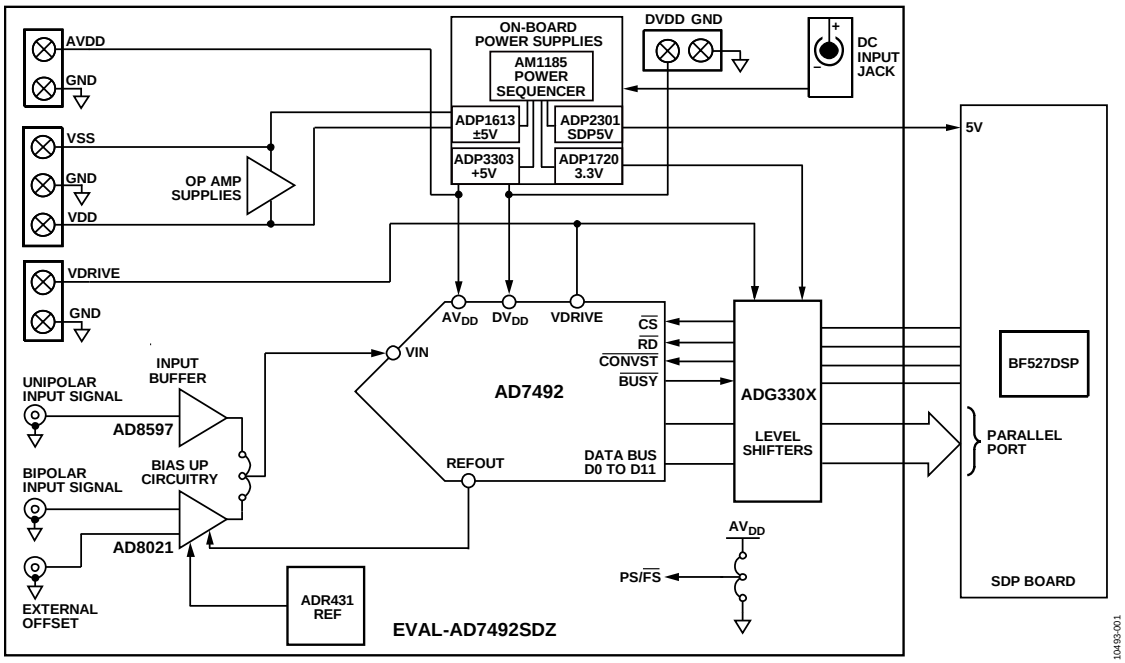

Figure 1.

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REVISION HISTORY

10/12—Revision 0: Initial Version

EVAL-AD7492SDZ QUICK START GUIDE

RECOMMENDED QUICK START GUIDE

To install the software, do the following:

1. Install the AD7492 software from the enclosed CD. When installing the software, ensure that the EVAL-SDP-CB1Z board is disconnected from the USB port of the PC. Restart the PC after installation.
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7492SDZ board, as shown in Figure 2.
3. Screw the two boards together with the enclosed nylon screw-nut set because it ensures that the boards connect firmly together.
4. Connect the 9 V power supply adapter included in the kit to the J2 connecter on the EVAL-AD7492SDZ board.
5. Connect the EVAL-SDP-CB1Z board to the PC via the USB cable. For Windows® XP, users may need to search for the EVAL-SDP-CB1Z drivers. If prompted by the operating system, choose to automatically search for the drivers for the EVAL-SDP-CB1Z board.
6. Launch the EVAL-AD7492SDZ software from the **Analog Devices** subfolder in the **All Programs** menu.

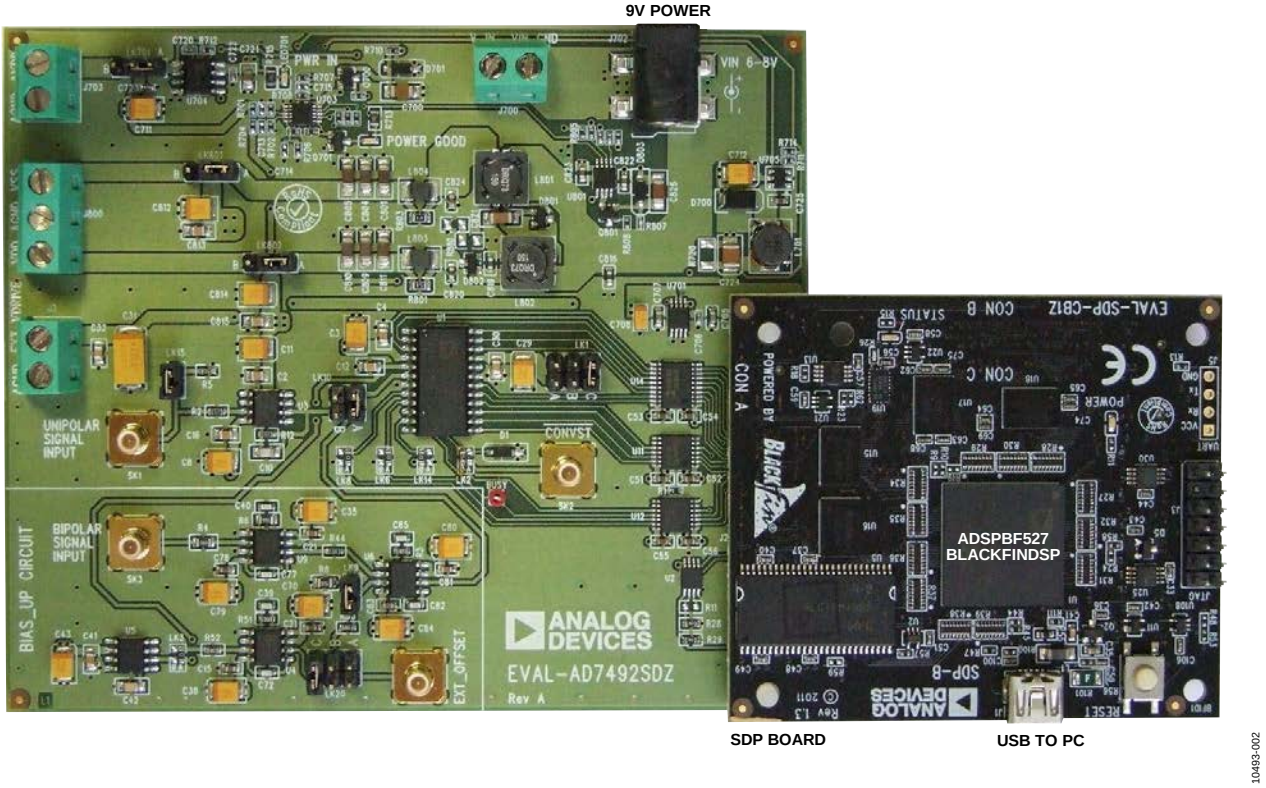


Figure 2. Hardware Configuration, Setting Up the EVAL-AD7492SDZ

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7492 is a 12-bit high speed, low power, successive approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and features a maximum throughput rate of 1 MSPS. It contains a low noise, wide bandwidth track-and-hold amplifier that can handle bandwidths up to 10 MHz.

The conversion process and data acquisition are controlled using standard control inputs allowing for easy interface to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$, and conversion is also initiated at this point. The BUSY pin goes high at the start of conversion and goes low 880 ns later to indicate that the conversion is complete. There are no pipeline delays associated with the part. The conversion result is accessed via the standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7492 uses advanced design techniques to achieve very low power dissipation at high throughput rates. The part offers flexible power/throughput rate management. It is also possible to operate the part in full sleep mode and partial sleep mode, where the part wakes up to do a conversion and automatically enters a sleep mode at the end of conversion. The type of sleep mode is hardware selected by the PS/$\overline{\text{FS}}$ pin. Using these sleep modes allows very low power dissipation numbers at lower throughput rates.

The analog input range for the part is 0 V to the reference voltage. The 2.5 V reference is supplied internally and is available for external referencing.

HARDWARE LINK OPTIONS

Before using the evaluation board, 13 link options must be set for the required operating setup. Table 1 outlines the function of these options. Table 1 shows the position in which all the links are set when the evaluation board is packaged. Jumper and solder link (LKx) options must be set correctly to select the appropriate operating setup before using the evaluation board. The default link positions are shown in Table 2, and the functions of these options are outlined in Table 1

Table 1. Link Options

Link No.	Function
LK1	This link determines the value of V_{DRIVE}. When in Position A, V_{DRIVE} is tied to AV_{DD}. When in Position B, V_{DRIVE} is supplied externally via the J3 connector. When in Position C, V_{DRIVE} is set to 3.3 V.
LK2	This link option selects the source of the $\overline{\text{CONVST}}$ input. When this link is in Position A, the $\overline{\text{CONVST}}$ input is provided by the SK2 external socket. When this link is in Position B, the $\overline{\text{CONVST}}$ input is provided by the EVAL-SDP-CB1Z board.
LK3	This link option determines whether the REF OUT signal from the AD7492 (Position A) or the voltage generated by the ADR431 reference (Position B) is connected to the positive input of U4.
LK6	This link option selects the source of the $\overline{\text{RD}}$ input. When this link is in Position A, the $\overline{\text{RD}}$ input is provided by the EVAL-SDP-CB1Z board. When this link is in Position B, it is tied to ground.
LK8	This link option selects the source of the $\overline{\text{CS}}$ signal. When this link is in Position A, the $\overline{\text{CS}}$ signal is provided by the EVAL-SDP-CB1Z. When this link is in Position B, it is tied to ground.
LK9	When inserted, the buffered REF OUT voltage is divided by a factor of 3 and used as the bias input for U6.
LK10	In Position A, the biased up output of U6 is applied to the VIN pin of the AD7492. In Position B, the buffered unipolar signal input that is applied to SK1 is connected to the V_{IN} pin of the AD7492.
LK14	This link option selects the sleep mode that the AD7492 can be put into. Then, this link is in Position A, and the part goes into full sleep when low power operation is selected. When this link is in Position B, the part goes into partial sleep when low power operation is selected.
LK15	When inserted, the unipolar V_{IN} impedance matching resistor is connected into the circuit.
LK20	This link option selects the voltage applied to the positive input of U6. When in Position A, an external offset can be applied via the EXT_OFFSET SMB connector. When in Position B, it is tied to ground. When in Position C, it is a buffered reference voltage.
LK701	This link option selects the source of the AV_{DD} signal. In Position A, the 5 V signal generated on-board is selected. In Position B, the signal externally connected via J703 is selected.
LK801	This link option selects the source of the VSS_−5V signal. In Position A, the VSS_−5V signal generated on-board is selected. In Position B, the external VSS signal is connected to J800-1.
LK802	This link option selects the source of the + VDD_+5V signal. In Position A, the VDD_+5V signal generated on-board is selected. In Position B, the external VDD signal connected to J800-3 is selected.

Table 2. Link Options—Setup Condition

Link No.	Position	Function
LK1	A	V_{DRIVE} is set to AV_{DD}.
LK2	B	The $\overline{CONVST}$ signal is provided by the EVAL-SDP-CB1Z.
LK3	A	The REFOUT pin of the AD7492 is connected to the bias circuitry.
LK6	A	The $\overline{RD}$ signal is provided by the EVAL-SDP-CB1Z.
LK8	A	The $\overline{CS}$ signal is provided by the EVAL-SDP-CB1Z.
LK9	Inserted	The buffered REF OUT voltage is divided by a factor of 3, and it is used as the bias input for U6.
LK10	B	The V_{IN} pin of AD7492 is connected to the buffered unipolar signal input that is applied to SK1.
LK14	B	The AD7492 goes into partial sleep mode if low power operation is selected.
LK15	Inserted	The unipolar V_{IN} impedance matching resistor is connected into the circuit.
LK20	A	The buffered internal reference is used as the bias input for U6.
LK801	A	It selects the VSS_−5V signal generated on the board as opposed to the externally connected VSS (J800-1) signal.
LK802	A	It selects the VDD_+5V signal generated on the board as opposed to the externally connected VDD (J800-3) signal.
LK701	A	It selects the AV_{DD} signal generated on the board as opposed to being externally connected via J703.

POWER SUPPLIES

Take care before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode.

When using the EVAL-AD7492SDZ in conjunction with the EVAL-SDP-CB1Z board, connect the dc transformer to the J700 connector. AV_{DD}, DV_{DD}, and V_{DRIVE} are generated on-board. Each supply is decoupled on the EVAL-AD7492SDZ using 10 µF and 0.1 µF capacitors. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 3. External Power Supply Required

Power Supply Terminal	Voltage Range (V)	Purpose
V_{IN}[1]	+7 to +9	Supplies all the on-board power supplies that generate all the required supplies to run the evaluation board
V_{DD}	+5.5	Amplifier +VDD
V_{SS}	−5.5	Amplifier −VSS
AV_{DD}[2]	+2.7 to +5.25	ADC analog and digital supply rails
V_{DRIVE}	+2.7 to +5.25	Supply voltage for the output drivers and digital input circuitry

[1] When this is supplied, all other power supplies are available on-board. If this supply is not used, all other supplies must be sourced from an external source.

[2] Analog supply voltage. This is the only supply voltage for all the analog circuitry on the AD7492. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Decouple this supply to AGND.

PARALLEL INTERFACE

The EVAL-AD7492SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Zoperates at a 3.3 V logic level. This allows V_{DRIVE} voltages to exceed 3.3 V. An external $\overline{CONVST}$ signal can be supplied to the board via the SK2 SMB. Parallel data can only be monitored via the EVAL-SDP-CB1Z board and software. A break out board ADZS-BRKOUT-EX3 is available that allows access to the digital lines.

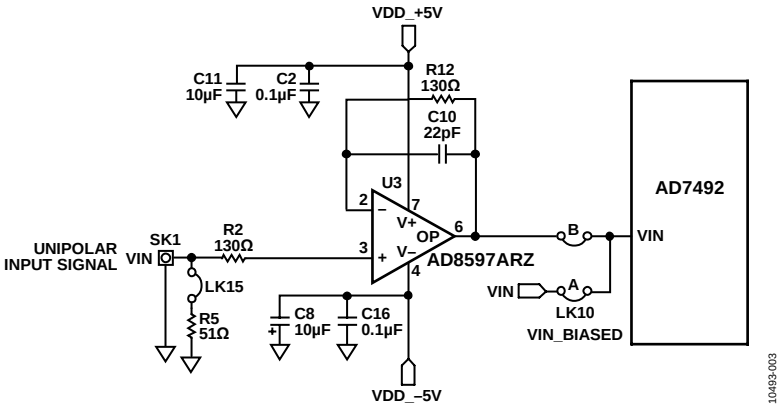


Figure 3. Unipolar Input Buffer Circuitry

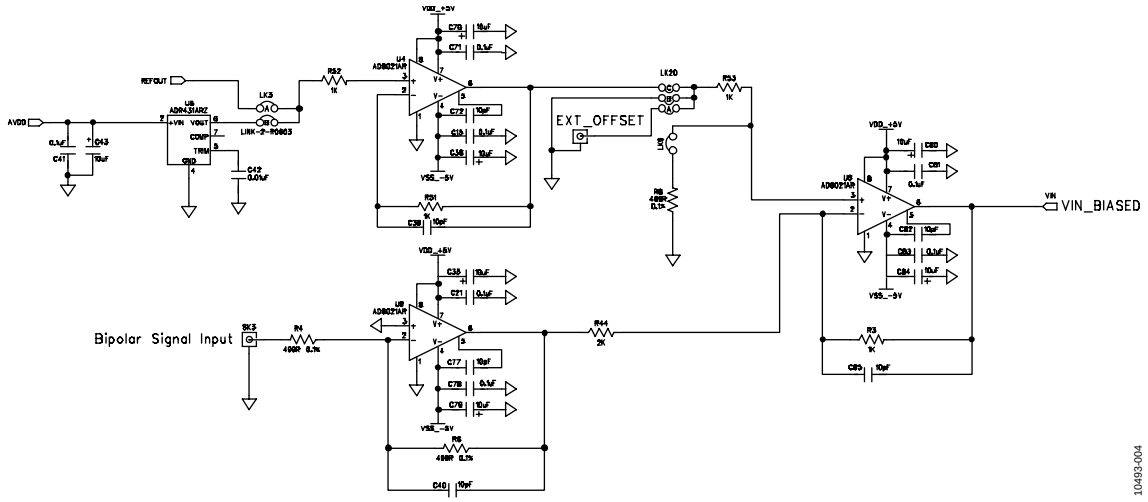


Figure 4. Bipolar Input Buffer Circuitry

ANALOG INPUTS

The analog input to the evaluation board can be either the SK1 SMB (push on) connector with a unipolar signal source or the SK3 SMB (push on) connector when using a bipolar signal source.

The unipolar input is buffered with dedicated circuitry (U3) and discrete components, as shown in Figure 3.

LK15 can be used to put a 50 Ω impedance matching load on the input. LK10 is placed in Position B to connect the output of U3 to the AD7492.

The bipolar signal is buffered with dedicated circuitry (U4, U6, and U9) along with the discreet components shown in Figure 4.

The circuit shown in Figure 4 allows for different configurations, and an external source can be applied to bias the input voltage.

The analog input buffer amplifier (U3) is set as a unity gain buffer. The amplifier positive rail is driven from ±5 V (from ADP1613, U801, that is used to drive a dual rail, power supply, SEPIC Cuk configuration), which can be changed to a different value, as required, by using the external terminals on J800. LK801 and LK802 must be set to Position B to drive the amplifiers from an external source. For dynamic performance, an FFT test can be done by applying a very low distortion ac source.

REFERENCE OPTIONS

The reference source can be from the AD7492 REF OUT pin or the ADR431 ultralow noise XFET® voltage reference device (U5).

EXTERNAL CONNECTORS

Table 4 lists the connector functions of the evaluation board.

Table 4. Connector Functions

Connector	Function
EXT_OFFSET	SMB socket for external bias input, which provided that LK20 is correctly configured, can be applied to U6
J3	External VDRIVE screw terminal connector
J700	7 V to 9 V bench supply screw terminal connector
J702	7 V to 9 V dc transformer power connector
J703	AVCC screw terminal connector
J800	VSS and VDD screw terminal connectors
SK1	Unipolar signal input SMB socket
SK2	$\overline{\text{CONVST}}$ signal input SMB socket
SK3	Bipolar signal input SMB socket

EVAL-AD7492SDZ BASIC HARDWARE SETUP

The AD7492 evaluation board connects to the EVAL-SDP-CB1Z. The EVAL-SDP-CB1Z board is a controller board that is the communication link between the PC and the main evaluation board. Figure 2 shows a photograph of the connections made between the AD7492 daughter board and the EVAL-SDP-CB1Z board.

Before connecting power, connect the EVAL-AD7492SDZ board to Connector A or Connector B on the EVAL-SDP-CB1Z board. Nylon screws are included in the EVAL-AD7492SDZ evaluation kit and can be used to ensure that the EVAL-AD7492SDZ and the EVAL-SDP-CB1Z boards are connected firmly together.

Once the EVAL-AD7492SDZ and the EVAL-SDP-CB1Z boards are connected securely, connect the power supplies on the EVAL-AD7492SDZ board. The EVAL-AD7492SDZ requires an external power supply that is included in the evaluation board kit.

Connect this power supply to the J702 connector on the EVAL-AD7492SDZ board. Alternatively, a bench power supply can be used to power the EVAL-AD7492SDZ via J700. Further details on the required power supply connections and options are detailed in the Power Supplies section.

Before connecting the EVAL-SDP-CB1Z board to the PC, ensure that the AD7492 software has been installed from the enclosed CD. The full software installation procedure is detailed in the Evaluation Board Software section.

Finally, connect the EVAL-SDP-CB1Z board to the PC via the USB cable enclosed in the EVAL-SDP-CB1Z kit. If using the Windows XP platform, users may need to search for the EVAL-SDP-CB1Z drivers. If prompted by the operating system, choose to automatically search for the drivers for the EVAL-SDP-CB1Z.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD7492SDZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the installation. The default location for the software is **C:\Program Files\Analog Devices\AD7492**.

Install the evaluation software before connecting the evaluation board and the EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the installation:

1. EVAL-AD7492SDZ evaluation board software install
2. EVAL-SDP-CB1Z SDP board drivers install

Figure 5 to Figure 9 show the steps to take to install the EVAL-AD7492SDZ evaluation software. Figure 10 to Figure 13 show the steps to take to install the EVAL-SDP-CB1Z drivers. Proceed through all of the installation steps allowing the software and drivers to be placed in the appropriate locations. Until the software and drivers have been installed, do not connect the EVAL-SDP-CB1Z board to the PC.

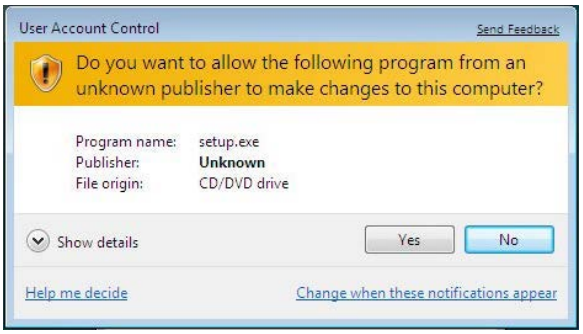


*Figure 5. AD7492 Install Window 1 (**Yes**)*

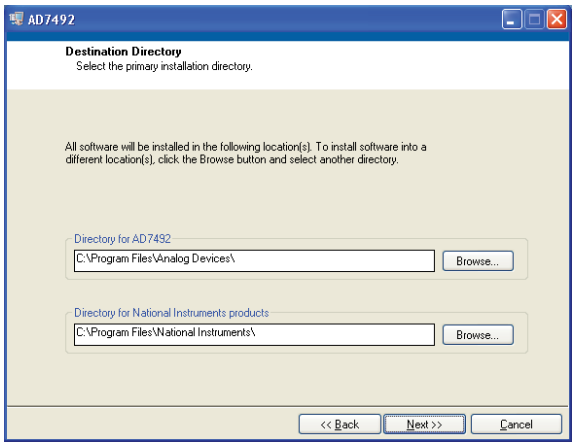


Figure 6. AD7492 Install Window 2 (Choose Destination)

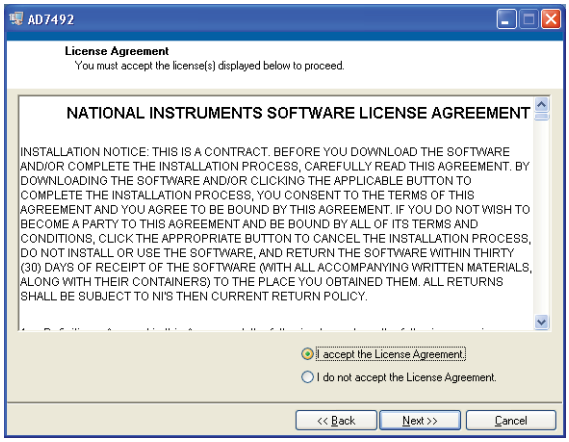


*Figure 7. Install Window 3 (**I accept the License Agreement. Next >>**)*

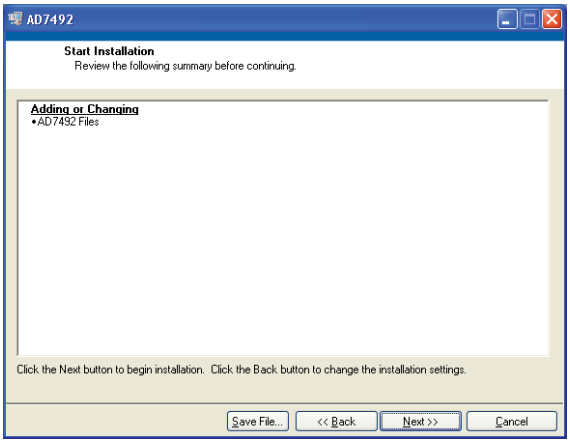


*Figure 8. AD7492 Install Window 4 (**Next >>**)*

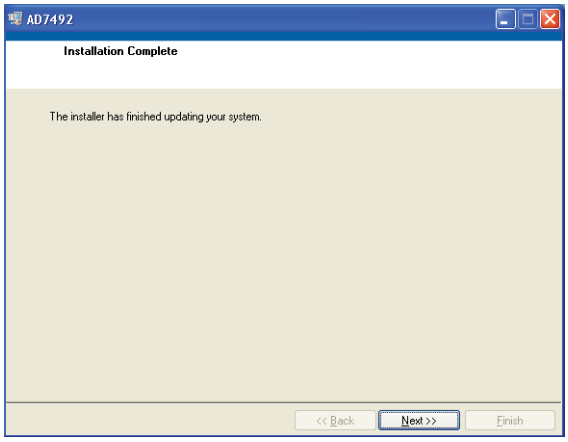


*Figure 9. AD7492 Install Window 5 (**Next >>**)*

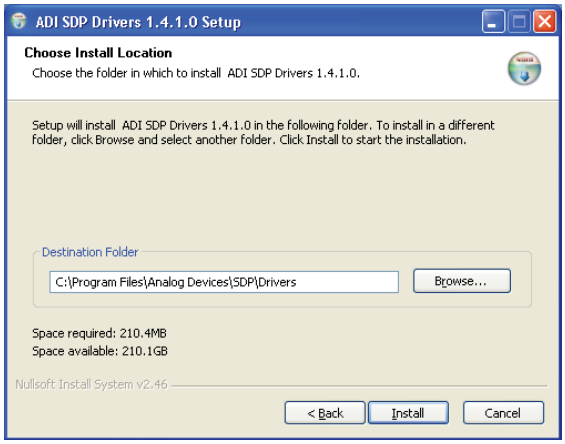


*Figure 10. EVAL-SDP-CB1Z Drivers Setup Window 2 (**Choose Install Location**)*

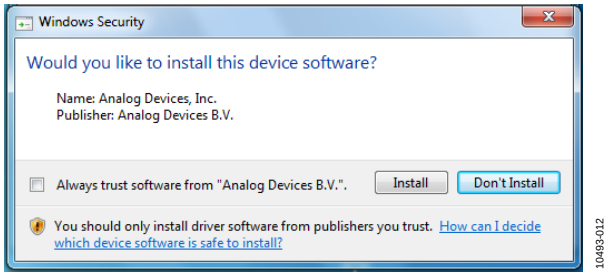


*Figure 11. EVAL-SDP-CB1Z Drivers Setup Window 3 (**Install**)*

*Figure 12. EVAL-SDP-CB1Z Drivers Setup Window 4 (**Finish**)*

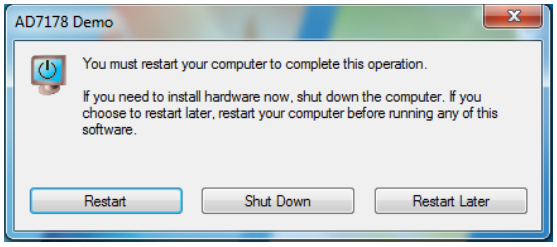


*Figure 13. EVAL-SDP-CB1Z Drivers Setup Window 5 (**Restart**)*

After installation from the CD is complete, connect the EVAL-AD7492SDZ to the EVAL-SDP-CB1Z as described in the Evaluation Board Hardware section.

When the EVAL-SDP-CB1Z board is first plugged in via the USB cable provided, allow the **Found New Hardware Wizard** to run. Once the drivers are installed, verify that the board has connected correctly by looking at the **Device Manager** of the PC. Right-click **My Computer/Manage/System Tools/Device Manager**, as shown in Figure 14, to find the **Device Manager**. **Analog Devices System Development Platform (32MB)** should appear under **ADI Development Tools**. This now completes the installation.

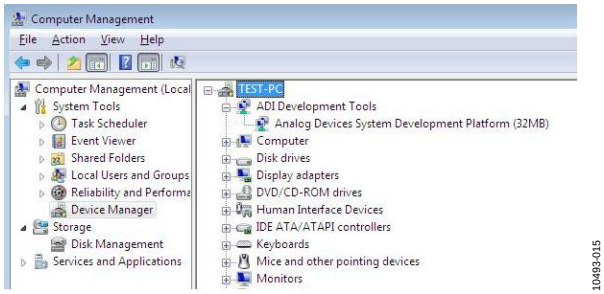


Figure 14. Device Manager

LAUNCHING THE SOFTWARE

Once the EVAL-AD7492SDZ and EVAL-SDP-CB1Z are correctly connected to the PC, the AD7492 software can be launched.

To launch the software, complete the following steps:

1. From the **Start** menu, select **Programs/Analog Devices/AD7492**. The main window of the software then displays.
2. If the AD7492 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 15). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

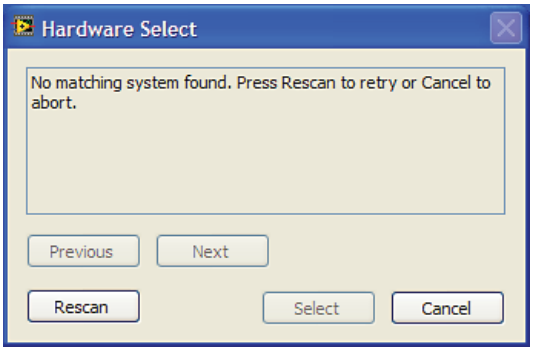


Figure 15. Connectivity Error Alert

Figure 16. Setup Screen

SOFTWARE OPERATION

When the software is launched, the panel opens, and the software looks for hardware connected to the PC. The software detects the generic attached to the PC and returns this in a user dialog box.

The user software panel then launches, as shown in Figure 16.

USER SOFTWARE PANEL DESCRIPTION

The user software panel, as shown in Figure 16, has the following features:

1. **File** menu with a+ choice of the following:
   a. **Load Data**: load previously captured data in tab separated values (.tsv) format for analysis
   b. **Save Data as .tsv**: Save captured data in .tsv format for future analysis
   c. **Print Front Panel Picture**: use to print the front panel to default printer.
   d. **Save Picture**: use to save the current screen capture
   e. **Exit**
2. When hardware is connected to the USB port, the software automatically detects which generic is connected and displays in here. Without the hardware, the software can operate in standalone mode for data analysis, and the part information notes the part number pulled from the saved data file.
3. Sampling frequency (fig says **Sampling Rate**?). The default sampling frequency matches the maximum sample rate of the ADC connected to the board. Users can adjust the sampling frequency; however, there are limitations around the sample frequency, where unusable sample frequencies are input, the software automatically adjusts the sample frequency accordingly. Units can be entered, such as 10k for 10,000 Hz. Because the maximum sample frequency possible is device dependent, with some of the ADCs capable of operating up to 250 kSPS, while others can run to 1.3 MSPS, the software matches the particular ADC ability. If the user enters a value larger than the ability of the existing device, the software indicates this and reverts to the maximum sample frequency.

4. **Sample**: to perform a single capture.
5. **Continuous**: to perform a continuous capture from the ADC. Press a second time to stop sampling.
6. Select the number of samples to analyze.
7. There are four tabs available that display the data in different formats. These are listed here and described in more detail in the Data Capture/Waveform, AC Testing—Data Capture/Histogram, DC Testing—Data Capture/Histogram, AC Testing—Data Capture/FFT, and Data Capture/Summary sections.
   a. Waveform
   b. Histogram
   c. FFT
   d. Summary

To exit the software, go to **File/Exit**.

Within any of the chart panels, the following tools allow user control of the different chart displays:

-  is used for controlling the cursor, if present.
-  is used for zooming in and out.
-  is used for panning.

To save plots, click on File > **Save plot**.

DATA CAPTURE/WAVEFORM TAB

Figure 17 shows the **Data Capture/Waveform** tab. The input signal here is a 1 kHz sine wave.

The waveform analysis reports back the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

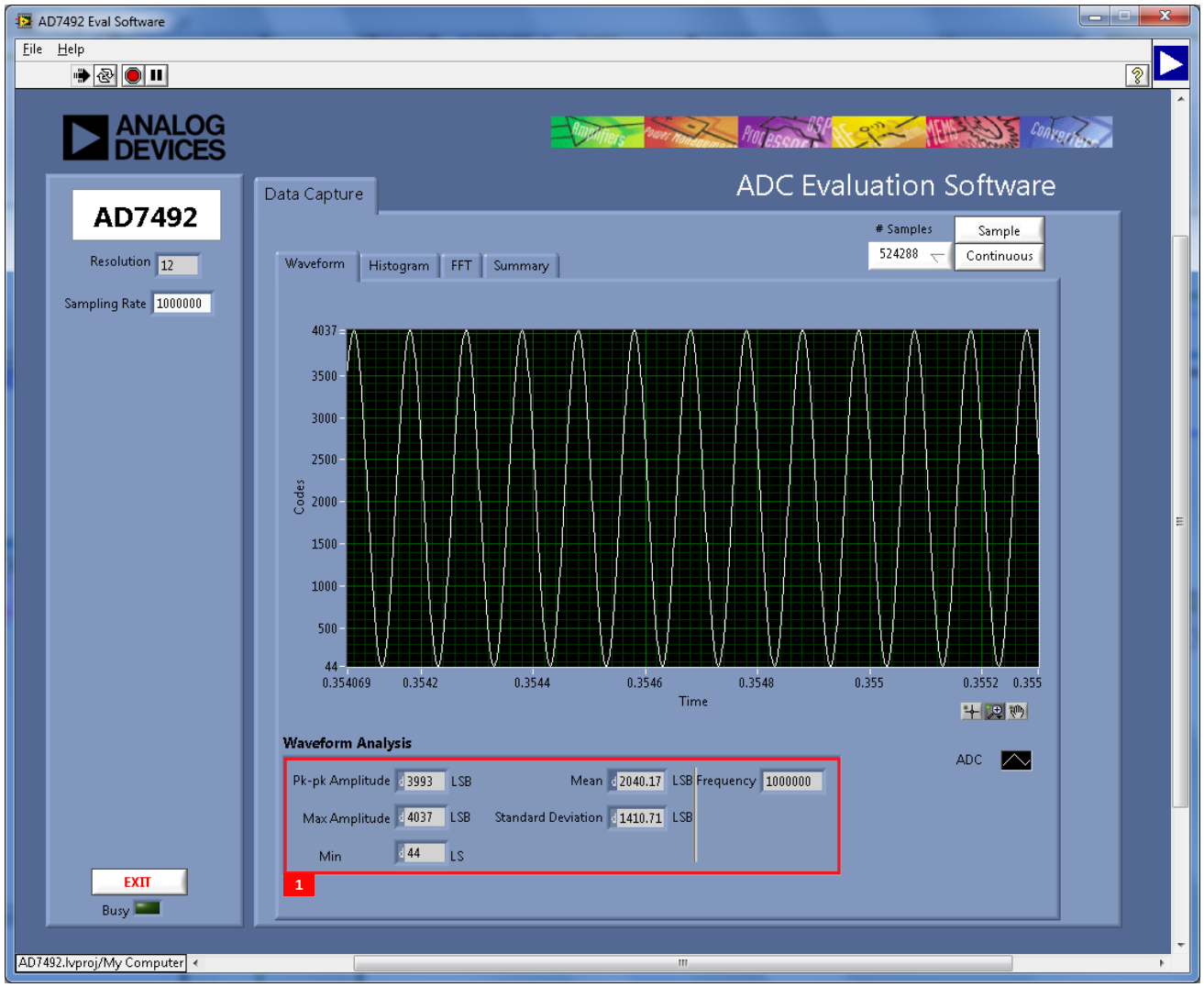


*Figure 17. **Data Capture/Waveform** Tab*

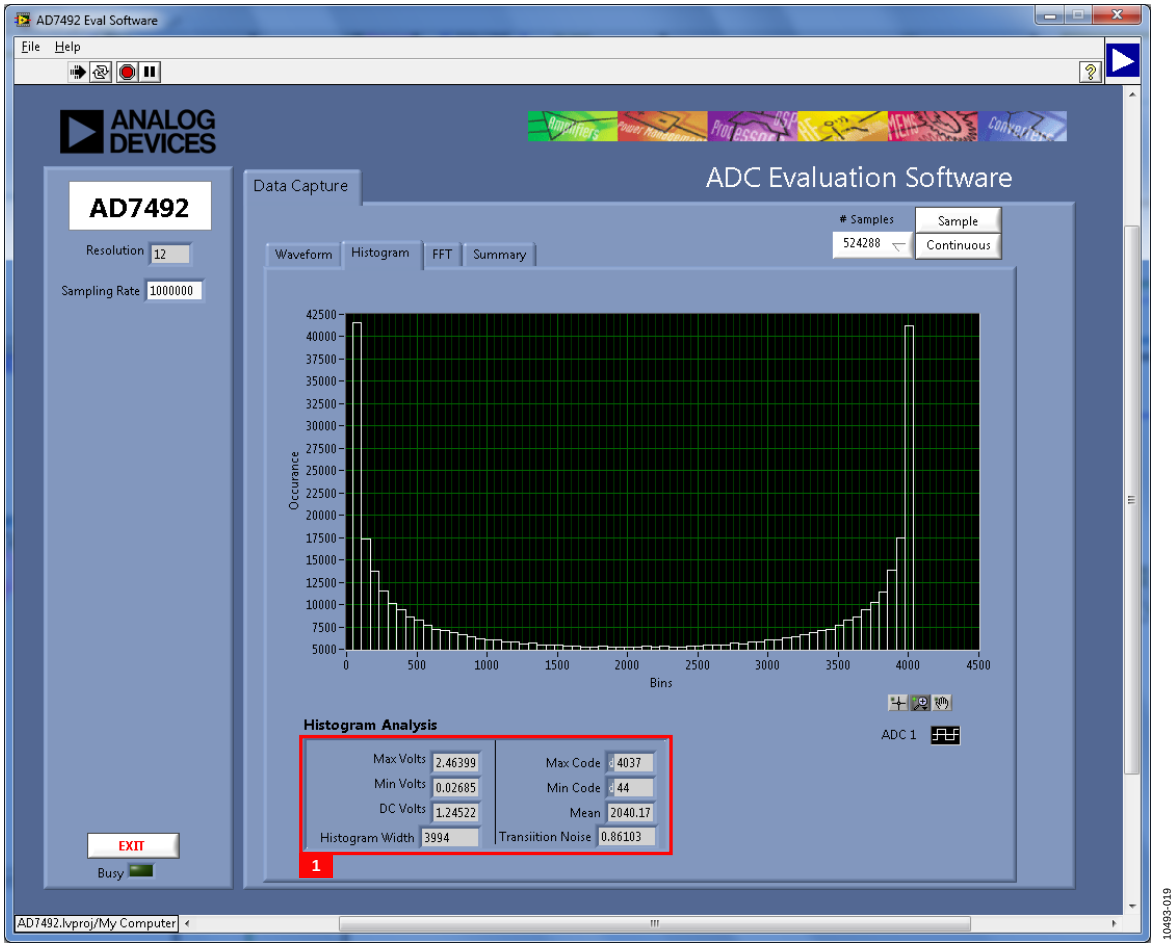


*Figure 18. **Data Capture/Histogram** Tab*

AC TESTING—DATA CAPTURE/HISTOGRAM TAB

Figure 18 shows the **Data Capture/Histogram** tab. This tests the ADC for the code distribution for ac input and computes the mean and standard deviation, or transition noise of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select **Histogram** from the test selection window and click **Sample.** An ac histogram needs a quality signal source applied to the input of the SK1 and SK3 connectors. Figure 18 shows the histogram for a 10 kHz sine wave applied to the ADC input, and the results calculated.

Number 1 in Figure 18 shows the different measured values for the data captured.

DC TESTING—DATA CAPTURE/HISTOGRAM TAB

More commonly, the **Data Capture/Histogram** tab is used for dc testing. This is where user can test the ADC for the code distribution for dc input and compute the mean and standard deviation, or transition noise of the converter, and display the results. Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select **Histogram** from the test selection window and click **Sample**. A histogram test can be performed without an external source because the evaluation board has a buffered $V_{REF}/2$ source at the ADC input. To test other dc values, apply a source to the SK1 and SK3 inputs. It may be required to filter the signal to make the dc source noise compatible with that of the ADC.

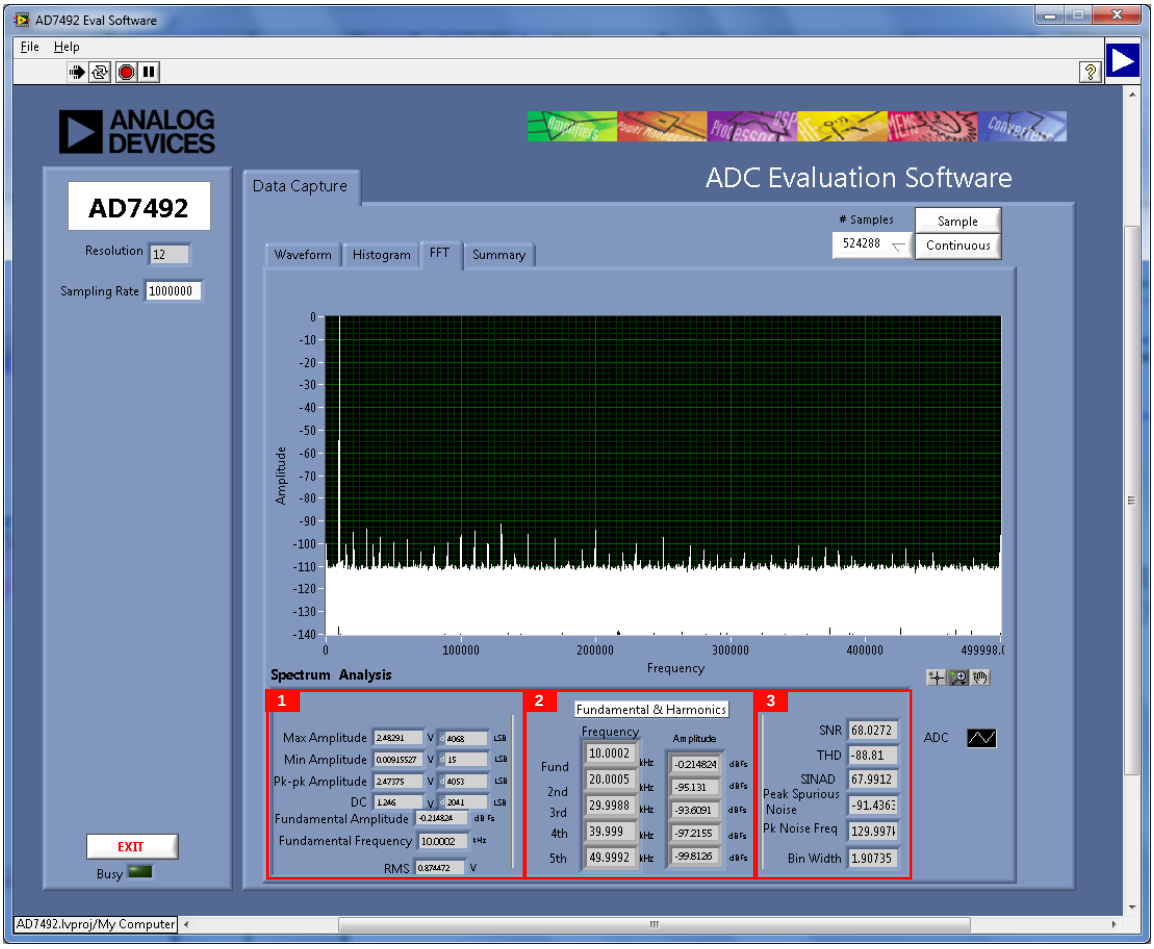


*Figure 19. **Data Capture/FFT** Tab*

AC TESTING—DATA CAPTURE/FFT TAB

Figure 19 shows the **Data Capture/FFT** tab This tests the traditional ac characteristics of the converter and displays a Fast Fourier Transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC, where the FFT is performed displaying the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). To perform an ac test, apply a sinusoidal signal to the evaluation board at the SMB inputs, SK1/SK3. Low distortion, better than 100 dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter; however, take consideration in this choice.

Furthermore, if using a low frequency band-pass filter when the full-scale input range is more than a few volts peak-to-peak, it is recommended to use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 19 displays the following results of the captured data:

1. Shows the input signal information
2. Displays the fundamental frequency (**Fund**) and amplitude in addition to the second (**2nd**) to fifth (**5th**) harmonics
3. Displays the performance data: **SNR**, **THD**, **SINAD**, **Peak Spurious Noise**, **Pk Noise Freq**, and **Bin Width**

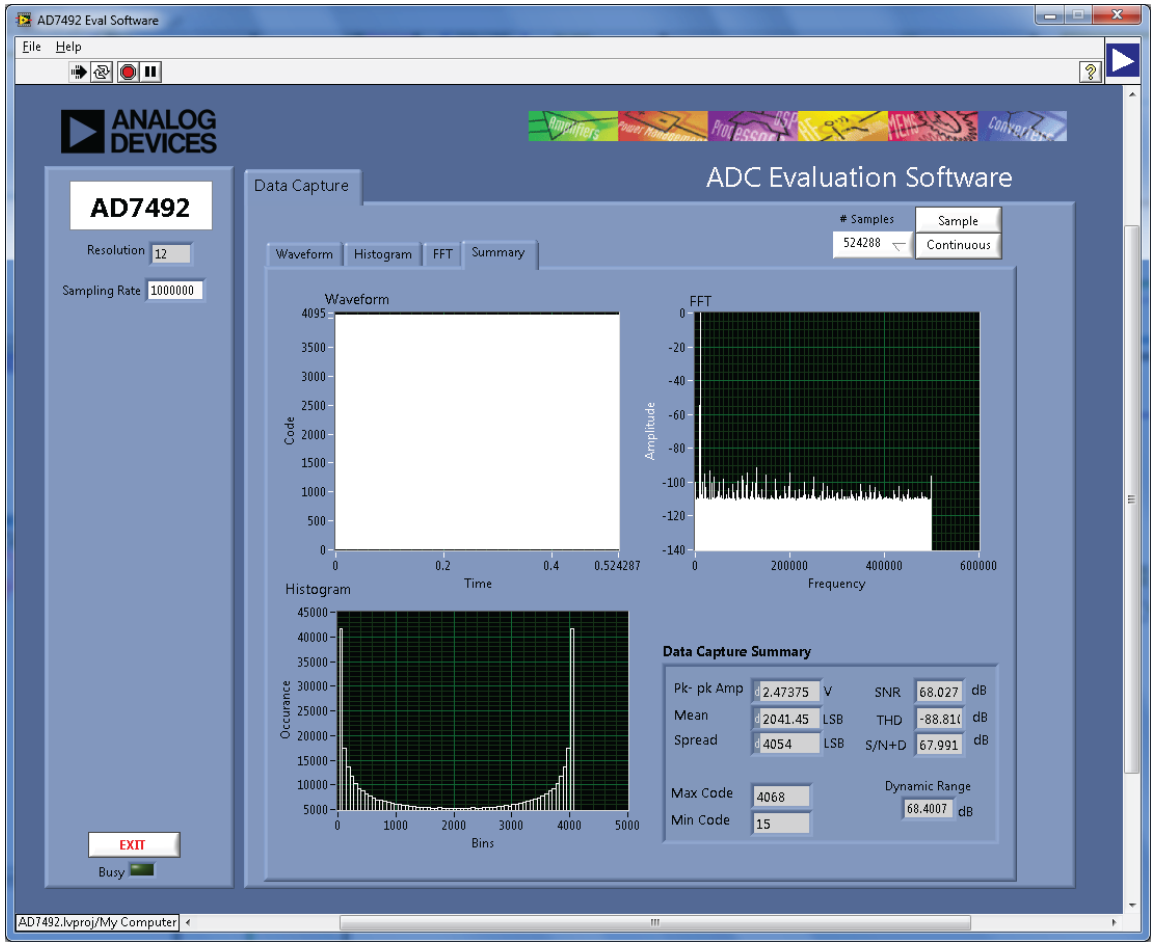


*Figure 20. **Data Capture/Summary** Tab*

DATA CAPTURE/SUMMARY TAB

Figure 20 shows the **Data Capture/Summary** tab. The **Data Capture/Summary** tab captures all the display information and provides them in one panel with a synopsis of the information including key performance parameters, such as SNR and THD.

SAVE FILE

The software can save the current captured data for later analysis to a .tsv file. In the **Choose file to Write.** Window, users are prompted to save to an appropriate folder location (see Figure 21).

LOAD FILE

In the **Choose file to Read.** Window, users are prompted to load the file (see Figure 22). User may have to navigate to find these example files. The default location for the example files is: **C:\Program Files\Analog Devices\AD7492\examples**.

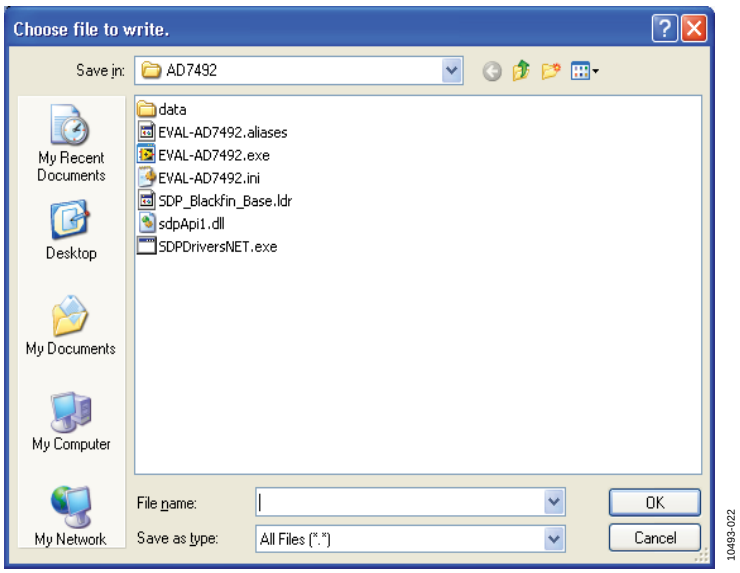


Figure 21. Save File Dialog Box

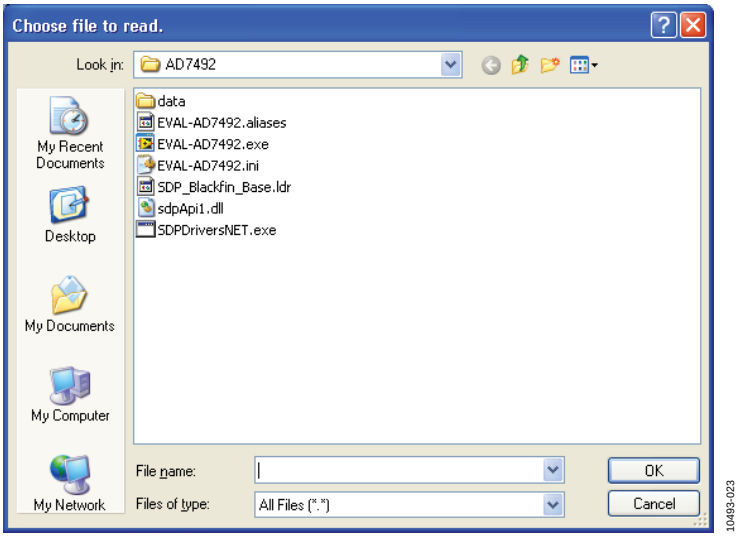


Figure 22. Load File Dialog Box

EVALUATION BOARD SCHEMATICS AND ARTWORK

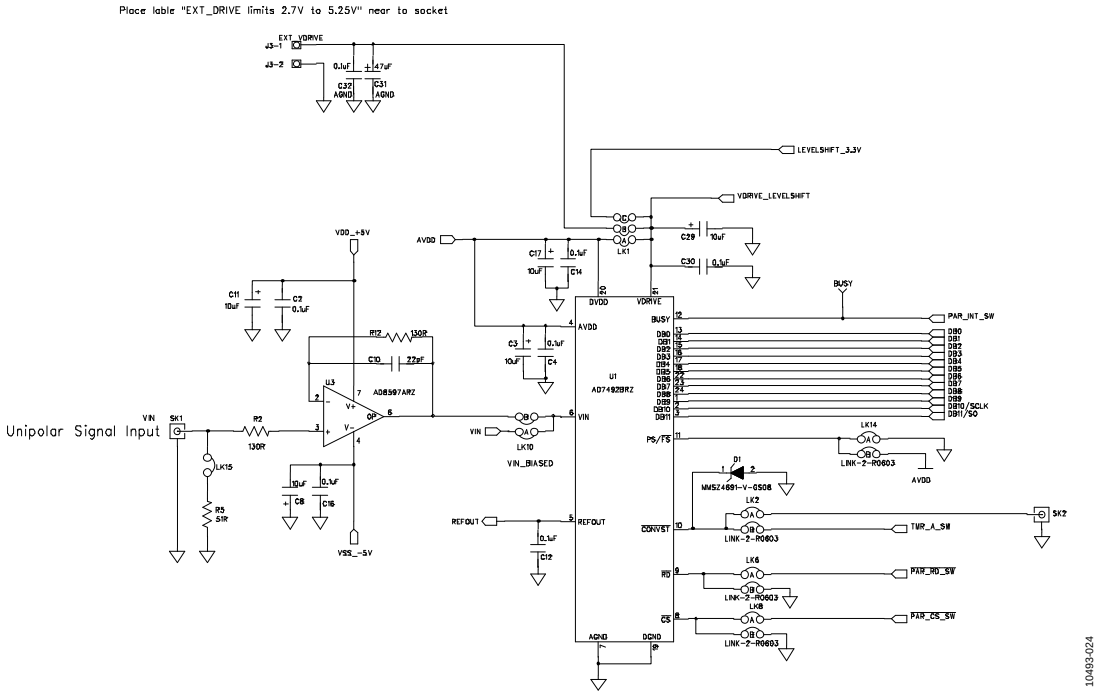


Figure 23. Schematic Page 1

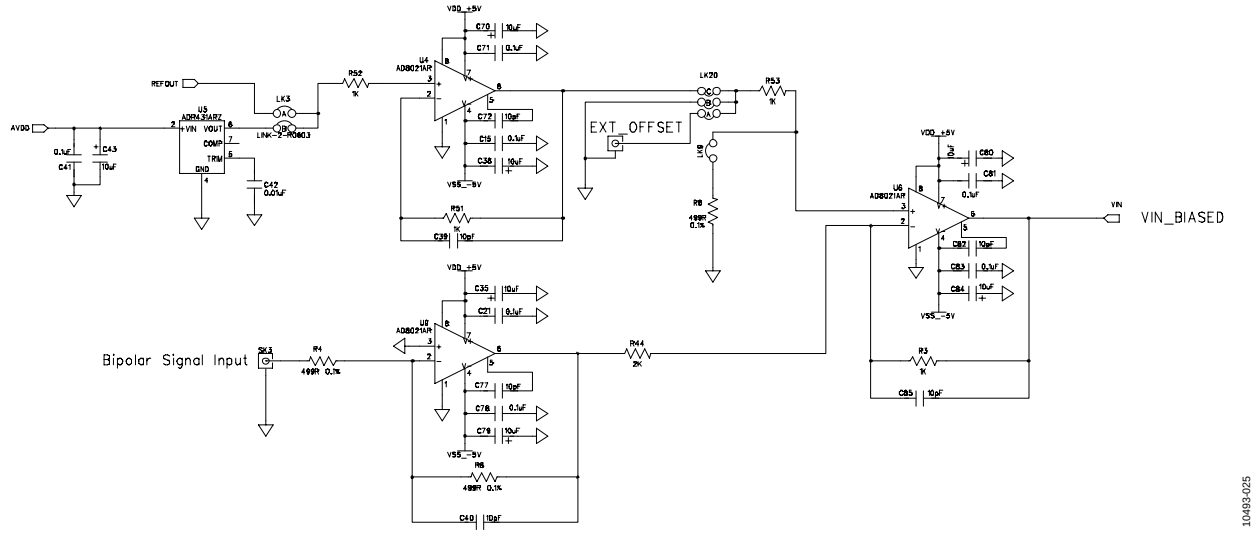


Figure 24. Schematic Page 2

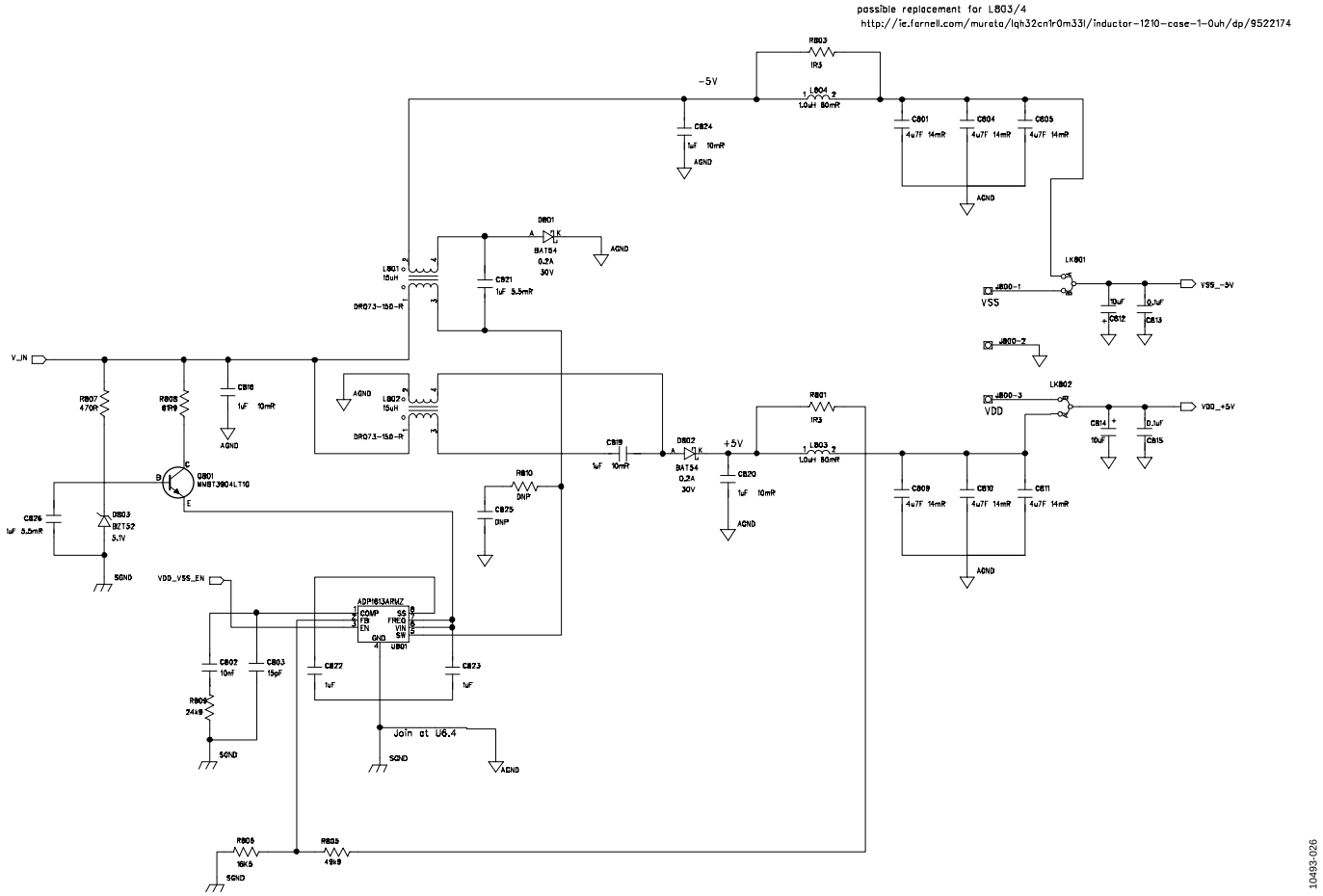


Figure 25. Schematic Page 3

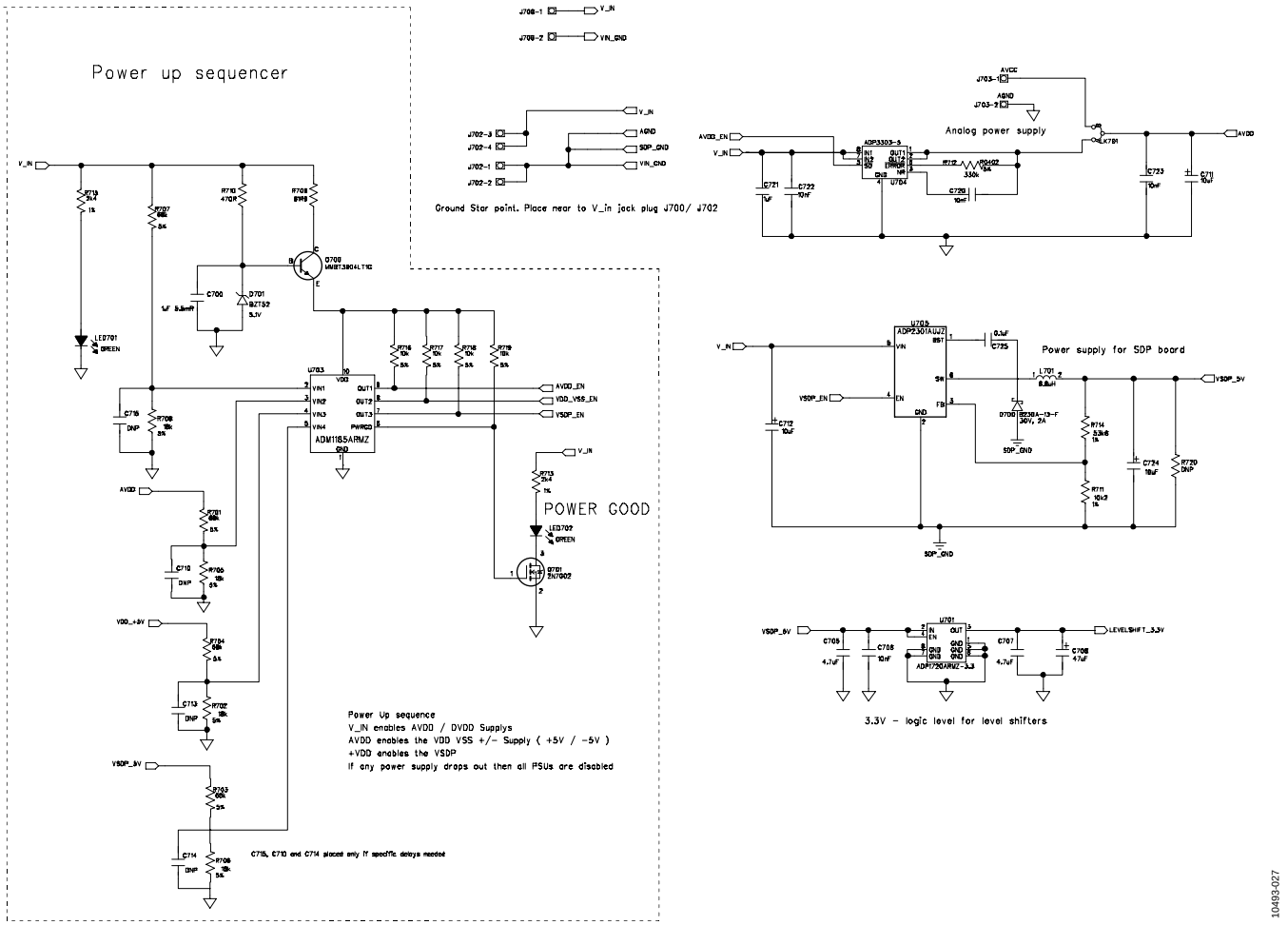


Figure 26. Schematic Page 4

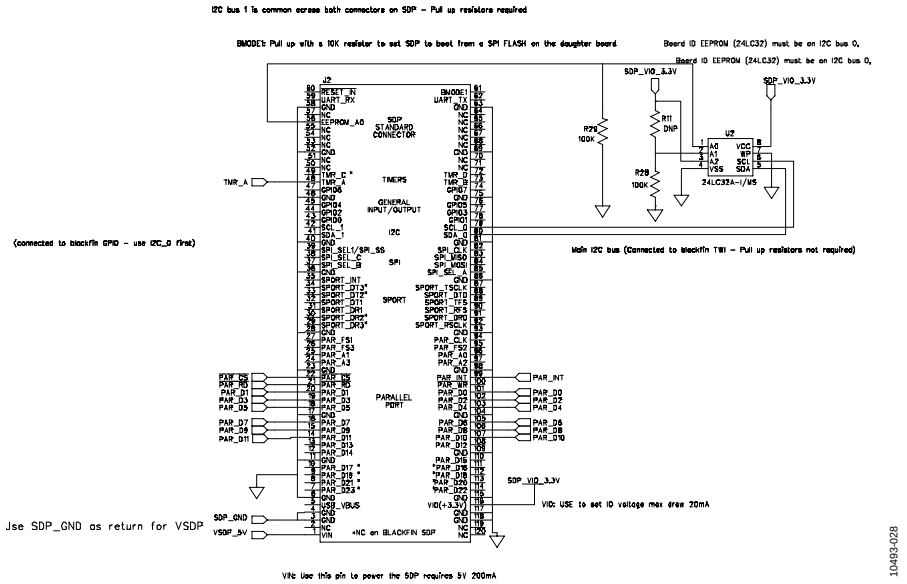


Figure 27. Schematic Page 5

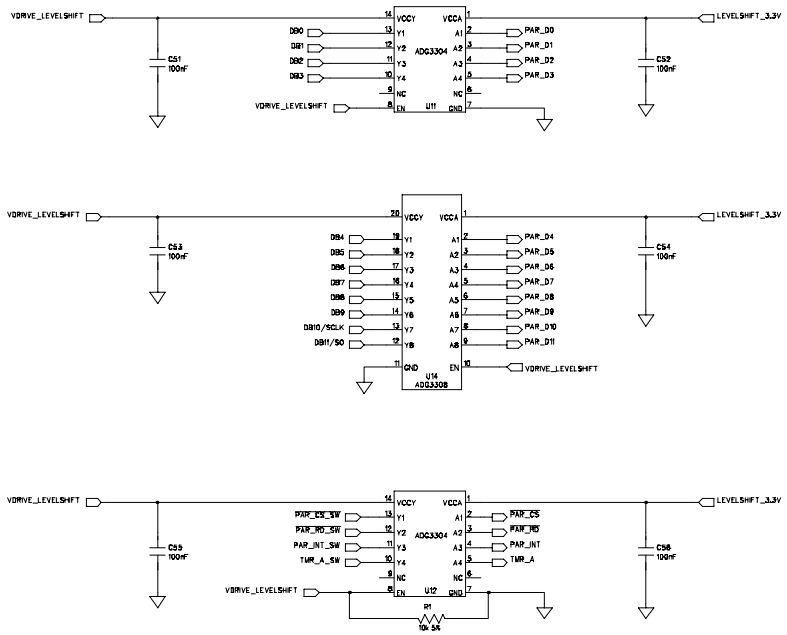
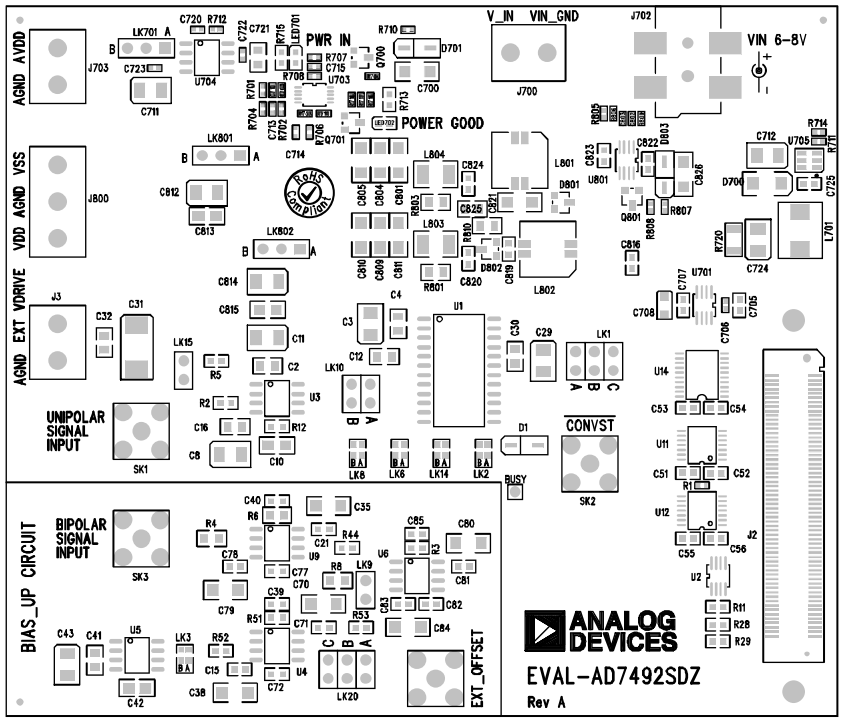


Figure 28. Schematic Page 6



Eval–AD7492SDZ (Rev. A) Top Side View.
Top Side Silkscreen

Figure 29. Top Printed Circuit Board (PCB) Silkscreen

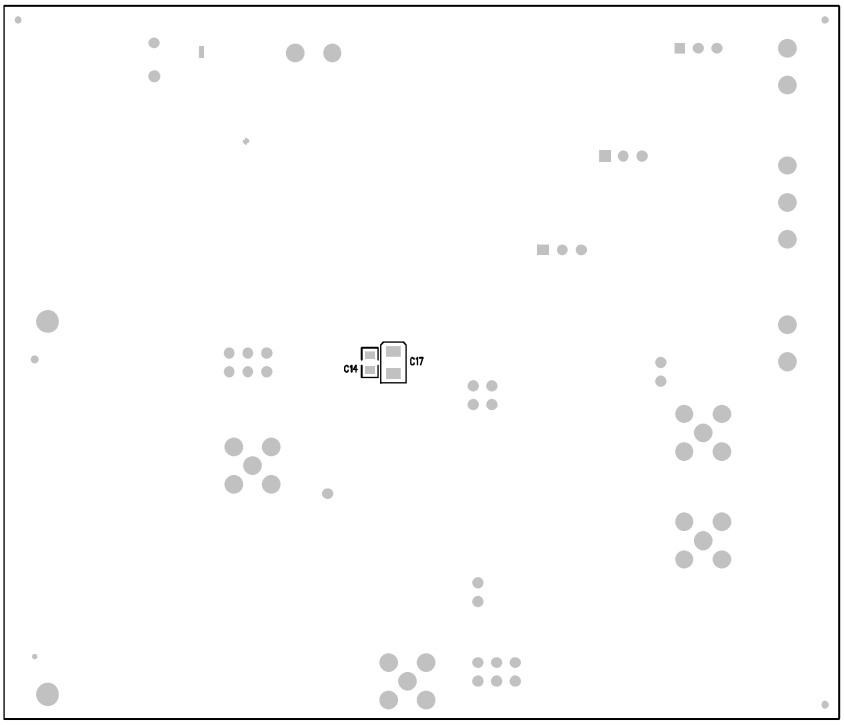


Figure 30. Bottom PCB Silkscreen

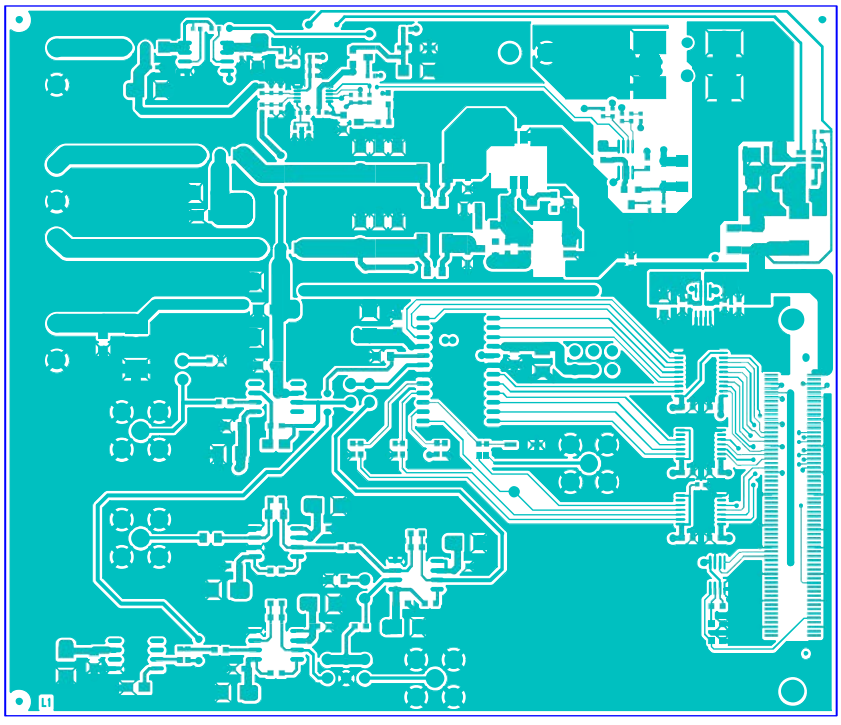
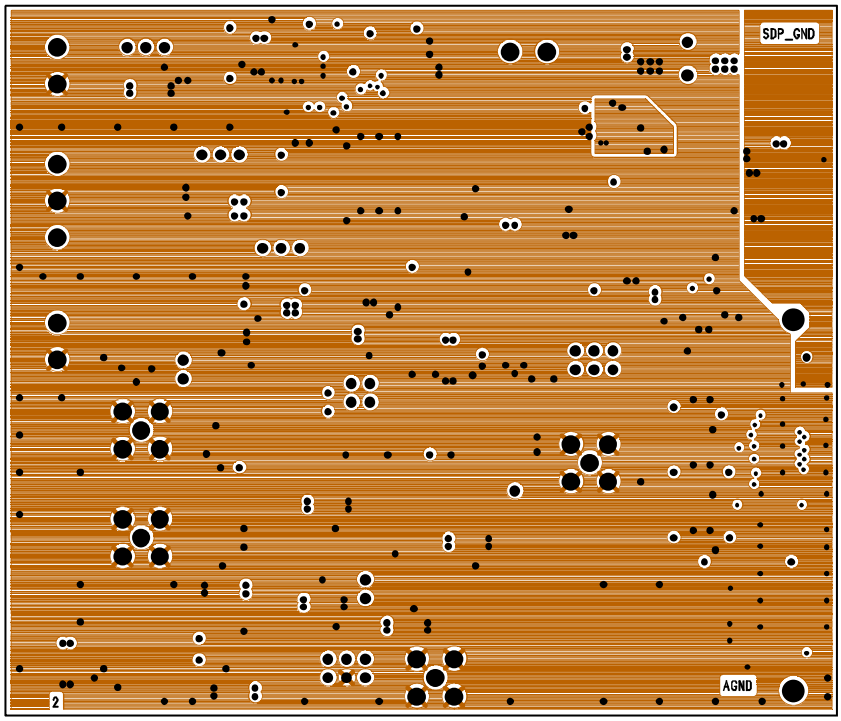


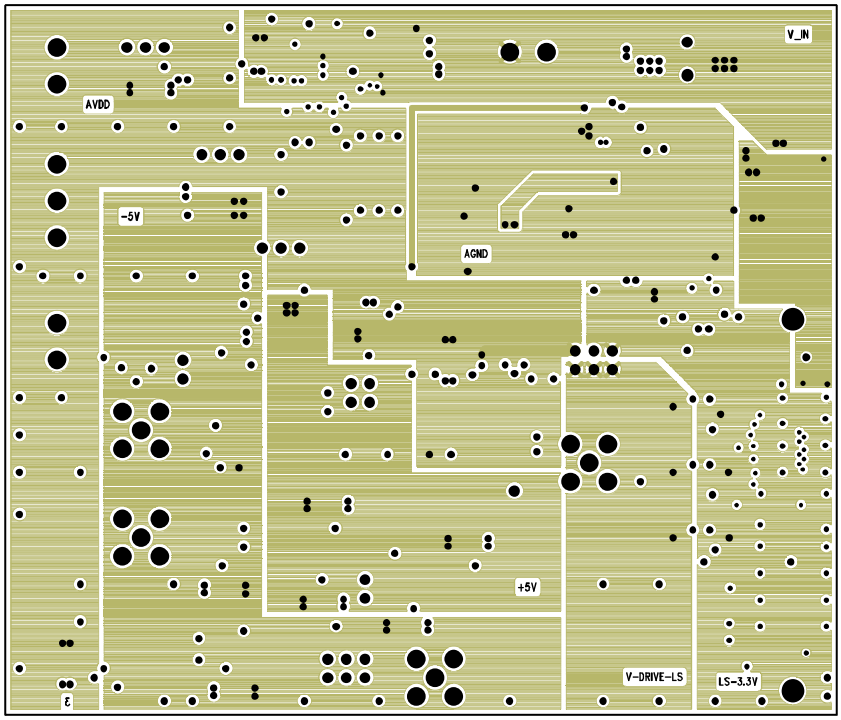
Figure 31. Layer 1 Component Side View



Eval-AD7492SDZ (Rev. A) Top Side View.
Layer 2 – Ground

10493-033

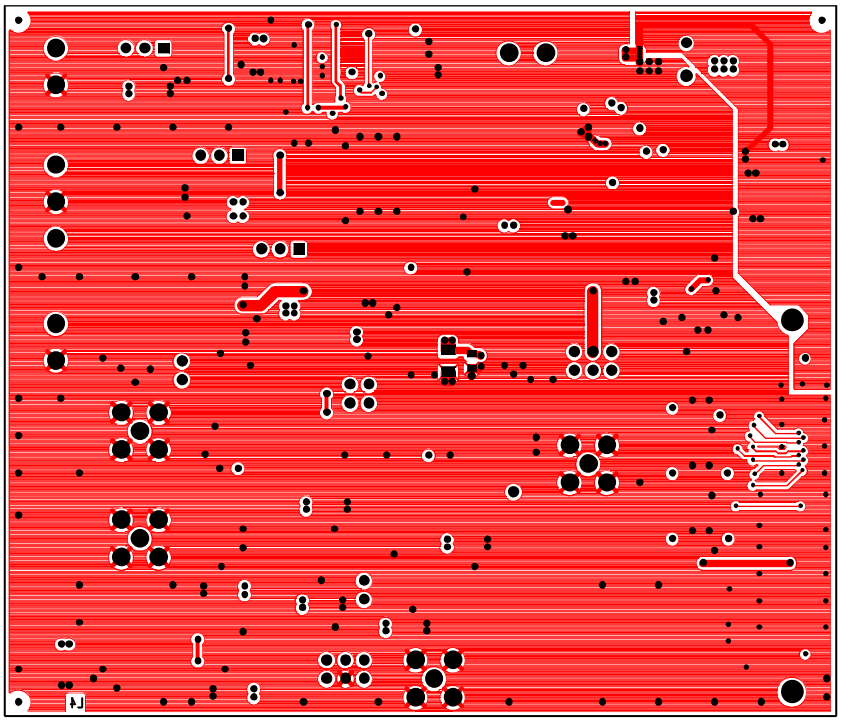
Figure 32. Layer 2 Component Side View



Eval-AD7492SDZ (Rev. A) Top Side View.
Layer 3 – Power

10493-034

Figure 33. Layer 3 Component Side View



Eval-AD7492SDZ (Rev. A) Top Side View.
Bottom Side Layer 4

10493-035

Figure 34. Layer 4 Component Side View

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG10493-0-10/12(0)

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