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Kind regards,

Team Nexperia

# 74AHC125; 74AHCT125

Quad buffer/line driver; 3-state

Rev. 04 — 11 January 2008

Product data sheet

## 1. General description

The 74AHC125; 74AHCT125 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74AHC125; 74AHCT125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $nY$ ) are controlled by the output enable input ( $n\overline{OE}$ ). A HIGH at  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state.

The 74AHC125; 74AHCT125 is identical to the 74AHC126; 74AHCT126 but has active LOW enable inputs.

## 2. Features

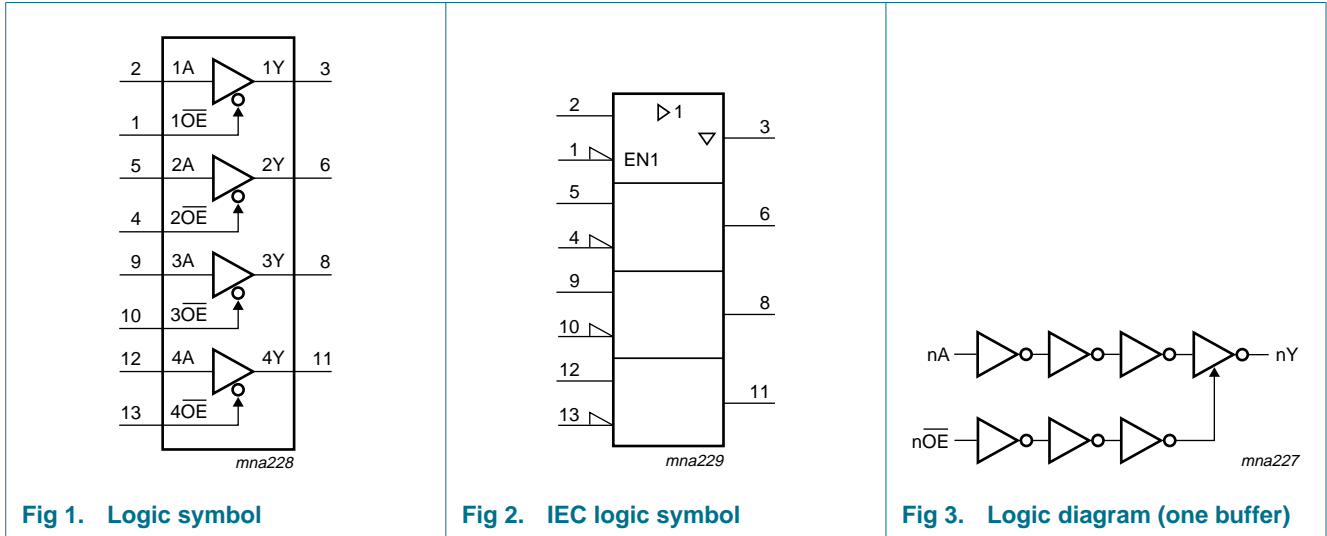
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than  $V_{CC}$
- For 74AHC125 only: operates with CMOS input levels
- For 74AHCT125 only: operates with TTL input levels
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

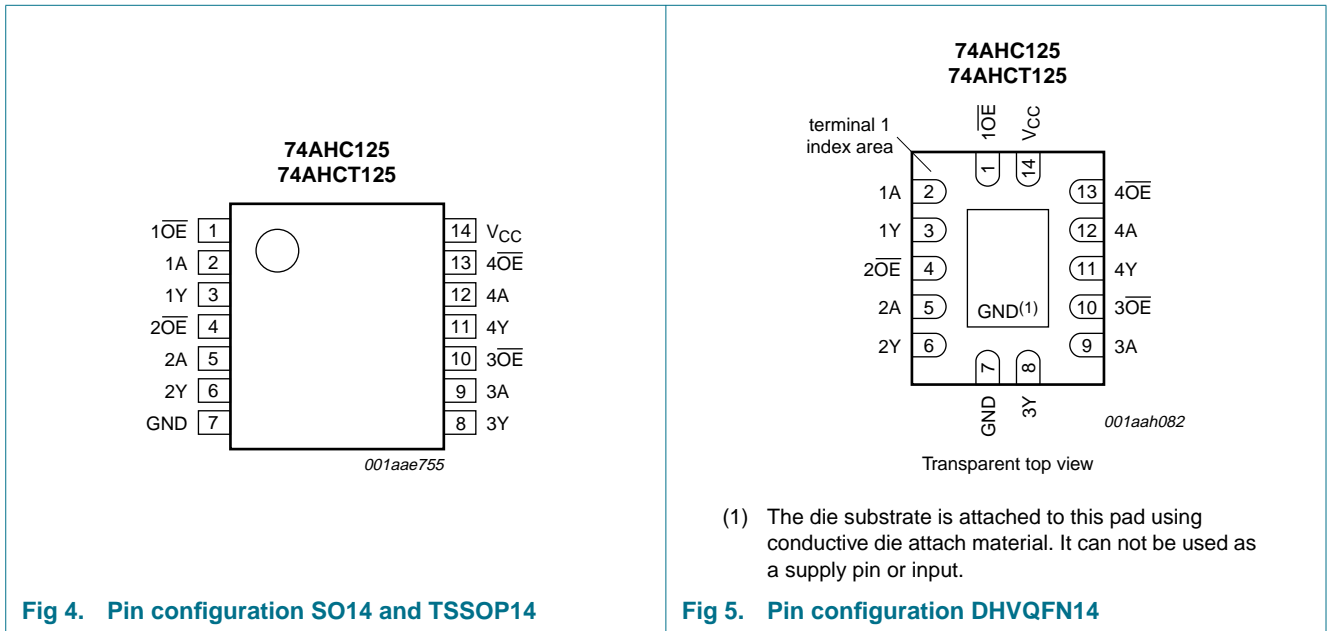
Type number	Package			
	Temperature range	Name	Description	Version
74AHC125D 74AHCT125D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC125PW 74AHCT125PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC125BQ 74AHCT125BQ	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	SOT762-1

## 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
1 $\overline{OE}$	1	output enable input (active LOW)
1A	2	data input
1Y	3	data output
2 $\overline{OE}$	4	output enable input (active LOW)
2A	5	data input
2Y	6	data output
GND	7	ground (0 V)
3Y	8	data output
3A	9	data input
3 $\overline{OE}$	10	output enable input (active LOW)
4Y	11	data output
4A	12	data input
4 $\overline{OE}$	13	output enable input (active LOW)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Control	Input	Output
n $\overline{OE}$	nA	nY
L	L	L
	H	H
H	X	Z

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1] -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>O</sub>	output current	V <sub>O</sub> = -0.5 V to (V <sub>CC</sub> + 0.5 V)	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA

**Table 4. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
	SO14 package		[2] -	500	mW
	TSSOP14 package		[3] -	500	mW
	DHVQFN14 package		[4] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

[3] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

[4] P<sub>tot</sub> derates linearly with 4.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC125			74AHCT125			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74AHC125</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	μA
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF
<b>For type 74AHCT125</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	per input pin; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A V <sub>O</sub> = V <sub>CC</sub> or GND; other pins at V <sub>CC</sub> or GND	-	-	±0.25	-	±2.5	-	±10.0	μA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	μA

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; $I_O = 0$ A; other pins at $V_{CC}$ or GND; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance		-	3.0	10	-	10	-	10	pF
$C_O$	output capacitance		-	4.0	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 GND = 0 V; For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	

**For type 74AHC125**

$t_{pd}$	propagation delay	nA to nY; see <a href="#">Figure 6</a> <sup>[2]</sup>								
		$V_{CC} = 3.0$ V to 3.6 V								
		$C_L = 15$ pF	-	4.4	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50$ pF	-	6.2	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V								
$t_{en}$	enable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		$V_{CC} = 3.0$ V to 3.6 V								
		$C_L = 15$ pF	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50$ pF	-	6.8	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V								
$t_{dis}$	disable time	nOE to nY; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		$V_{CC} = 3.0$ V to 3.6 V								
		$C_L = 15$ pF	-	6.7	9.7	1.0	11.5	1.0	12.5	ns
		$C_L = 50$ pF	-	9.6	13.2	1.0	15.0	1.0	16.5	ns
		$V_{CC} = 4.5$ V to 5.5 V								
$C_{PD}$	power dissipation capacitance	$C_L = 50$ pF; $f_i = 1$ MHz; $V_I =$ GND to $V_{CC}$ <sup>[3]</sup>	-	10	-	-	-	-	-	pF

**Table 7. Dynamic characteristics ...continued**  
*GND = 0 V; For test circuit see Figure 8.*

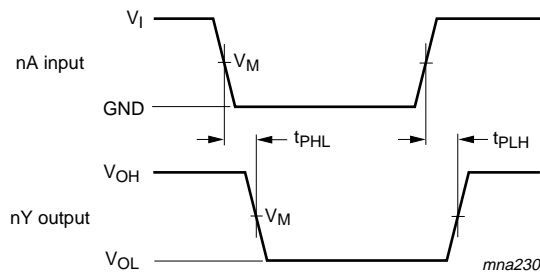
Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>For type 74AHCT125</b>										
t <sub>pd</sub>	propagation delay	nA to nY; see Figure 6 <sup>[2]</sup>								
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		C <sub>L</sub> = 50 pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
t <sub>en</sub>	enable time	nOE to nY; see Figure 7								
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.4	5.1	1.0	6.0	1.0	6.5	ns
		C <sub>L</sub> = 50 pF	-	4.9	7.3	1.0	8.3	1.0	9.5	ns
t <sub>dis</sub>	disable time	nOE to nY; see Figure 7 <sup>[2]</sup>								
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		C <sub>L</sub> = 50 pF	-	6.5	8.8	1.0	10.0	1.0	11.0	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	<sup>[3]</sup>	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
 t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in Volts  
 N = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 11. Waveforms

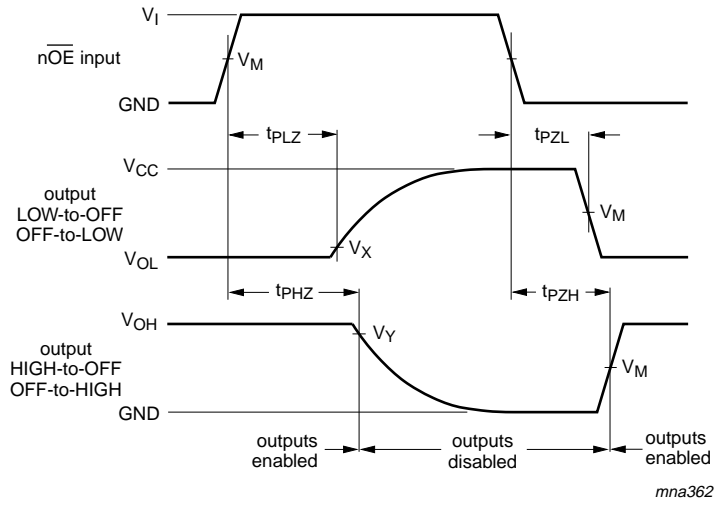


Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 6. Propagation delay input (nA) to output (nY)**





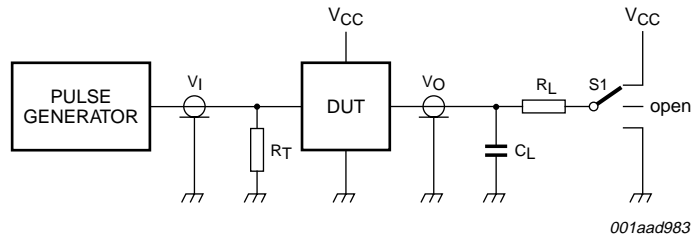
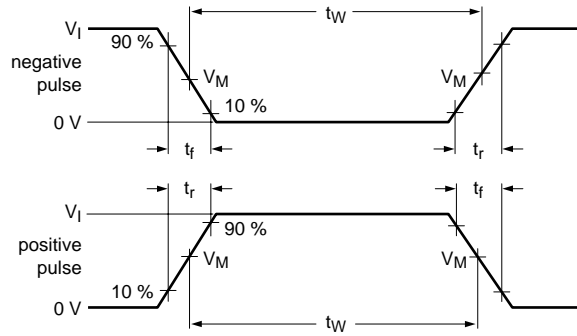
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74AHC125	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OL} - 0.3 V$
74AHCT125	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OL} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig 8. Load circuit for switching times**

**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC125	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT125	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

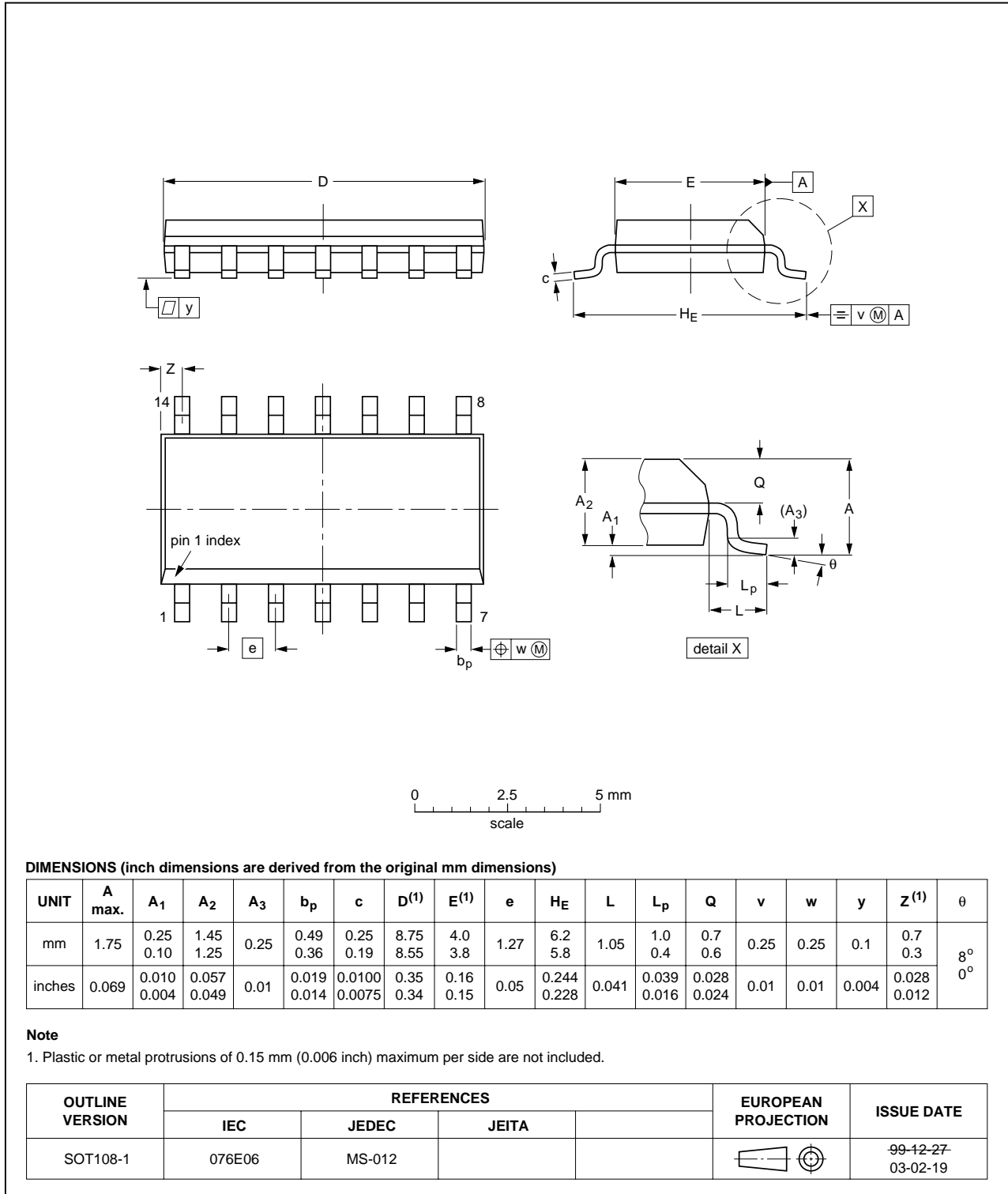


Fig 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

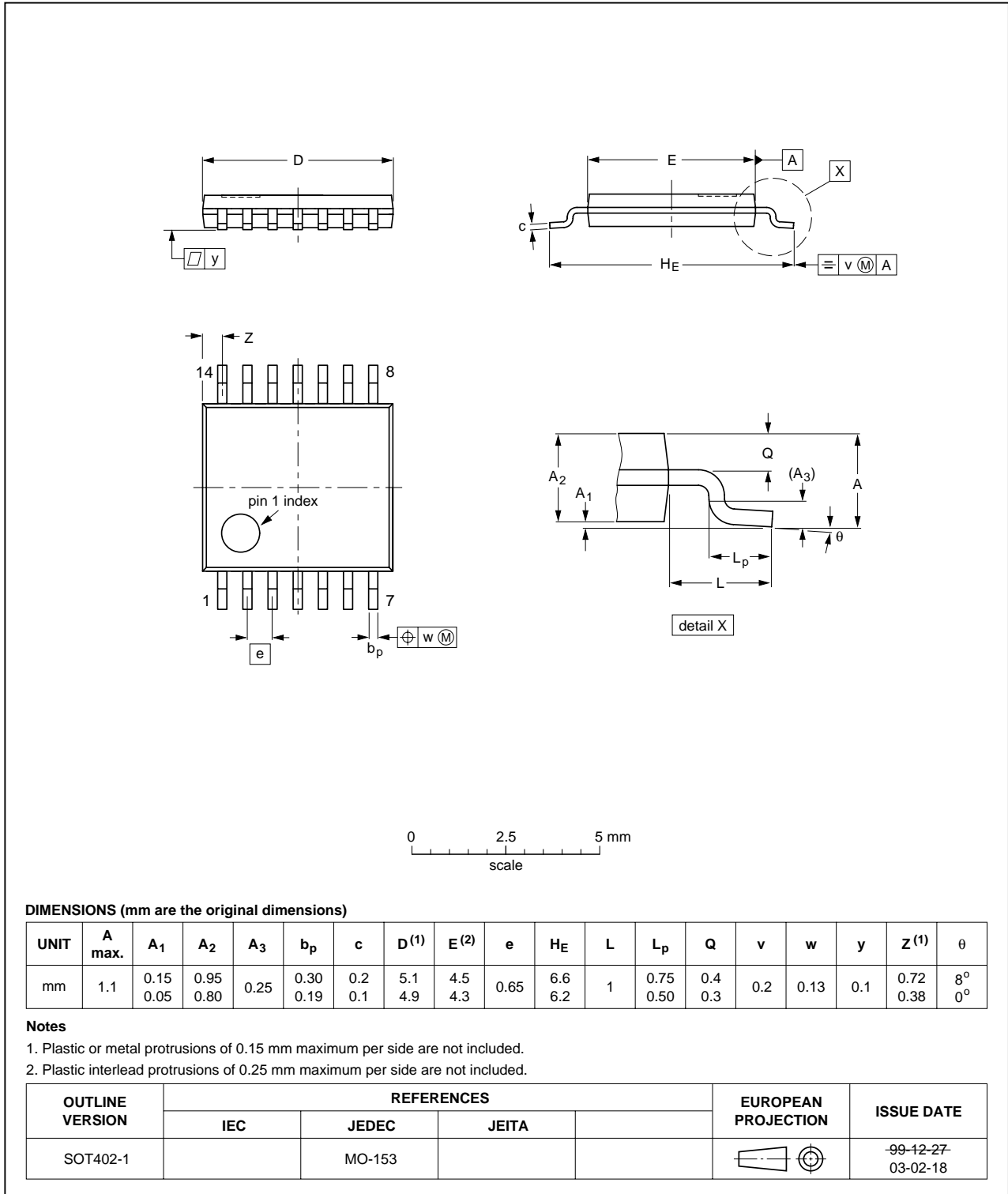
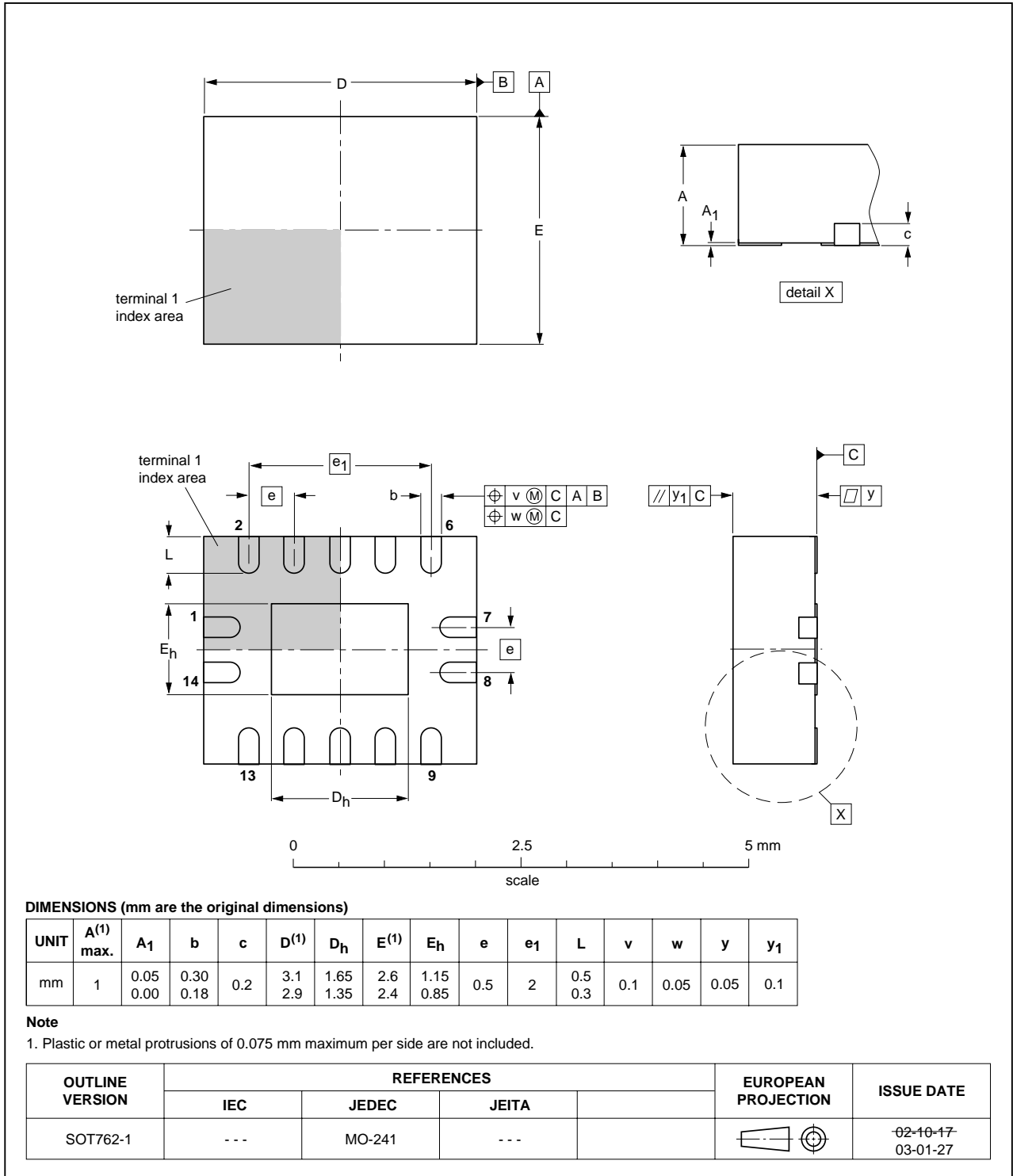


Fig 10. Package outline SOT402-1 (TSSOP14)

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm**

**SOT762-1**



**Fig 11. Package outline SOT762-1 (DHVQFN14)**

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT125_4	20080111	Product data sheet	-	74AHC_AHCT125_3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 3</a>: DHVQFN14 package added.</li> <li>• <a href="#">Section 7</a>: derating values added for DHVQFN14 package.</li> <li>• <a href="#">Section 12</a>: outline drawing added for DHVQFN14 package.</li> </ul>			
74AHC_AHCT125_3	20060324	Product data sheet	-	74AHC_AHCT125_2
74AHC_AHCT125_2	19990927	Product specification	-	74AHC_AHCT125_N_1
74AHC_AHCT125_N_1	19990111	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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