Evaluation Board for Differential Input, Simultaneous Sampling, 12-/14-Bit ADC

EVAL-AD7352/AD7356/AD7357

FEAURES

Full-featured evaluation board for the AD7352, AD7356, and AD7357
EVAL-CED1Z compatible
Standalone capability
On-board analog buffering and voltage reference
Various linking options
PC software for control and data analysis when used with EVAL-CED1Z

GENERAL DESCRIPTION

This data sheet describes the evaluation board for the AD7352, AD7356, and AD7357, which are dual, 12-bit (AD7352 and AD7356) and 14-bit (AD7357), simultaneous sampling successive approximation ADCs. These parts operate from a 2.5 V power supply and a 1.8 V to 3.6 V V_{DRIVE} and feature throughput rates of up to 5 MSPS. Full details on the AD7352, AD7356, and AD7357 are available in the respective data sheets, which are available at www.analog.com, and should be consulted in conjunction with this data sheet when using the evaluation board.

On-board components include two ADR421, 2.5 V, ultrahigh, precision band gap references; two AD8138 single-ended-to-differential converters; and one AD8022 op amp.

Various link options are explained in the Evaluation Board Hardware section. Interfacing to this board is through a 96-way connector. This 96-way connector is compatible with the EVAL-CED1Z, which is available from Analog Devices, Inc. External connectors are provided for a number of signals.

EVALUATION BOARD BLOCK DIAGRAM

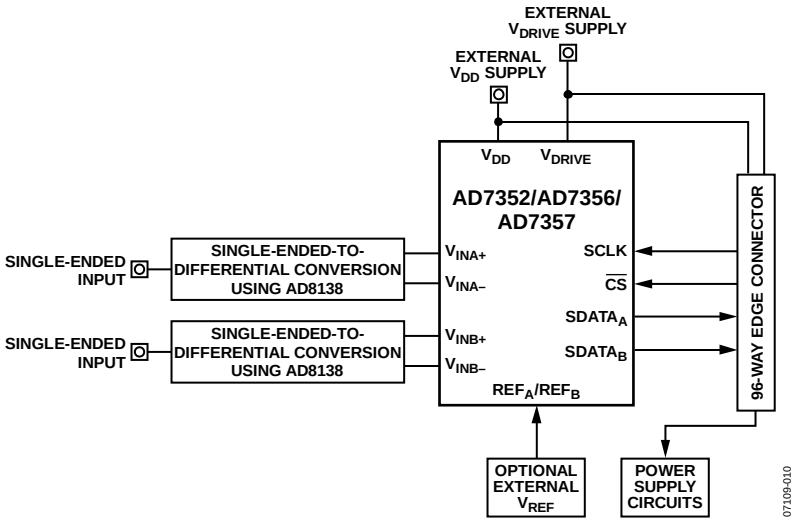

Figure 1.

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REVISION HISTORY

2/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CED1Z, all supplies are provided from the converter evaluation and development (CED) board through the 96-way connector. When using the board as a standalone unit, external supplies must be provided. This evaluation board has the following power supply inputs: V_{DD} (+2.5 V), V_{DRIVE} (+3.3 V), V+ (5 V), V− (−5 V), AGND, and DGND.

The supply pins of all the op amps and references are decoupled to AGND with a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. The AD7352, AD7356, and AD7357 V_{DD} and V_{DRIVE} supply pins are also decoupled to AGND with 10 µF tantalum capacitors and 0.1 µF multilayer ceramic capacitors.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes: AGND and DGND. These are connected at one location close to the AD7352, AD7356, or AD7357.

LINK OPTIONS

There are four link options that must be set for the required operating setup before using the evaluation board. The functions of each option are outlined in Table 1.

There are an additional 21 solder link options for various functions. These link options are outlined in Table 2. These options are initially set up to be EVAL-CED1Z compatible on all boards.

Table 1. Link Option Functions

Link No.	Function
LK1	This link option is used to select the source of the V_{DD} (+2.5 V) supply, which is used to power the AD7352, AD7356, and AD7357. In Position A, V_{DD} is supplied from the CED board through the 96-way connector. In Position B, V_{DD} is supplied from an external source via Power Connector J11.
LK2	This link option selects the source of the V_{DRIVE} (+3.3 V) supply for the AD7352, AD7356, and AD7357. In Position A, V_{DRIVE} is supplied from the CED board. In Position B, V_{DRIVE} must be supplied from an external source via Power Connector J12.
LK3	This link option selects the source of the V− (−5 V) supply for the op amps. In Position A, V− must be supplied from an external source via Power Connector J14. In Position B, V− is supplied from the CED board.
LK4	This link option selects the source of the V+ (+5 V) supply for the op amps. In Position A, V+ must be supplied from an external source via Power Connector J14. In Position B, V+ is supplied from the CED board.

Table 2. Solder Link Option Functions

Link No.	Function
S1	This link selects the source of the SCLK signal for the AD7352, AD7356, and AD7357. If this link is closed, SCLK must be supplied from an external source via SCLK SMB Connector J8.
S2	This link selects the source of the SCLK signal for the AD7352, AD7356, and AD7357. If this link is closed, SCLK is supplied by the CED board.
S3	This link selects the destination of the $SDATA_A$ signal from the AD7352, AD7356, and AD7357. If this link is closed, the $SDATA_A$ signal goes to $SDATA_A$ SMB Connector J9.
S4	This link selects the destination of the SDATAA signal from the AD7352, AD7356, and AD7357. If this link is closed, the $SDATA_A$ signal goes to the CED board through the 96-way connector.
S5	This link selects the destination of the SDATAB signal from the AD7352, AD7356, and AD7357. If this link is closed, the $SDATA_B$ signal goes to $SDATA_B$ SMB Connector J10.
S6	This link selects the destination of the SDATAB signal from the AD7352, AD7356, and AD7357. If this link is closed, the $SDATA_B$ signal goes to the CED board through the 96-way connector.
S7	This link selects the source of the $\overline{CS}$ signal for the AD7352, AD7356, and AD7357. If this link is closed, $\overline{CS}$ must be supplied from an external source via SCLK SMB Connector J7.
S8	This link selects the source of the $\overline{CS}$ signal for the AD7352, AD7356, and AD7357. If this link is closed, $\overline{CS}$ is supplied by the CED board.
S9	If a bipolar analog input source is used, this link should be open. If a unipolar analog input source is used, this link should be closed.
S11	This link selects the source of the common-mode input for the AD8138 op amp that drives ADC A on the AD7352, AD7356, and AD7357. If this link is closed, the common mode is supplied from an external source via EXT COM A Connector J3.
S12	This link selects the source of the SCLK signal for the AD7352, AD7356, and AD7357. If this link is closed, SCLK is supplied by the CED board.

Link No.	Function
S13	This link selects the source of the common-mode input for the AD8138 op amp that drives ADC A on the AD7352, AD7356, and AD7357. If this link is closed, the common mode is supplied from the buffered output of the internal reference.
S14	This link selects the source of the common-mode input for the AD8138 op amp that drives ADC B on the AD7352, AD7356, and AD7357. If this link is closed, the common mode is supplied from an external source via EXT COM B Connector J4.
S16	This link selects the source of the common-mode input for the AD8138 op amp that drives ADC B on the AD7352, AD7356, and AD7357. If this link is closed, the common mode is supplied from the buffered output of the internal reference.
S18	If a bipolar analog input source is used, this link should be open. If a unipolar analog input source is used, this link should be closed.
S19	This link selects whether the source for ADC A is terminated through a 49.9 Ω resistor. If this link is closed, the source is terminated.
S20	This link allows the application of an external reference to ADC A through EXT REF A Connector J5.
S21	This link, when closed, applies a 2.5 V output from the ADR421 reference to ADC A.
S22	This link allows the application of an external reference to ADC B through EXT REF B Connector J6.
S23	This link, when closed, applies a 2.5 V output from the ADR421 reference to ADC A.
S24	This link selects whether the source for ADC B is terminated through a 49.9 Ω resistor. If this link is closed, the source is terminated.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are set according to the required operating mode. There are two modes in which to operate the evaluation board. The user can operate the board either with the CED or as a standalone board. Table 3 shows the position in which all the links and solder links are set when the evaluation board is packaged. When the board is shipped, the assumption is that the user will use the EVAL-AD7352/AD7356/AD7357 with the EVAL-CED1Z. Therefore, the links are set so that all power supplies and control signals are supplied by the EVAL-CED1Z.

Table 3. Link Positions on the EVAL-AD7352/AD7356/AD7357 When Packaged

Link No.	Position	Function
LK1	A	V_{DD} is supplied from the CED through the 96-way connector.
LK2	A	V_{DRIVE} is supplied from the CED.
LK3	B	V− is supplied from the CED.
LK4	B	V+ is supplied from the CED.
S1	Open	N/A.
S2	Closed	SCLK is supplied from the CED.
S3	Open	N/A.
S4	Closed	The $SDATA_A$ signal goes to the CED through the 96-way connector.
S5	Open	N/A.
S6	Closed	The $SDATA_B$ signal goes to the CED through the 96-way connector.
S7	Open	N/A.
S8	Closed	$\overline{CS}$ is supplied by the CED.
S9	Open	N/A.
S11	Open	N/A.
S12	Closed	SCLK is supplied by the CED.
S13	Closed	The common mode for the AD8138 op amp that drives ADC A on the AD7356 and AD7357 is supplied from the buffered output of the internal reference.
S14	Open	N/A.
S16	Closed	The common mode for the AD8138 op amp that drives ADC B on the AD7356 and AD7357 is supplied from the buffered output of the internal reference.
S18	Open	N/A.
S19	Closed	The source for ADC A is to be terminated through a 49.9 Ω resistor.
S20	Open	N/A.
S21	Open	N/A.
S22	Open	N/A.
S23	Open	N/A.
S24	Closed	The source for ADC B is to be terminated through a 49.9 Ω resistor.

INTERFACING THE EVALUATION BOARD TO THE EVAL-CED1Z

Interfacing the EVAL-CED1Z to the AD7352/AD7356/AD7357 evaluation board is via a 96-way connector, J1. The pinout for the J1 connector is shown in Figure 2. Table 4 provides a description of the pins used on the 96-way connector, and Table 5 details the pin designations.

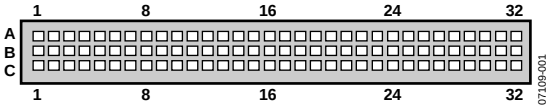

Figure 2. Pin Configuration for the 96-Way Connector, J1

Table 4. The 96-Way Connector Pin Descriptions

Signal	Description
DR0PRI	Data Receive Primary 0. This input is connected to the $SDATA_A$ pin of the AD7352, AD7356, and AD7357 via S4.
DR0SEC	Data Receive Secondary 0. This input is connected to the $SDATA_B$ pin of the AD7352, AD7356, and AD7357 via S12.
DR1PRI	Data Receive Primary 1. This input can also be connected to the $SDATA_B$ pin of the AD7352, AD7356, and AD7357 via S6.
RSCLK0	Receive clock. This continuous clock is connected to the SCLK pin of the AD7352, AD7356, and AD7357 via S2.
RFS0	Receive frame sync. This pin is connected to the $\overline{CS}$ pin of the AD7352, AD7356, and AD7357 via S8 to frame the serial data transfer.
+VARD	Digital +3.3 V supply. This is used to provide the V_{DRIVE} supply to the board via LK2 for the digital logic.
+VARA	Analog +2.5 V supply. This is used to provide the V_{DD} supply to the board via LK1.
DGND	Digital ground. These lines are connected to the digital ground plane on the evaluation board.
AGND	Analog ground. These lines are connected to the analog ground plane on the evaluation board.
AV_{SS} (−5 V)	−5 V supply (V−). This line is connected to the −5 V supply line on the board via LK3.
AV_{CC} (+5 V)	+5 V supply (V+). This line is connected to the +5 V supply line on the board via LK4.

Table 5. 96-Way Connector Pin Functions[1]

Pin	Row A	Row B	Row C
1			DR1PRI
2			
3			
4	DGND	DGND	DGND
5			DR0PRI
6			RFS0
7			RSCLK0
8	+VARD	+VARD	+VARD
9			
10			
11			
12	DGND	DGND	DGND
13			DR0SEC
14			
15			
16	DGND	DGND	DGND
17			
18			
19			
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27	+VARA	AGND	+VARA
28		AGND	
29	AGND	AGND	AGND
30		AGND	
31	AV_{SS} (−5 V)	AV_{SS} (−5 V)	AV_{SS} (−5 V)
32	AV_{CC} (+5 V)	AV_{CC} (+5 V)	AV_{CC} (+5 V)

[1] The unused pins of the 96-way connector are not shown.

SOCKETS

There are 12 SMB input sockets relevant to the operation of the AD7352, AD7356, and AD7357 on this evaluation board. All of these sockets are used for applying an externally generated signal to the evaluation board. When operating the board with the EVAL-CED1Z, the only external sockets necessary are those used to supply the analog inputs to the ADC (that is, VA and VB). All other sockets are optional, and if they are not used, their signals are supplied by the CED. Most of these sockets are used when operating the board as a standalone unit because in this mode of operation all required signals are supplied from external sources. The functions of these sockets are outlined in Table 6.

Table 6. Socket Functions

Socket	Function
VA	Subminiature BNC socket for a single-ended bipolar analog input that is applied to the AD8138 for buffering prior to the VA input of the ADC.
VB	Subminiature BNC socket for a single-ended bipolar analog input that is applied to the AD8138 for buffering prior to the VB input of the ADC.
EXT REF A	Subminiature BNC socket for an external reference voltage to be applied to REFA or to access the internal reference from the AD7352, AD7356, or AD7357.
EXT REF A	Subminiature BNC socket for an external reference voltage to be applied to REFB or to access the internal reference from the AD7352, AD7356, or AD7357.
EXT COM A	Subminiature BNC socket for an external common-mode voltage to be applied to AD8138 common-mode input for ADC A.
EXT COM B	Subminiature BNC socket for an external common-mode voltage to be applied to AD8138 common-mode input for ADC B.
$SDATA_A$	Subminiature BNC socket for $SDATA_A$ output.
$SDATA_B$	Subminiature BNC socket for $SDATA_B$ output.
$\overline{CS}$	Subminiature BNC socket for an external $\overline{CS}$ input.
SCLK	Subminiature BNC socket for an external SCLK input.

CONNECTORS

There are four connectors on the AD7352/AD7356/AD7357 evaluation board, as outlined in Table 7.

Table 7. Connector Functions

Connector	Function
J13	96-way connector for the digital interface and power supply connections.
J11	External V_{DD} and AGND power connector.
J12	External V_{DRIVE} and DGND power connector.
J14	External +5 V, −5 V, and AGND power connector.

OPERATING WITH THE EVAL-CED1Z

The evaluation board can be operated in a standalone mode or in conjunction with the EVAL-CED1Z controller, available from Analog Devices.

When interfacing the AD7352/AD7356/AD7357 evaluation board directly to the CED, all supplies and control signals to operate the AD7352/AD7356/AD7357 evaluation board are provided by the EVAL-CED1Z. When interfacing the respective evaluation board directly to the EVAL-CED1Z, throughput rates of up to 5 MSPS are supported on the AD7356, of up to 3 MSPS are supported on the AD7352, and of up to 4.2 MSPS are supported on the AD7357.

Software to communicate with the EVAL-CED1Z and the AD7352/AD7356/AD7357 evaluation board is provided with the AD7352/AD7356/AD7357 evaluation board package.

The 96-way connector on the AD7352/AD7356/AD7357 evaluation board plugs directly into the 96-way connector on the EVAL-CED1Z. The EVAL-CED1Z provides all the supplies for the evaluation board. It is powered from a 7 V, 15 W power supply that accepts input voltages from 100 V to 240 V ac, and it contains the relevant adaptors for worldwide use. The power supply is provided with the EVAL-CED1Z.

Connection between the EVAL-CED1Z and the USB port of a PC is via a standard USB 2.0 connection cable that is provided as part of the EVAL-CED1Z package.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7352/AD7356/AD7357 evaluation kit includes self-installing software on a CD-ROM for controlling and evaluating the performance of the AD7352, AD7356, or AD7357 when the part is operated with the EVAL-CED1Z. The software is compatible with Windows® 2000/XP®. If the setup file does not run automatically, **setup.exe** can be run from the CD-ROM.

When the CD-ROM is inserted into the PC, an installation program automatically begins. This program installs the evaluation software. The software should be installed before the USB cable is connected between the EVAL-CED1Z and the PC. This ensures that the appropriate USB driver files have been properly installed before the EVAL-CED1Z is connected to the PC.

SETTING UP THE EVAL-CED1Z

This section describes how the evaluation board, the EVAL-CED1Z, and the software should be set up to begin using the complete system.

1. Install the AD7352/AD7356/AD7357 evaluation board software.
2. Connect the EVAL-CED1Z board to the evaluation board via the 96-way connector.
3. Apply power to the EVAL-CED1Z via the 7 V, 15 W power supply provided. At this stage, the green LED labeled **Power** on the EVAL-CED1Z illuminates, indicating that the EVAL-CED1Z is receiving power.
4. Connect the USB cable between the PC and the EVAL-CED1Z. A green LED positioned beside the USB connector on the EVAL-CED1Z board illuminates, indicating that the USB connection has been established.
5. After the EVAL-CED1Z is detected, proceed through any dialog boxes that appear, using the recommended options, to finalize the installation.
6. Start the EVAL-AD7352/AD7356/AD73577 software. In the **Part Information** section on the main menu of the software click the relevant part number from the drop-down box. This sends the FPGA code to the EVAL-CED1Z. The two red LEDs, D14 and D15, on the EVAL-CED1Z illuminate, indicating that the EVAL-CED1Z is functional and ready to receive instructions.

When the software is run for the first time with the EVAL-CED1Z connected to the PC, the PC automatically finds and identifies the new device. Follow the on-screen instructions that appear to install the drivers for the EVAL-CED1Z on the PC. If an error appears on-screen when the software is first opened, then the PC is not recognizing the USB device. This error is corrected by the following procedure:

1. Open the PC **Device Manager**. The **Device Manager** is accessed by right-clicking the **My Computer** icon on the desktop and then selecting **Properties**. When the **System Properties** window opens, select the **Hardware** tab.
2. Click **Device Manager** in the **Hardware** tab of the **System Properties** window.
3. Examine the devices listed under the **Universal Serial Bus Controller** heading.
4. If an unknown device is listed, right-click the option and select **Update Driver**.
5. The **New Hardware Wizard** runs twice, and the following hardware is listed under the **ADI Development Tools**: **ADI Converter Evaluation** and **Development Board (WF)**.
6. Reboot the PC.

SOFTWARE OPERATION

With the hardware set up, you can now use the software to control the EVAL-CED1Z and the AD7352/AD7356/AD7357 evaluation board. To launch the software, select the **AD735x** submenu from the **Analog Devices** menu and then click the **AD735x** icon. Figure 3 displays the main window that opens. If an error message appears, click **OK** and restart the application after checking the connection between the adapter board and the USB port on the PC. In addition, check that the USB device is identified by the **Device Manager**, as detailed in the Setting Up the EVAL-CED1Z section.

The software that controls the AD7352/AD7356/AD7357 evaluation board through the EVAL-CED1Z has four main sections. Figure 3 shows the window that appears when the software is run. The top portion of the window contains the menu bar. The **Part Information** section is on the left side of the window. The **Data Capture** and **Linearity** tabs are in the center of the window, and each consists of a number of subtabs.

USING THE SOFTWARE

Menu Bar

The menu bar consists of the following menus: **File**, **Edit**, and **Help**.

File Menu

Open (Sample Data)

Opens the sample data that has already been saved.

Save (Sample Data)

Saves the sample data that is currently displayed.

Open (Linearity Data)

Opens the linearity data that has already been saved.

Save (Linearity Data)

Saves the linearity data that is currently displayed.

Print Front Panel Picture

Prints the software window that is currently displayed.

Save as Picture

Saves the displayed window plot (that is, waveform, histogram, FFT).

Exit

Closes the software.

Edit Menu

Reinitialize Values to Default

Reinitializes all controls in the main window to their default values.

Help Menu

Open analog.com

Opens the www.analog.com website.

Part Information Tab

The **Part Information** tab allows you to select which evaluation board to use. The sampling frequency for the selected part is changeable. The maximum sample rate is 3 MSPS for the AD7352, 5 MSPS for the AD7356, and 4.2 MSPS for the AD7357. The SCLK frequency is set at 80 MHz for the AD7356 and AD7357 and at 48 MHz for the AD7352. Changing the sampling frequency changes the throughput rate, but does not change the SCLK frequency. The samples taken are uploaded and displayed.

The **Part Information** tab also includes a **Busy** status indicator that illuminates when the evaluation board is busy and an **EXIT** button to allow you to quit the program.

Data Capture Tab

In the **Data Capture** tab, you can select the number of samples to be captured from the drop-down box. The default number of samples is 4096; you are free to change this as required. To initiate a conversion and capture the sample data, click **Sample** or **Continuous**. Both of these buttons are located at the top right corner of the **Data Capture** tab. When you click **Sample**, the software instructs the EVAL-CED1Z board to take the required number of samples at a specific frequency from the evaluation board.

The samples taken are then uploaded and displayed. An FFT and/or histogram can be calculated and displayed. If you click **Continuous**, the software repeats the process indefinitely until you click **Stop**. (The **Continuous** button switches to **Stop** when clicked.) You can switch among displaying data from ADC A, ADC B, or both while the software is running continuously. The desired display option is selected by clicking the **Waveform**, **Histogram**, **FFT**, and **Summary** subtabs.

Waveform Tab

The **Waveform** tab displays a digital storage oscilloscope (DSO) that allows you to display a waveform. When samples are uploaded from the EVAL-CED1Z, they are displayed here. The samples are displayed as integer code values.

At the bottom right of the graph are the zoom options. These allow you to zoom in and out for a closer look at a sample, if required. The **Waveform Analysis** section, which is located beneath the waveform graph, contains information about the samples taken, for example, the minimum/maximum position or frequency, the spread, the standard deviation, and the mean.

The waveform graph displays the information for both ADC A and ADC B or either ADC as desired. Two buttons located on the right side of the graph, labeled **VA ON/OFF** and **VB ON/OFF** are used to select which ADC's data is displayed. An indicator, located on the top right corner of the graph, shows what color graph represents each ADC.

Histogram Tab

This tab displays a histogram of the captured ADC codes. It can be used to provide an indication of the ADC's performance in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken, for example, the maximum and minimum codes captured.

FFT Tab

This tab displays a fast Fourier transform (FFT) plot. The FFT is typically used for examining the ADC's performance in the frequency domain. The **Spectrum Analysis** section contains information about the samples taken, for example, the ac specifications.

You can choose to display the information for ADC A, ADC B, or both in the window using the **VA ON/OFF** and **VB ON/OFF** buttons, as explained in the Waveform Tab section.

Summary Tab

This tab displays a summary of the graphs shown in the **Waveform**, **Histogram**, and **FFT** tabs.

Linearity Tab

In the **Linearity** tab, you can select the maximum number of hits per code. Code 0 and Code 4095 are not included for this calculation. The default number is set at 1000. To initiate conversions and perform the linearity routine, click **Get Linearity Data**. This instructs the EVAL-CED1Z board to take the required number of samples at a specific frequency from the evaluation board. Both the **Max Hits Per Code** control and the **Get Linearity Data** button are located on the top right side of the **Linearity** tab.

The samples are then uploaded and processed. The INL and DNL are calculated during the processing. The results are displayed in the **Histogram**, **DNL**, **INL**, and **Summary** subtabs.

The **Linearity Analysis** is displayed at the bottom of the **Linearity** tab. This section contains information about the samples taken, as well as the worst-case positive (WCP) and worst-case negative (WCN) INL and DNL data.

Histogram Tab

This tab displays a histogram of the captured ADC codes.

DNL Tab

This tab displays a plot of the DNL results.

INL Tab

This tab displays a plot of the INL results.

Summary Tab

This tab displays the histogram, INL, and DNL plots in one window.

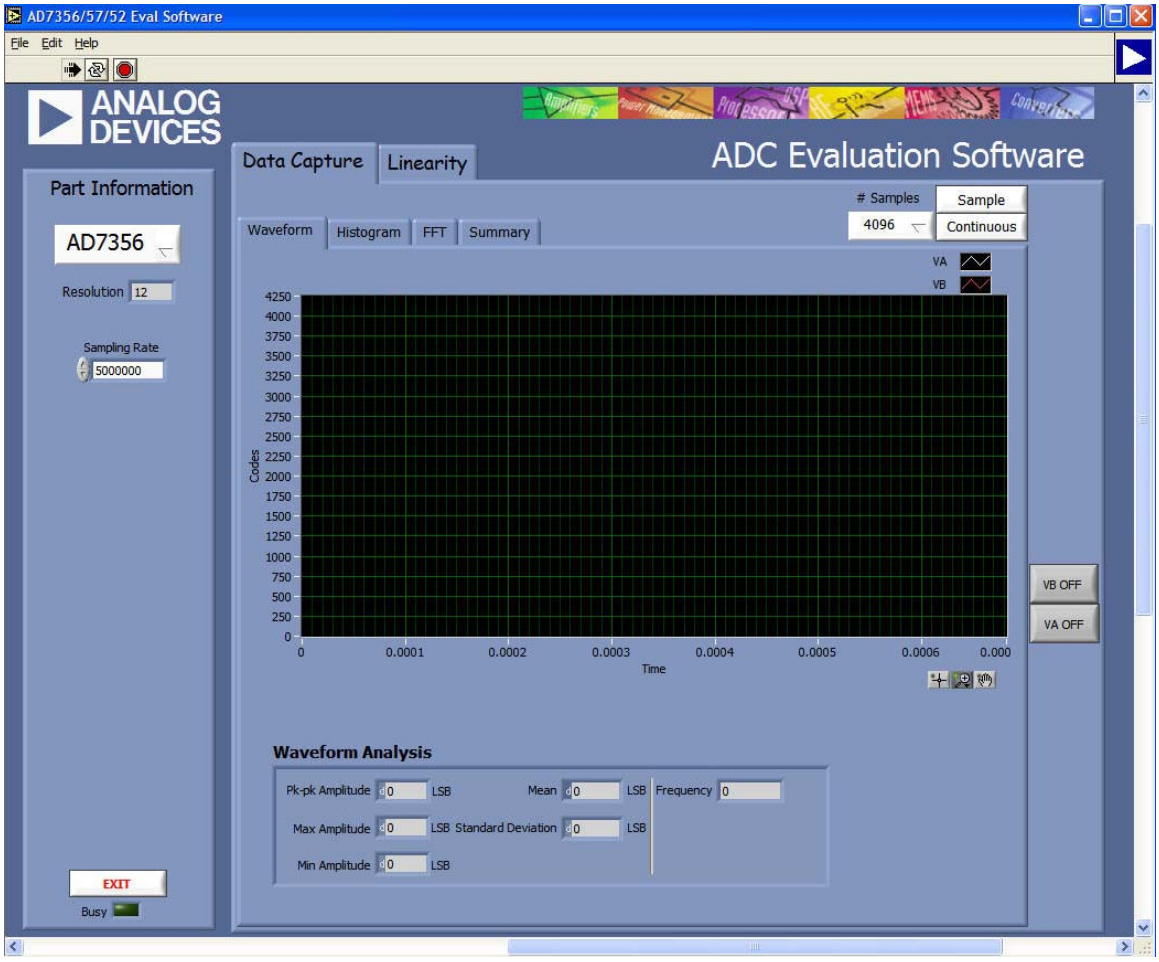

Figure 3. AD7352/AD7356/AD7357 Main Software Window

EVALUATION BOARD SCHEMATICS AND ARTWORK

AD7352/AD7356/AD7357 evaluation board schematics, silkscreen, and layout can be found in Figure 4 to Figure 10.

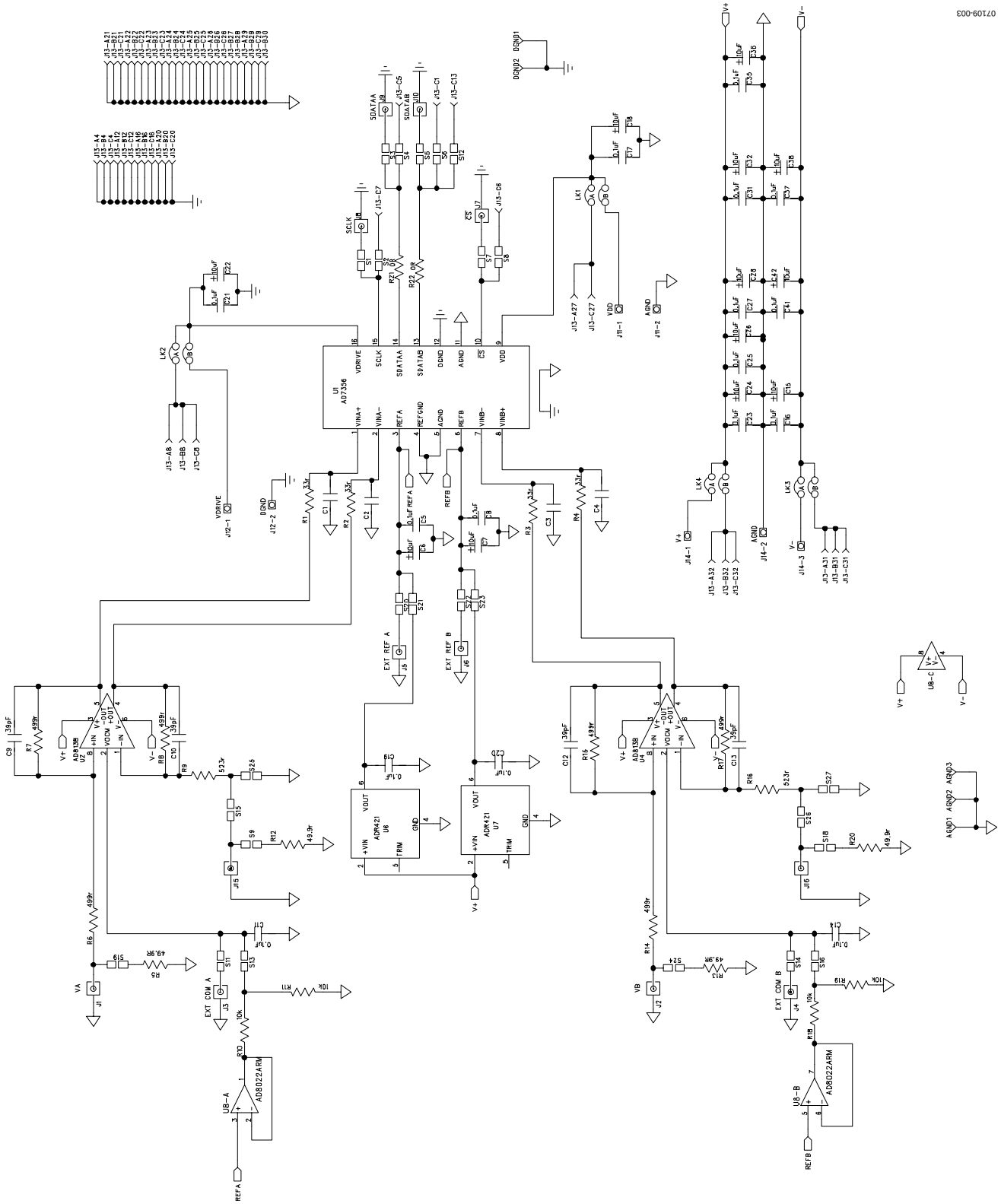

Figure 4. AD7352/AD7356/AD7357 Evaluation Board Circuit Diagram 1

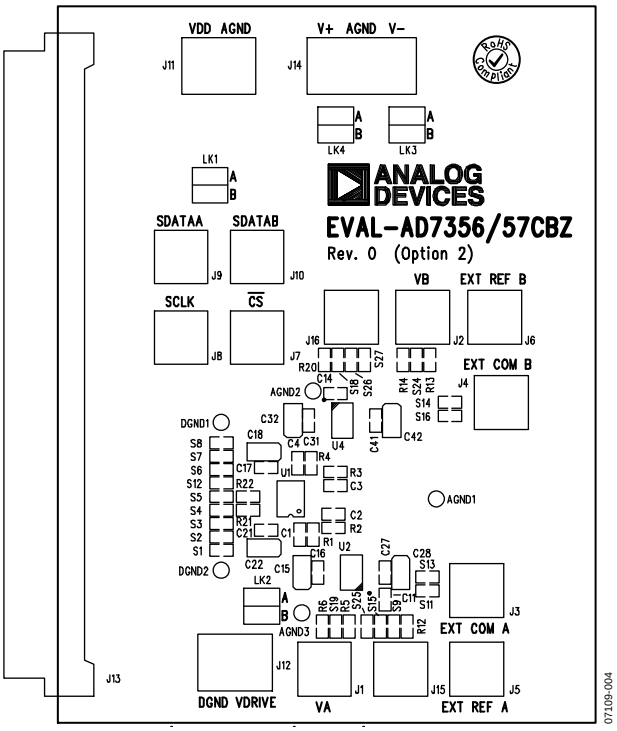

Figure 5. Silkscreen Top

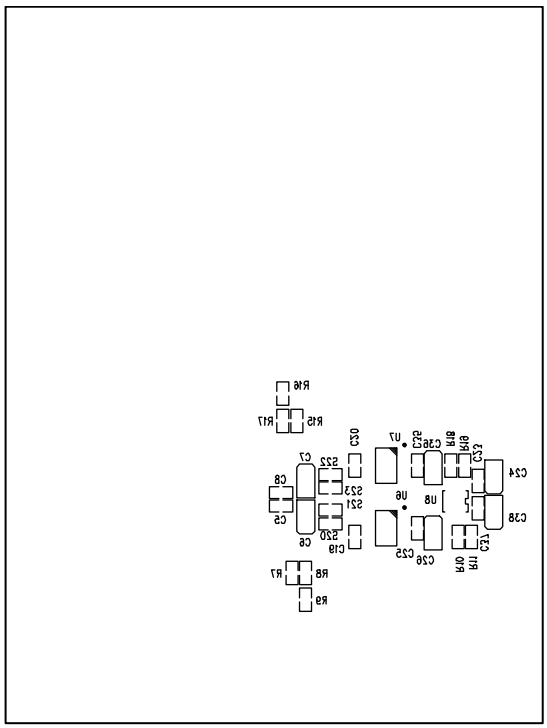

Figure 6. Silkscreen Bottom

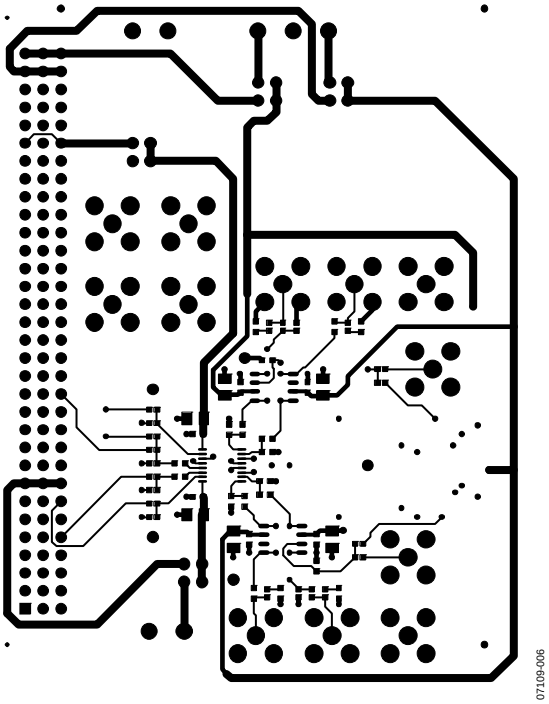

Figure 7. Layer 1 Artwork, Top

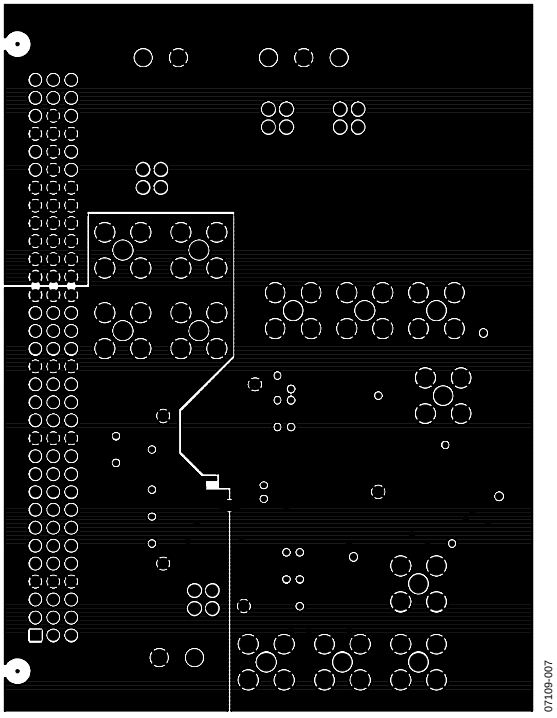

Figure 8. Layer 2 Artwork, Ground Planes

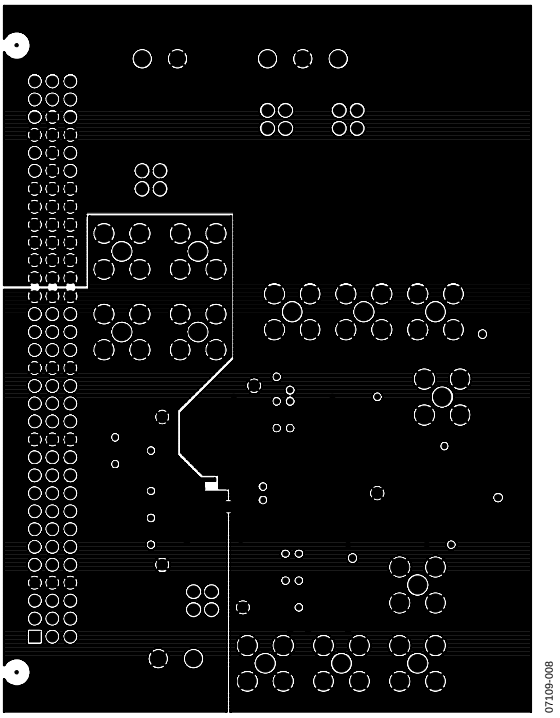

Figure 9. Layer 3 Artwork, Ground Planes

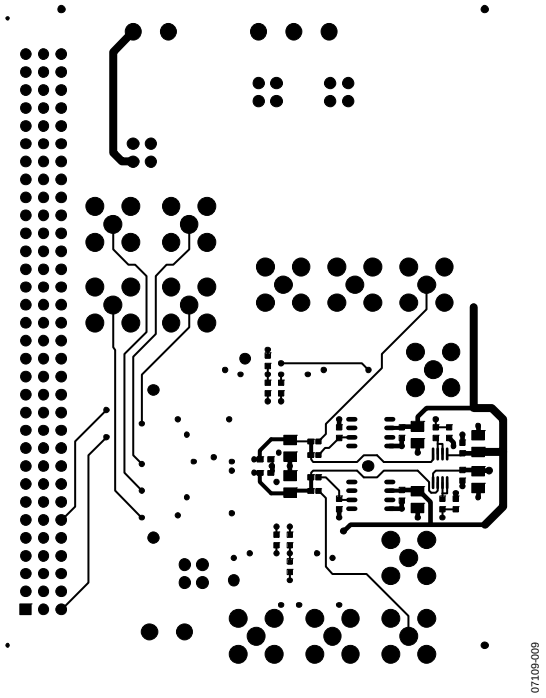

Figure 10. Layer 4 Artwork, Bottom

ORDERING INFORMATION

BILL OF MATERIALS

Table 8.

Qty	Reference Designator	Part Description	Supplier/Part Number[1]
16	C5, C8, C11, C14, C16, C17, C19, C20, C21, C23, C25, C27, C31, C35, C37, C41	Capacitor, SMD, 0603, 100 nF, X7R, 50 V	FEC 1288255
12	C6, C7, C15, C18, C22, C24, C26, C28, C32, C36, C38, C42	Capacitor, 10 µF, 10 V, Case A	FEC 1135105
4	C9, C10, C12, C13	Capacitor, 0603, 39 pF, 50 V	FEC 722030
12	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J15, J16	Jack, SMB, PCB, 50 Ω	FEC 1111349
4	R1, R2, R3, R4	Resistor, 0603, 33 Ω	FEC 9331050
4	R5, R12, R13, R20	Resistor, 0603, 49.9 Ω	FEC 1170658
6	R6, R7, R8, R14, R15, R17	Resistor, 0603, 499 Ω	FEC 1170758
2	R9, R16	Resistor, 0603, 523 Ω	FEC 1170760
4	R10, R11, R18, R19	Resistor, 0603, 10 kΩ	FEC 9330399
2	R21, R22	Resistor, 0603, 0.0 Ω	FEC 9331662
2	J11, J12	Terminal block, PCB, two-way	FEC 1177875
1	J13	Plug, DIN41612, R/A, C, 96-way, PK5	FEC 1097929
1	J14	Terminal block, PCB, three-way	FEC 1177876
1	U1	AD7356 differential input, 12-bit, SAR ADC, 16-lead TSSOP	Analog Devices AD7356BRUZ
2	U2, U4	AD8138 low noise amplifier for 16-bit systems 8-lead SOIC	Analog Devices AD8138ARZ
2	U6, U7	ADR421 2.5 V XFET® voltage reference 8-lead SOIC	Analog Devices ADR421ARZ
1	U8	AD8022 dual high speed, low noise op amp 8-lead MSOP	Analog Devices AD8022ARMZ

[1] FEC refers to Farnell Electronics.

ORDERING GUIDE

Model[1]	Description
EVAL-AD7352EDZ	AD7352 Evaluation Board
EVAL-AD7356EDZ	AD7356 Evaluation Board
EVAL-AD7357EDZ	AD7357 Evaluation Board
EVAL-CED1Z	Converter Evaluation and Development Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.