



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 500 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

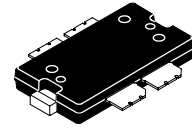
- Typical Single-Carrier N-CDMA Performance @ 465 MHz: $V_{DD} = 28$ Volts, $I_{DQ} = 1100$ mA, $P_{out} = 25$ Watts Avg., IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13). Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
Power Gain — 23 dB
Drain Efficiency — 30.2%
ACPR @ 750 kHz Offset — -47.6 dBc in 30 kHz Bandwidth
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 465 MHz, 125 Watts CW Output Power

Features

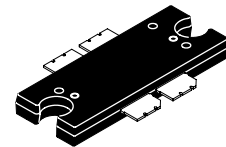
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF5S4125NR1
MRF5S4125NBR1

450-480 MHz, 25 W AVG., 28 V
SINGLE N-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 1486-03, STYLE 1
TO-270 WB-4
MRF5S4125NR1



CASE 1484-04, STYLE 1
TO-272 WB-4
MRF5S4125NBR1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature (1,2)	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 90°C, 125 W CW		0.33	
Case Temperature 90°C, 25 W CW		0.43	

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	10	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 400\ \mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 1100\ \text{mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	3.5	4.25	5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.5\ \text{Adc}$)	$V_{DS(on)}$	0.05	0.175	0.3	Vdc

Dynamic Characteristics (1)

Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	2.41	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	74.61	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1100\ \text{mA}$, $P_{out} = 25\ \text{W Avg. N-CDMA}$, $f = 465\ \text{MHz}$, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ $\pm 750\ \text{kHz}$ Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF.

Power Gain	G_{ps}	22	23	25	dB
Drain Efficiency	η_D	28	30.2	—	%
Adjacent Channel Power Ratio	ACPR	—	-47.6	-45	dBc
Input Return Loss	IRL	—	-15	-9	dB

1. Part internally input matched.

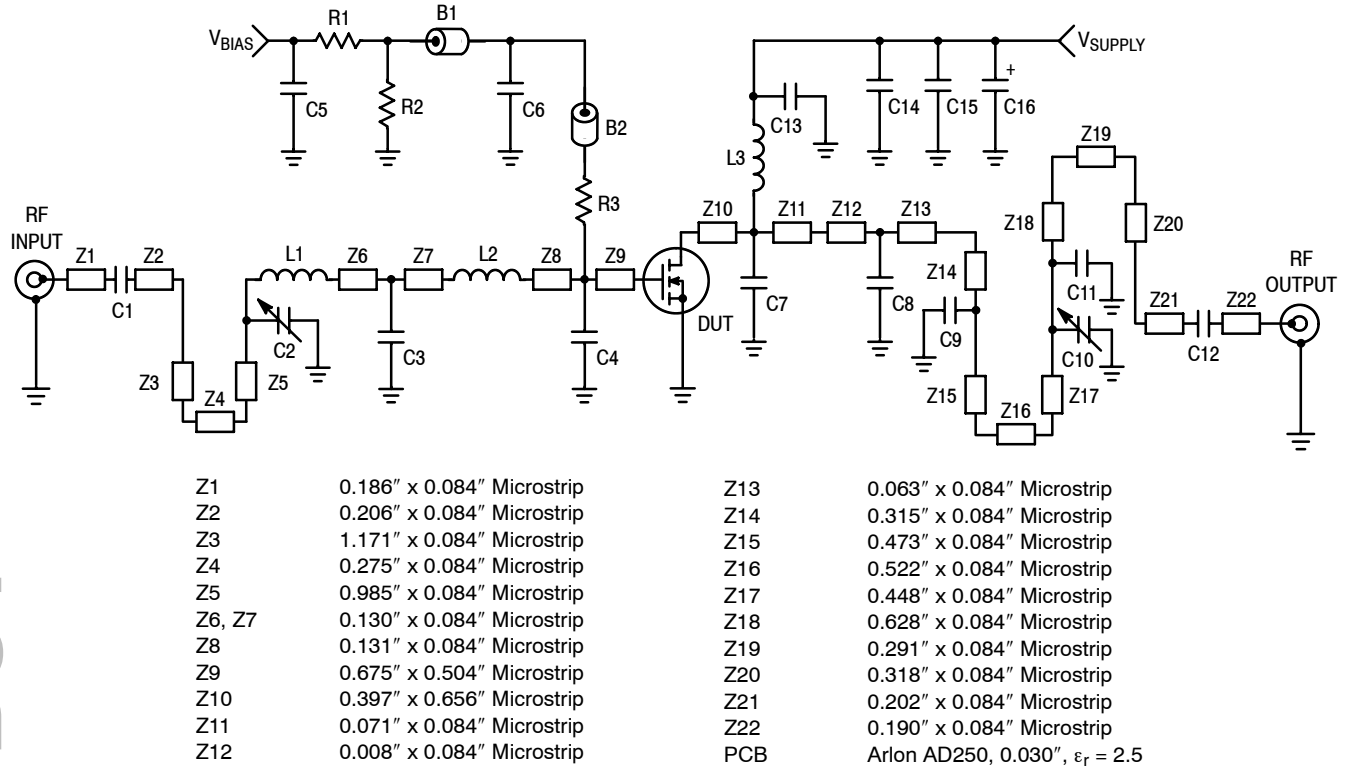


Figure 1. MRF5S4125NR1(NBR1) Test Circuit Schematic

Table 6. MRF5S4125NR1(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1, B2	Ferrite Beads, Short	2743019447	Fair-Rite
C1, C6, C12, C13	120 pF Chip Capacitors	ATC600B121BT250XT	ATC
C2, C10	0.8–8.0 pF, Variable Capacitors, Gigatrim	27291SL	Johanson
C3, C9	20 pF Chip Capacitors	ATC600B200BT250XT	ATC
C4	8.2 pF Chip Capacitor	ATC600B8R2BT250XT	ATC
C5, C14, C15	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C7	27 pF Chip Capacitor	ATC600B270BT250XT	ATC
C8	47 pF Chip Capacitor	ATC600B470BT250XT	ATC
C11	3.3 pF Chip Capacitor	ATC600B3R3BT250XT	ATC
C16	22 μ F, 35 V Tantalum Capacitor	T491X226K035A5	Kemet
L1, L2	1.6 nH Inductors	0906-2	Coilcraft
L3	27 nH Inductor	1812SMS-27N_L	Coilcraft
R1	1000 Ω , 1/4 W Chip Resistor	CRCW12061001FKTA	Vishay
R2	10 k Ω , 1/4 W Chip Resistor	CRCW12061002FKTA	Vishay
R3	100 Ω , 1/4 W Chip Resistor	CRCW1206100RFKTA	Vishay

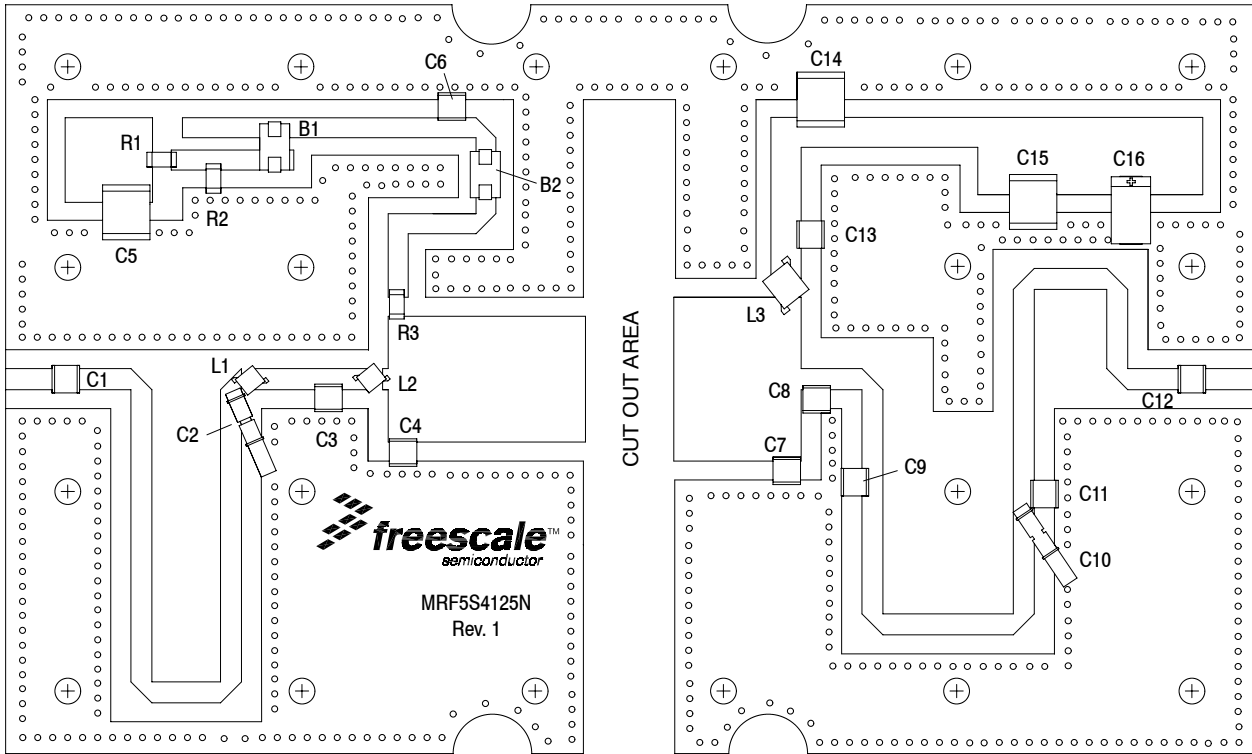


Figure 2. MRF5S4125NR1(NBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

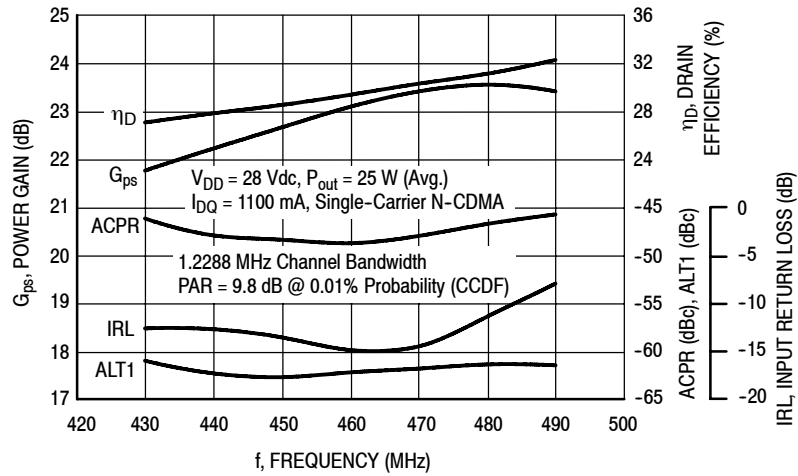


Figure 3. Single-Carrier N-CDMA Broadband Performance @ $P_{out} = 25$ Watts Avg.

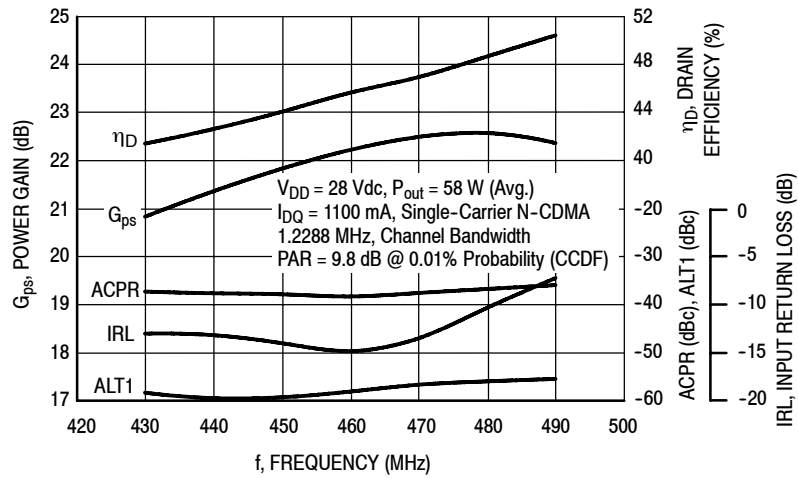


Figure 4. Single-Carrier N-CDMA Broadband Performance @ $P_{out} = 58$ Watts Avg.

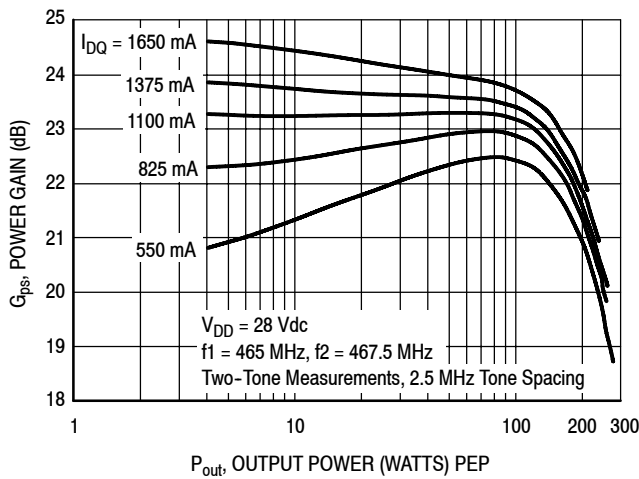


Figure 5. Two-Tone Power Gain versus Output Power

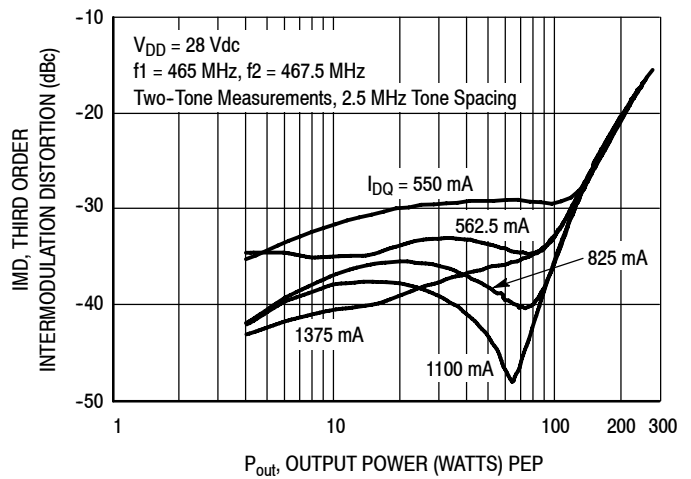


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

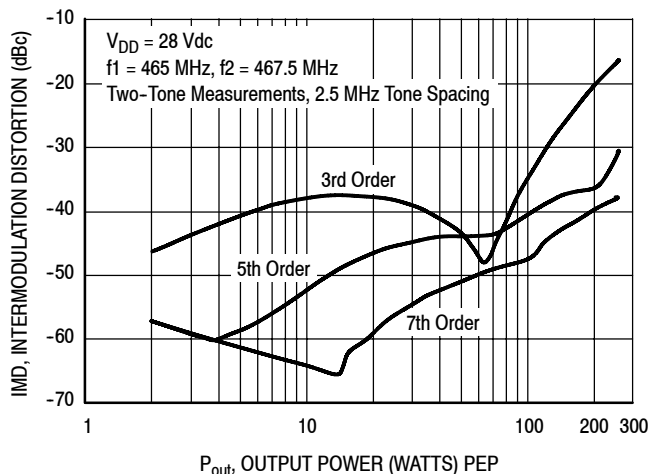


Figure 7. Intermodulation Distortion Products versus Output Power

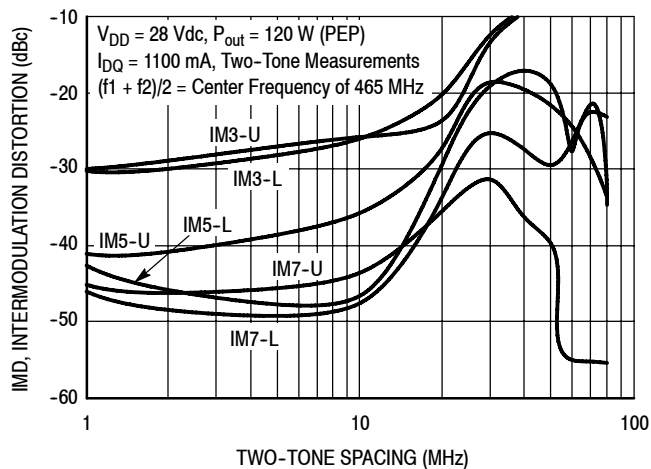


Figure 8. Intermodulation Distortion Products versus Tone Spacing

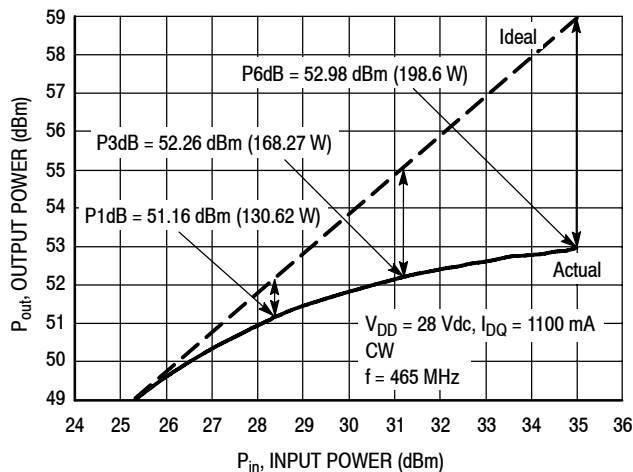


Figure 9. Pulsed CW Output Power versus Input Power

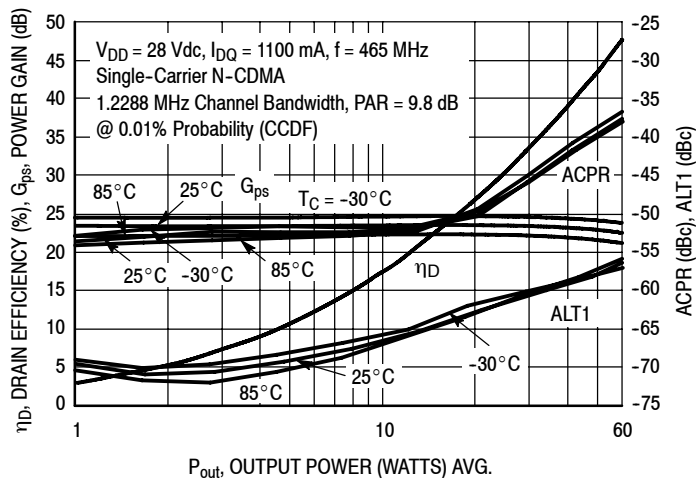


Figure 10. Single-Carrier N-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power

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TYPICAL CHARACTERISTICS

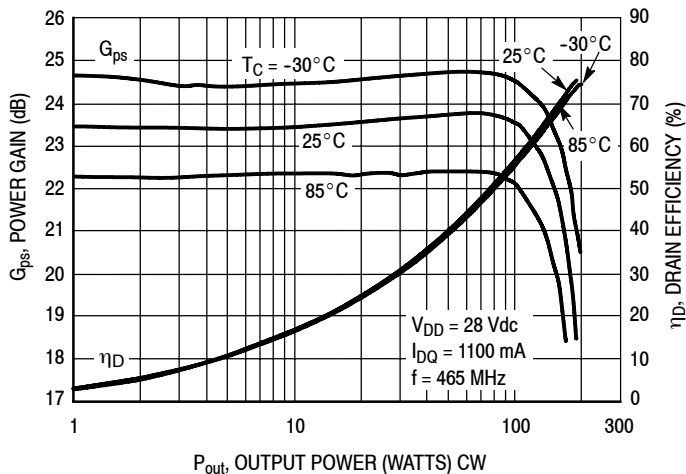


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

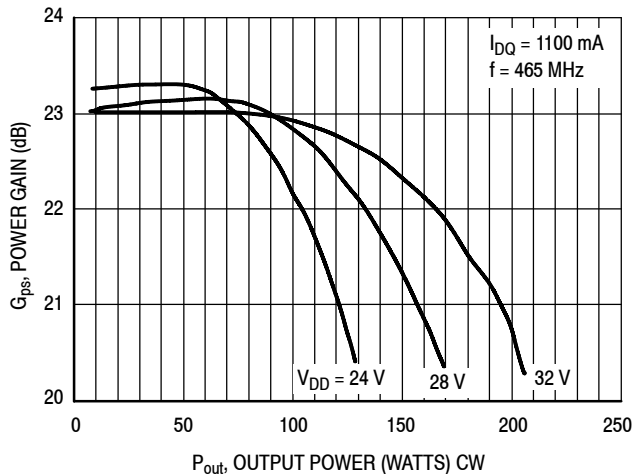
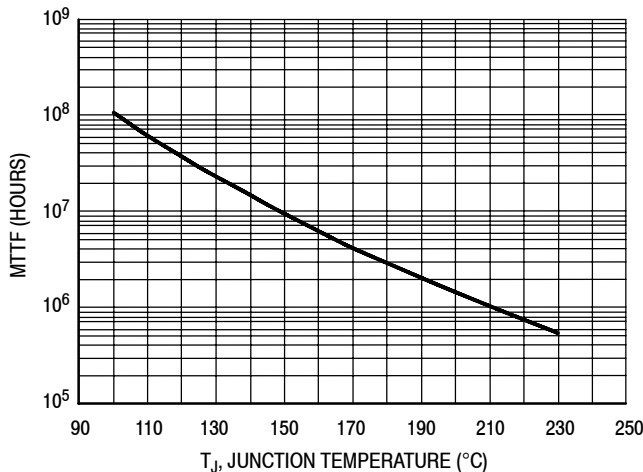


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28\text{ Vdc}$, $P_{out} = 25\text{ W Avg.}$, and $\eta_D = 30.2\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 13. MTTF versus Junction Temperature

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N-CDMA TEST SIGNAL

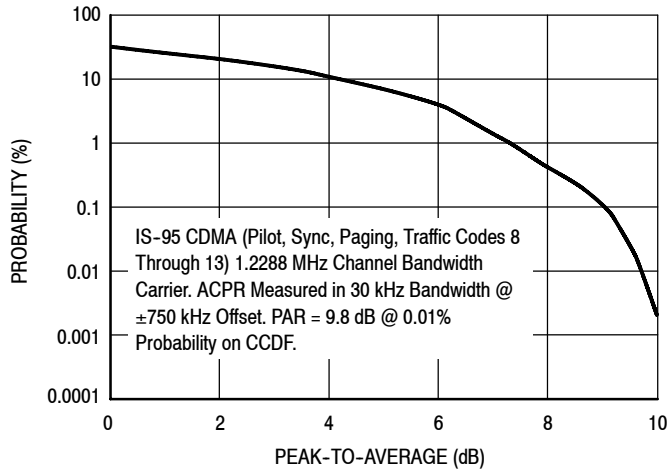


Figure 14. Single-Carrier CCDF N-CDMA

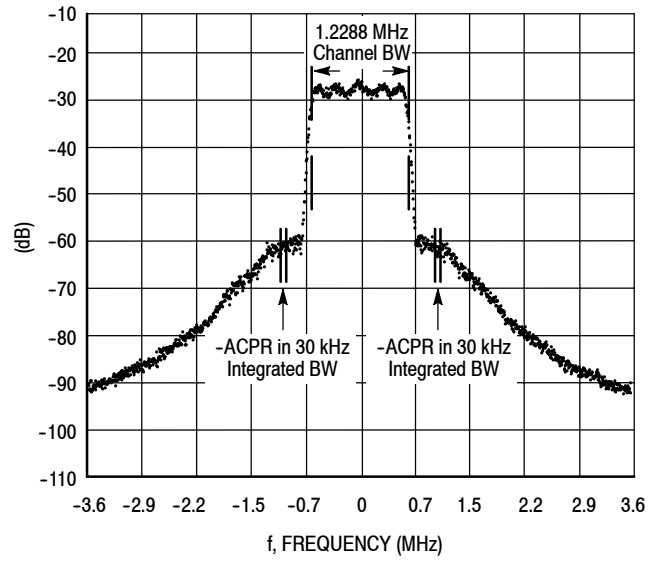
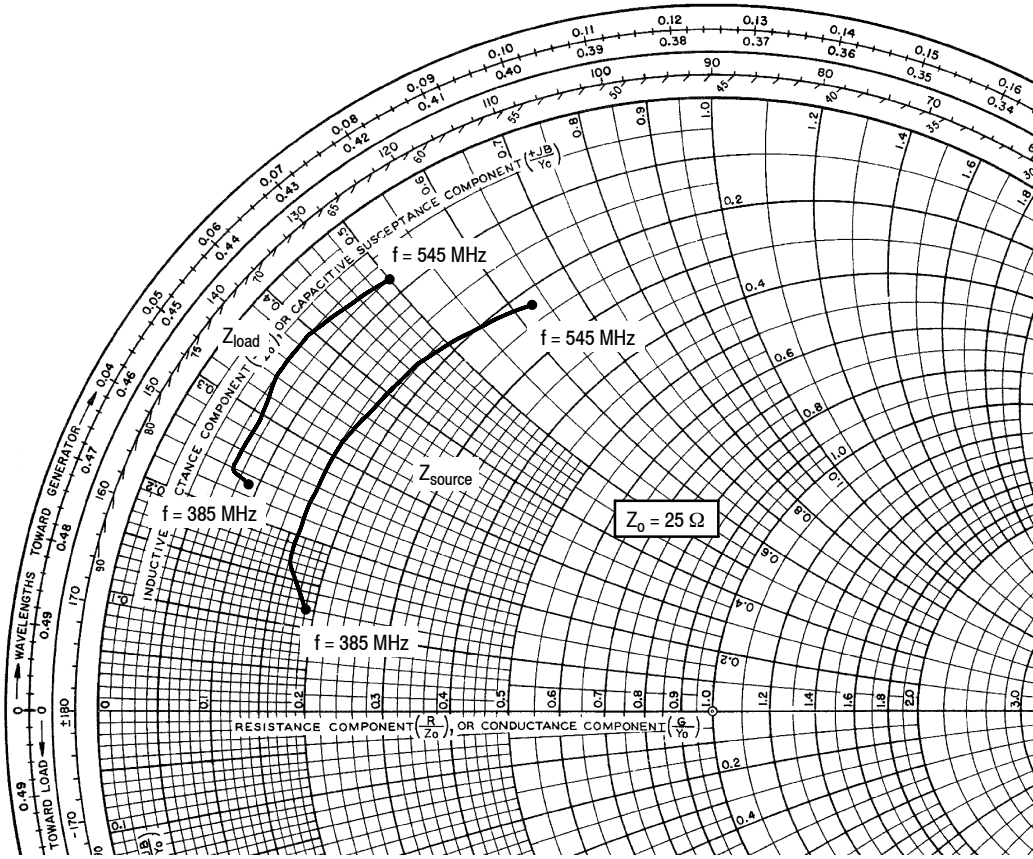


Figure 15. Single-Carrier N-CDMA Spectrum

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$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1100 \text{ mA}$, $P_{out} = 25 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
385	$4.735 + j2.917$	$2.229 + j5.627$
405	$4.073 + j4.202$	$1.809 + j6.123$
425	$3.987 + j5.466$	$1.842 + j6.684$
445	$3.909 + j6.743$	$1.767 + j7.187$
465	$4.094 + j7.661$	$1.822 + j7.338$
485	$4.128 + j9.483$	$1.566 + j8.397$
505	$4.446 + j11.620$	$1.525 + j9.787$
525	$4.921 + j13.710$	$1.769 + j11.120$
545	$5.437 + j15.838$	$2.023 + j12.467$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

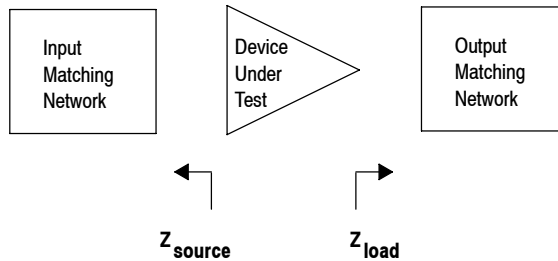
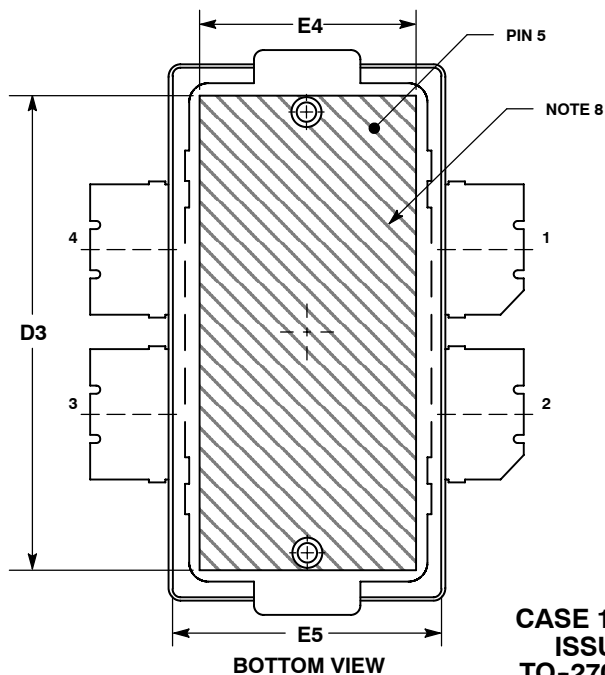
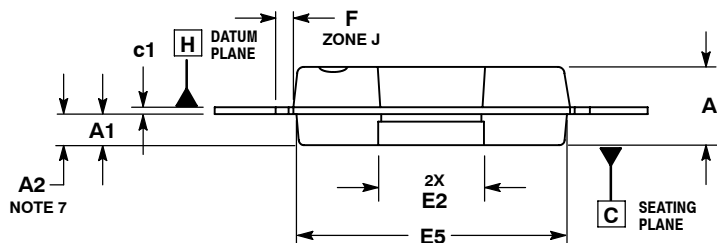
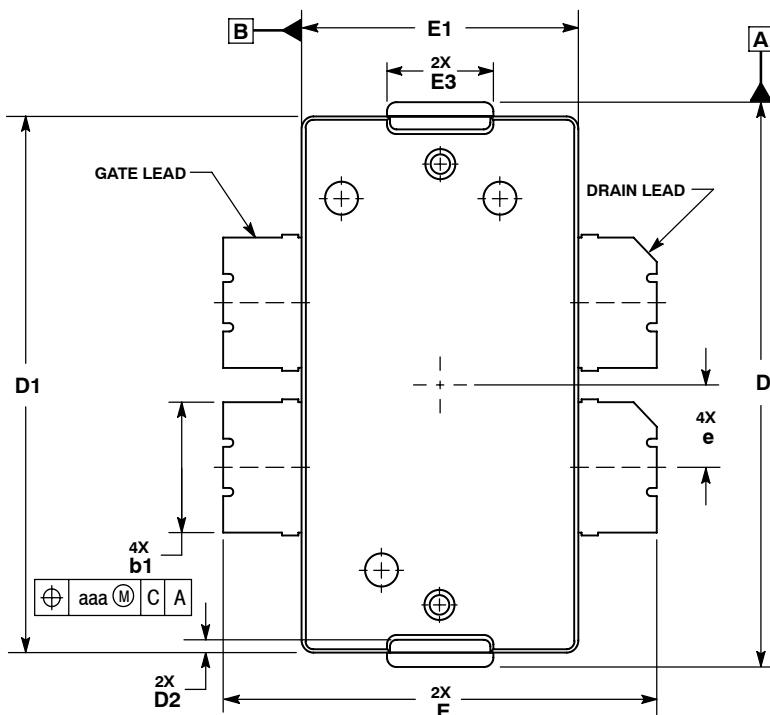


Figure 16. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS

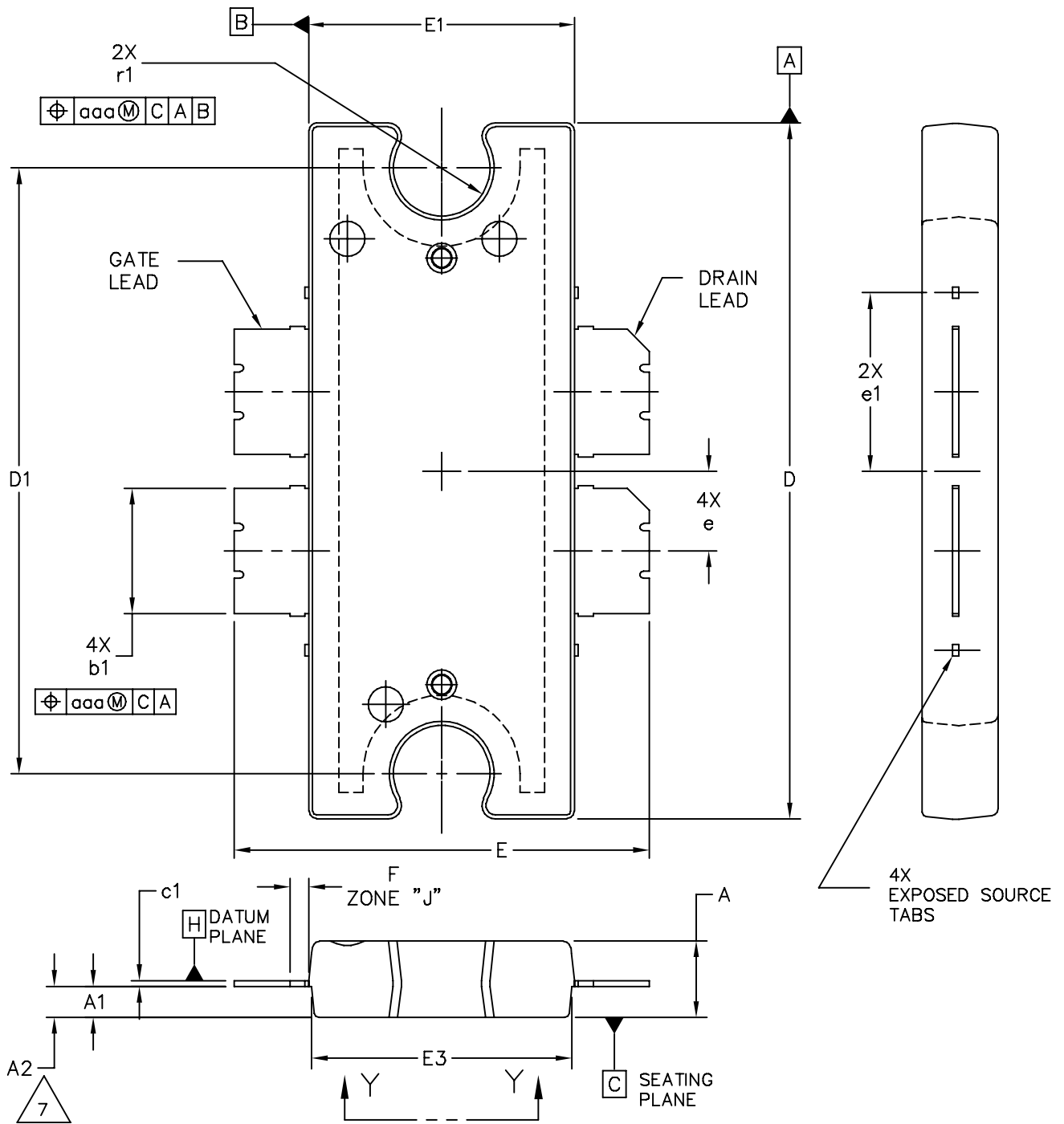


**CASE 1486-03
ISSUE C
TO-270 WB-4
PLASTIC
MRF5S4125NR1**

- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
 4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
 5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
 7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
 8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

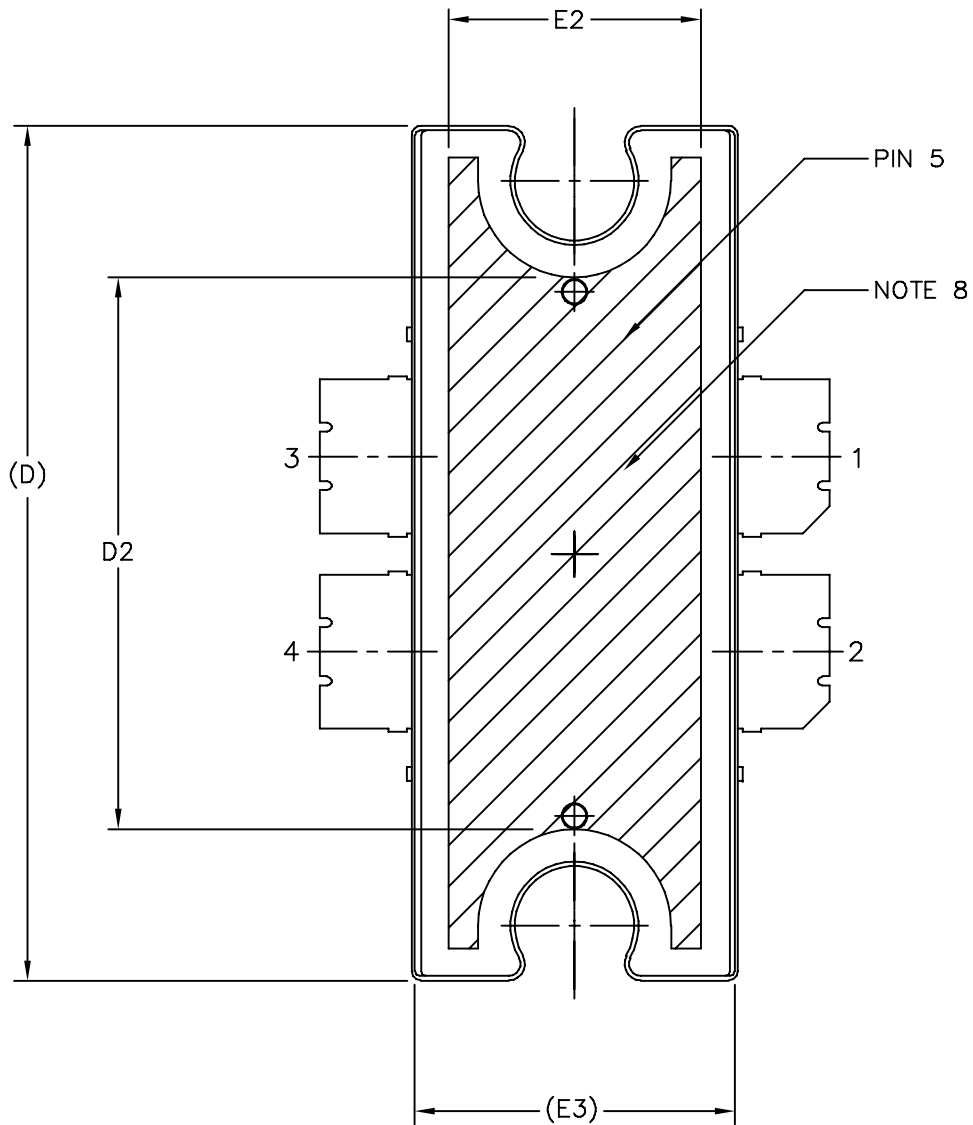
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.712	.720	18.08	18.29
D1	.688	.692	17.48	17.58
D2	.011	.019	0.28	0.48
D3	.600	---	15.24	---
E	.551	.559	14	14.2
E1	.353	.357	8.97	9.07
E2	.132	.140	3.35	3.56
E3	.124	.132	3.15	3.35
E4	.270	---	6.86	---
E5	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	0.18	0.28
e	.106 BSC		2.69 BSC	
aaa	.004		0.10	

- STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE



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		CASE NUMBER: 1484-04		05 APR 2006	
		STANDARD: NON-JEDEC			

MRF5S4125NR1 MRF5S4125NBR1



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	CASE NUMBER: 1484-04	05 APR 2006	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:

PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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MECHANICAL OUTLINE

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 4 LEAD WIDE BODY

DOCUMENT NO: 98ASA10575D

REV: D

CASE NUMBER: 1484-04

05 APR 2006

STANDARD: NON-JEDEC

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2007	• Initial Release of Data Sheet

LIFETIME BUY

LAST ORDER 1 JUL 11 LAST SHIP 30 JUN 12

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