

Ten Output Zero Delay Buffer

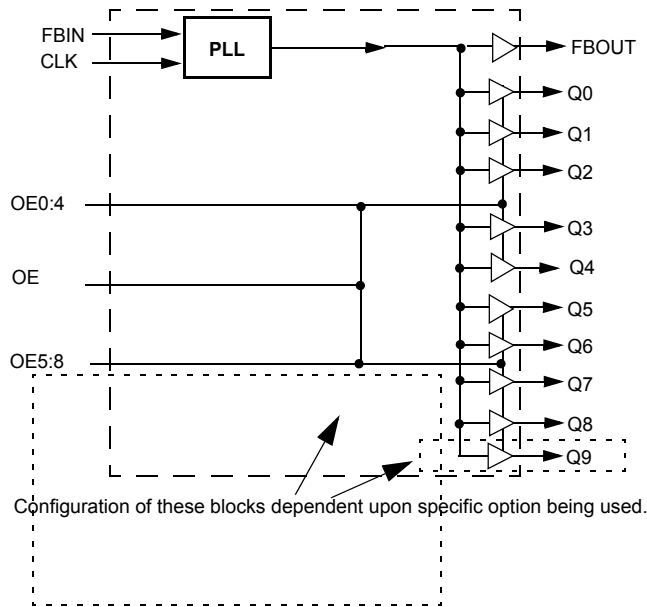
Features

- Well-Suited to both 100 and 133 MHz Designs
- 10 or 11 LVC MOS/LVTTL Outputs
- 3.3V Power Supply
- Available in 24-Pin TSSOP Package

Key Specifications

- Operating Voltage: 3.3V ± 10%
- Operating Range: 25 MHz <math>< f_{OUT} < 140\text{ MHz}</math>
- Cycle-to-Cycle Jitter less than 150 ps
- Output to Output Skew less than 100 ps
- Phase Error Jitter less than 125 ps
- Static Phase Error: less than 150 ps

Logic Block Diagram



Pinouts

Figure 1. 24-Pin TSSOP - W232-09

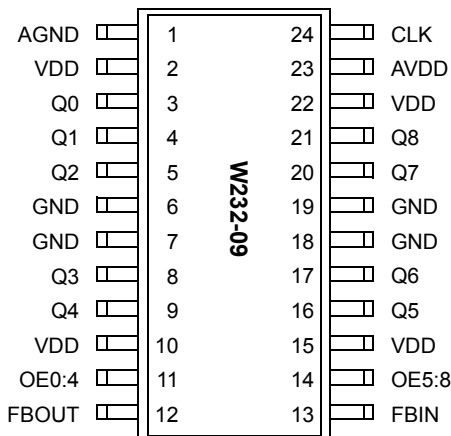
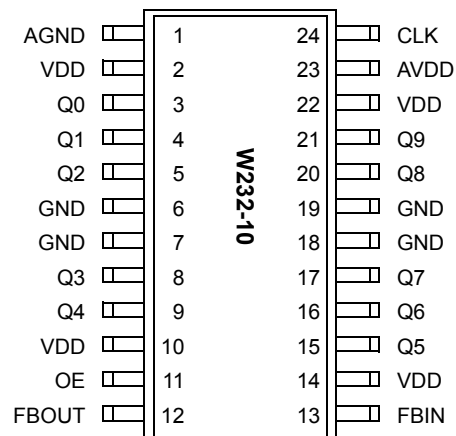


Figure 2. 24-Pin TSSOP - W232-10



Pin Definitions

| Pin Name | Pin No. (-09) | Pin No. (-10) | Pin Type | Pin Description |
|----------|-------------------------------|-----------------------------------|----------|--|
| CLK | 24 | 24 | I | Reference Input: Output signals Q0:9 are synchronized to this signal. |
| FBIN | 13 | 13 | I | Feedback Input: This input must be fed by one of the outputs (typically FBOUT) to ensure proper functionality. If the trace between FBIN and FBOUT is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations are synchronized to the CLK signal input. |
| Q0:8 | 3, 4, 5, 8, 9, 16, 17, 20, 21 | 3, 4, 5, 8, 9, 15, 16, 17, 20, 21 | O | Outputs: The frequency and phase of the signals provided by these pins are equal to the reference signal if properly laid out. |
| FBOUT | 12 | 12 | O | Feedback Output: Typically this is connected directly to the FBIN input with a trace equal in length to the traces between outputs Q0:9 and the destination points of these output signals. |
| AVDD | 23 | 23 | P | Analog Power Connection: Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance. |
| AGND | 1 | 1 | G | Analog Ground Connection: Connect to common system ground plane. |
| VDD | 2, 10, 15, 22 | 2, 10, 14 22 | P | Power Connections: Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance. |
| GND | 6, 7, 18, 19 | 6, 7, 18, 19 | G | Ground Connections: Connect to common system ground plane. |
| OE0:4 | 11 | – | I | Output Enable Input: Tie to V_{DD} (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q0:4 are disabled to a LOW state. |
| OE | – | 11 | I | Output Enable Input: Tie to V_{DD} (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q0:9 are disabled to a LOW state. |
| OE5:8 | 14 | – | I | Output Enable Input: Tie to V_{DD} (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q5:8 are disabled to a LOW state. |

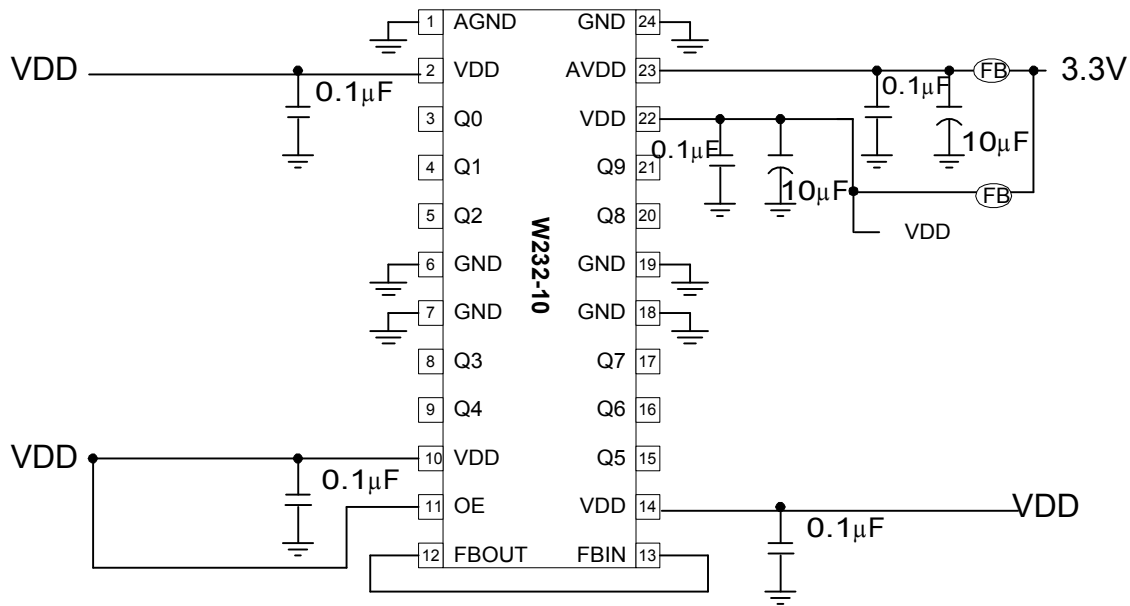
Overview

The W232 is a PLL-based clock driver designed for use in systems requiring a large number of synchronous timing signals. The clock driver has output frequencies of up to 140 MHz and output-to-output skews of less than 100 ps. The W232 provides minimum cycle-to-cycle and long-term jitter, which is of significant importance to meet the tight input-to-input skew budget in DIMM applications.

The W232 was specifically designed to accept SSFTG signals currently being used in motherboard designs to reduce EMI. Zero delay buffers which are not designed to pass this feature through may cause skewing failures.

Output enable pins allow shutdown of output when they are not being used. This reduces EMI and power consumption.

Figure 3. Schematic



Spread Aware

Many systems being designed now use a technology called Spread Spectrum Frequency Timing Generation (SSFTG). Cypress has been one of the pioneers of SSFTG development, and designed this product so as not to filter off the Spread Spectrum (SS) feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on SS timing technology, see the Cypress application note titled, “EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs” - AN1278.

How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. To achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is as follows.

External feedback is the trait that allows this compensation. Since the PLL on the ZDB causes the feedback signal to be in phase with the reference signal, when laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

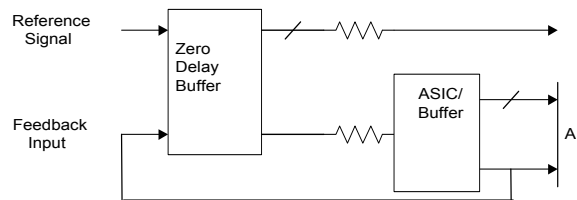
If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals up to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, and so on) which is put into the feedback path.

As shown in Figure 4, if the traces between the ASIC/buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device are driven HIGH at the same time the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is, however, more complex as any propagation delay in the ASIC/Buffer must be accounted for.

Figure 4. 6 Output Buffer in the Feedback Path



Absolute Maximum Ratings^[1]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter | Description | Rating | Unit |
|------------------|--|--------------|------|
| V_{DD}, V_{IN} | Voltage on any Pin with Respect to GND | -0.5 to +7.0 | V |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_A | Operating Temperature | 0 to +70 | °C |
| T_B | Ambient Temperature under Bias | -55 to +125 | °C |
| P_D | Power Dissipation | 0.5 | W |

DC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 10\%$

| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|-----------|---------------------|--------------------------|-----|-----|-----|---------------|
| I_{DD} | Supply Current | Unloaded, 100 MHz | | | 200 | mA |
| V_{IL} | Input Low Voltage | | | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 12\text{ mA}$ | | | 0.8 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -12\text{ mA}$ | 2.1 | | | V |
| I_{IL} | Input Low Current | $V_{IN} = 0\text{V}$ | | | 50 | μA |
| I_{IH} | Input High Current | $V_{IN} = V_{DD}$ | | | 50 | μA |

AC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$

| Parameter | Description | Test Condition | Min | Typ | Max | Unit |
|----------------|--|----------------------------|------|-----|-----|------|
| f_{OUT} | Output Frequency | 30-pF load ^[5] | 25 | | 140 | MHz |
| t_R | Output Rise Time | 0.8V to 2.0V, 30-pF load | | | 2.1 | ns |
| t_F | Output Fall Time | 2.0V to 0.8V, 30-pF load | | | 2.5 | ns |
| $t_{l_{CLKR}}$ | Input Clock Rise Time ^[2] | | | | 4.5 | ns |
| $t_{l_{CLKF}}$ | Input Clock Fall Time ^[2] | | | | 4.5 | ns |
| t_{PEJ} | CLK to FBIN Skew Variation ^[3, 4] | Measured at $V_{DD}/2$ | -350 | 0 | 350 | ps |
| t_{SK} | Output to Output Skew | All outputs loaded equally | -100 | 0 | 100 | ps |
| t_D | Duty Cycle | 30-pF load | 43 | 50 | 58 | % |
| t_{LOCK} | PLL Lock Time | Power supply stable | | | 1.0 | ms |
| t_{JC} | Jitter, Cycle-to-Cycle ^[5] | | | | 150 | ps |

Notes

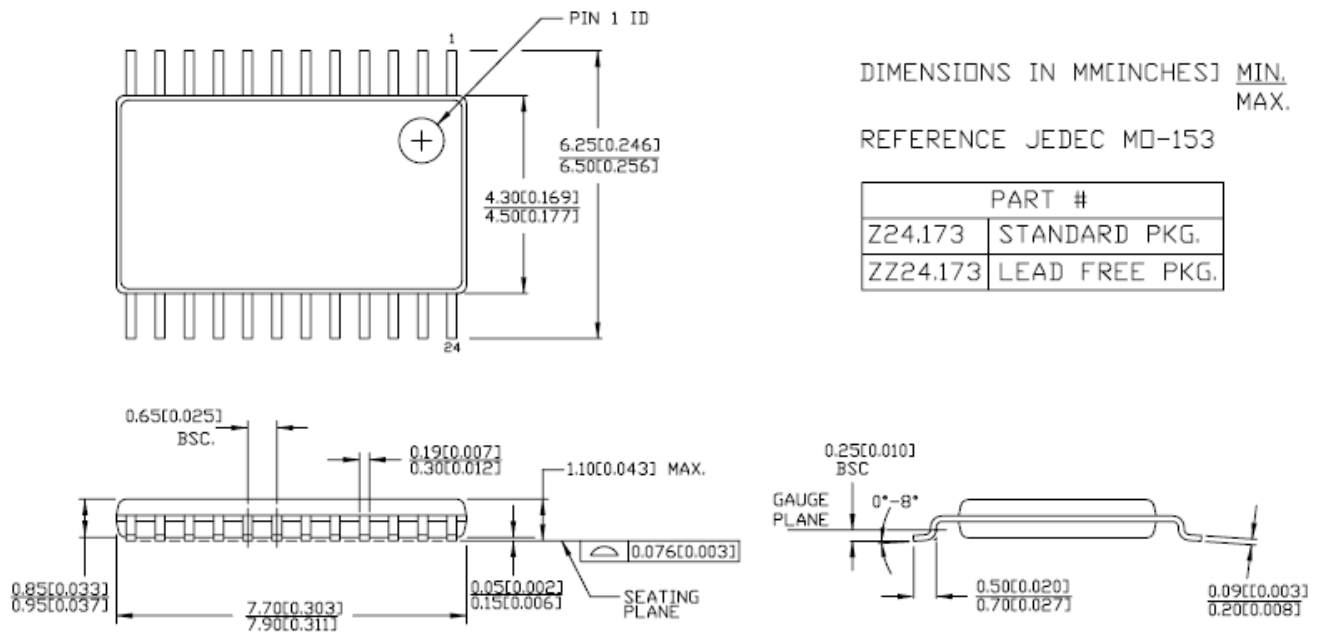
- Multiple Supplies: The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
- Longer input rise and fall time degrades skew and jitter performance.
- Skew is measured at $V_{DD}/2$ on rising edges.
- Duty cycle is measured at $V_{DD}/2$.
- Production tests are run at 133 MHz.
- For frequencies below 40 MHz, Cycle-to-Cycle Jitter degrades to 175 ps.

Ordering Information

| Ordering Code | Status | Package Type |
|----------------|----------|---------------------------|
| W232-09X | Obsolete | 24-pin TSSOP |
| W232-09XT | Obsolete | 24-pin TSSOP, Tape & Reel |
| W232-10X | Active | 24-pin TSSOP |
| W232-10XT | Active | 24-pin TSSOP, Tape & Reel |
| Pb-Free | | |
| W232ZXC-10 | Active | 24-pin TSSOP |
| W232ZXC-10T | Active | 24-pin TSSOP, Tape & Reel |

Package Diagram

Figure 5. 24-Pin Thin Shrink Small Outline Package (TSSOP)



51-85119-A

Document History Page

| Document Title: W232 Ten Output Zero Delay Buffer | | | | |
|---|---------|-----------------|-----------------|--|
| Document Number: 38-07167 | | | | |
| REV. | ECN NO. | Submission Date | Orig. of Change | Description of Change |
| ** | 110277 | 10/25/01 | SZV | Change from Spec number: 38-00827 to 38-07167 |
| *A | 111278 | 03/22/02 | IKA | Put package type in order information table for TSSOP |
| *B | 122808 | 12/15/02 | RBI | Add Power up Requirements to Operating Conditions Information |
| *C | 2548211 | 08/15/08 | LJN | Obsolete spec |
| *D | 2635369 | 01/21/09 | KVM | Updated template Un-obsolete spec Indicate W232-09 is obsolete in Ordering Information table |
| *E | 2699171 | 04/28/2009 | KVM/PYRS | Added Ordering Information Table |

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