

ActiveQRTM Quasi-Resonant PWM Controller

FEATURES

- CCM and Quasi-Resonant Operation
- Adjustable up to 45kHz Switching Frequency
- OCP/OLP Protection
- Integrated Patented Frequency Foldback Technique
- Integrated Patented Line Compensation
- Built-in Soft-Start Circuit
- Line Under-Voltage, Thermal, Output Over-voltage, Output Short Protections
- Current Sense Resistor Short Protection
- Transformer Winding Short Protection
- 100mW Standby Power
- Complies with Global Energy Efficiency and CEC Average Efficiency Standards
- Tiny SOT23-6 Packages

APPLICATIONS

- AC/DC Adaptors/Chargers for Cell Phones, Cordless Phone, PDAs, E-books
- Adaptors for Portable Media Player, DSCs, Set-top boxes, DVD players, records
- Linear Adapter Replacements

GENERAL DESCRIPTION

The ACT513 is a high performance peak current mode PWM controller. ACT513 applies *ActiveQRTM* and frequency foldback technique to reduce EMI and improve efficiency. ACT513's maximum design switching frequency is set at 45kHz. Very low standby power, good dynamic response and accurate voltage regulation is achieved with an opto-coupler and the secondary side control circuit.

The idle mode operation enables low standby power of 100mW with small output voltage ripple. By applying frequency foldback and *ActiveQRTM* technology, ACT513 increases the average system efficiency compared to conventional solutions and exceeds the latest ES2.0 efficiency standard with good margin.

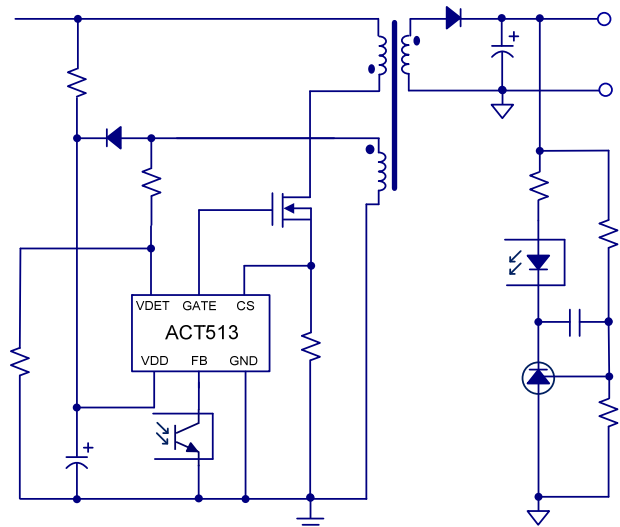
ACT513 integrates comprehensive protection. In case of over temperature, over voltage, winding short, current sense resistor short, open loop and overload conditions, it would enter into auto restart mode including Cycle-by-Cycle current limiting.

ACT513 is to achieve no overshoot and very short rise time even with a big capacitive load with the built-in fast and soft start process.

In full load condition, ACT513 is able to be designed to work in both CCM mode and DCM mode to meet different types of applications. Quasi-Resonant (QR) operation mode can improve efficiency during DCM operation, and reduce EMI and further reduce the components in input filter.

ACT513 is ideal for applications up to 60 Watts.

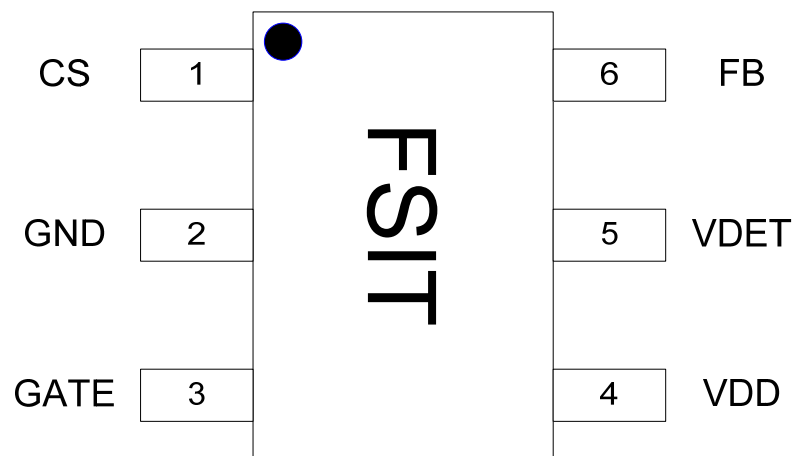
Figure 1:
Simplified Application Circuit



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT513US-T	-40°C to 85°C	SOT23-6	6	TUBE & REEL	FSIT

PIN CONFIGURATION



SOT23-6
ACT513US

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch.
2	GND	Ground.
3	GATE	Gate Drive. Gate driver for the external MOSFET transistor.
4	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
5	VDET	Valley Detector Pin. Connect this pin to a resistor divider network from the auxiliary winding to detect zero-crossing points for valley turn on operation.
6	FB	Feedback Pin. Connect this pin to optocouplers's collector for output regulation.

ABSOLUTE MAXIMUM RATINGS^①

PARAMETER	VALUE	UNIT
FB, CS, VDET to GND	-0.3 to + 6	V
VDD, GATE to GND	-0.3 to + 28	V
Maximum Power Dissipation (SOT23-6)	0.45	W
Operating Junction Temperature	-40 to 150	°C
Junction to Ambient Thermal Resistance (θ_{JA})	220	°C/W
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 14V$, $L_M = 4mH$, $R_{CS} = 1.27\Omega$, $V_{OUT} = 12V$, $N_P = 122$, $N_S = 14$, $N_A = 15$, $T_A = 25^\circ C$, unless otherwise specified.)

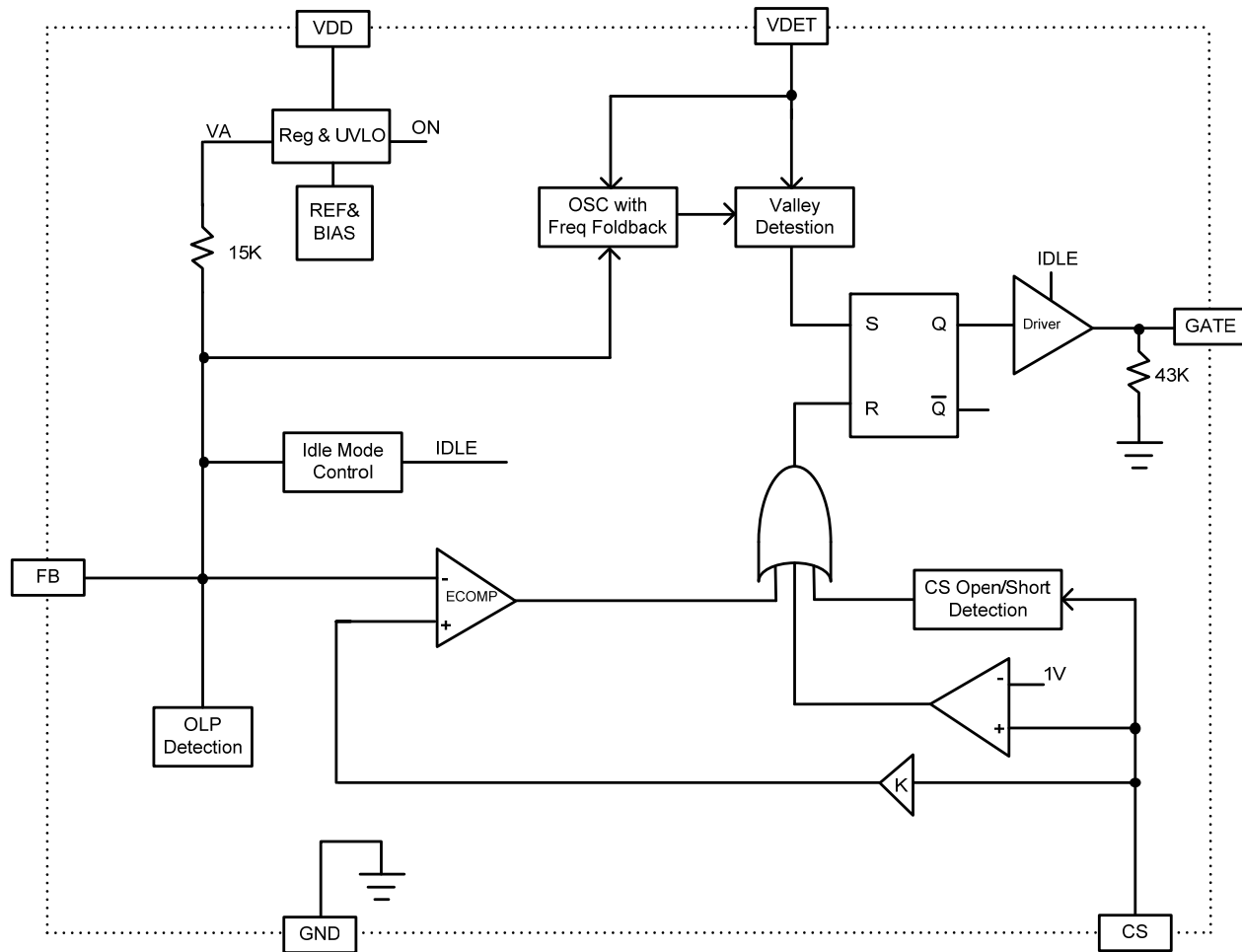
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0V	11.5	12.5	13.5	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	6.7	7.4	8.1	V
VDD Over Voltage Protection	V_{DDOVP}	V_{DD} Rising from 0V		25		V
Start Up Supply Current	I_{DDST}	$V_{DD} = 10V$, before VDD Turn-on		8	13	μA
IDD Supply Current	I_{DD}	$V_{DD} = 15V$, after VDD Turn-on ,FB floating		0.6		mA
IDD Supply Current at Standby	I_{DDSTBY}	FB = 1.3V		0.4		mA
IDD Supply Current at Fault	$I_{DDFAULT}$	Fault mode, FB Floating		250		μA
Feedback						
FB Pull up Resistor	R_{FB}			15		k Ω
CS to FB Gain	A_{CS}			3		V/V
VFB at Max Peak Current				$3 + V_{BE}$		V
FB Threshold to Stop Switching	V_{FBBM1}			1.35		V
FB Threshold to Start Switching	V_{FBBM2}			1.51		V
Output Overload Threshold				4.2		V
OverLoad/Over Voltage Blanking Time	$T_{OVBLANK}$			320		ms

ELECTRICAL CHARACTERISTICS CONT'D

($V_{DD} = 14V$, $L_M = 4mH$, $R_{CS} = 1.27\Omega$, $V_{OUT} = 12V$, $N_P = 122$, $N_S = 14$, $N_A = 15$, $T_A = 25^\circ C$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
CS Current Limit Threshold	V_{CSLIM}		0.91	0.974	1.03	V
Leading Edge Blanking Time	$T_{CSBLANK}$		300	400	500	ns
GATE DRIVE						
Gate Rise Time	T_{RISE}	$V_{DD} = 10V$, $CL = 1nF$		200	300	ns
Gate Falling Time	T_{FALL}	$V_{DD} = 10V$, $CL = 1nF$		115	200	ns
Gate Low Level ON-Resistance	R_{ONLO}	$I_{SINK} = 30mA$		7		Ω
Gate High Level ON-Resistance	R_{ONHI}	$I_{SOURCE} = 30mA$		40		Ω
Gate Leakage Current		GATE = 25V, before VDD turn-on			1	μA
Oscillator						
Maximum Switching Frequency	f_{MAX}			45		kHz
Switching Frequency Foldback	f_{MIN}	$FB = 2.3V + V_{BE}$		$f_{MAX}/3$		kHz
Maximum Duty Cycle	D_{MAX}		65	75		%
Valley Detection						
ZCD Threshold Voltage	$V_{DET_{TH}}$			100		mV
Valley Detection Time Window		After valley detection time window, if no valley detected, forcedly turn-on main switch		3.5		μs
VDET Leakage Current				1		μA
Protection						
CS Short Waiting Time				6		μs
CS Short Detection Threshold				0.112		V
CS Open Threshold Voltage				1.73		V
Abnormal OCP Blanking Time				150		ns
Thermal Shutdown Temperature				135		$^\circ C$
Line UVLO	$I_{VDETUVLO}$			0.1		mA
Line OVP	$I_{VDETOVP}$			2		mA
VDET Over Voltage Protection	$V_{DETVOOVP}$			2.72		V
VDET Vo Short Threshold	$V_{DETVOshort}$			0.58		V

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACT513 is a high performance peak current mode low-voltage PWM controller IC. The controller includes the most advance features that are required in the adaptor applications up to 60 Watt. Unique fast startup, frequency foldback, QR switching technique, accurate peak current line compensation, idle mode, short winding protection, OCP, OTP, OVP and UVLO are included in the controller.

Startup

Startup current of ACT513 is designed to be very low so that VDD could be charged to VDDON threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, two 1MΩ, 1/8 W startup resistors could be used together with a VDD capacitor(4.7uF) to provide a fast startup and yet low power dissipation design solution.

During startup period, the IC begins to operate with minimum Ippk to minimize the switching stresses for the main switch, output diode and transformers. And then, the IC operates at maximum power output to achieve fast rise time. After this, V_{OUT} reaches about 90% V_{OUT}, the IC operates with a 'soft-landing' mode(decrease Ippk) to avoid output overshoot.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT513 regulates its output voltage through secondary side control circuit . The output voltage information is sensed at FB pin through OPTO coupling. The error signal at FB pin is amplified through TL431 and OPTO circuit. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

$$V_{OUTCV} = V_{REF_TL431} \times \left(1 + \frac{R_{F1}}{R_{F2}}\right) \quad (1)$$

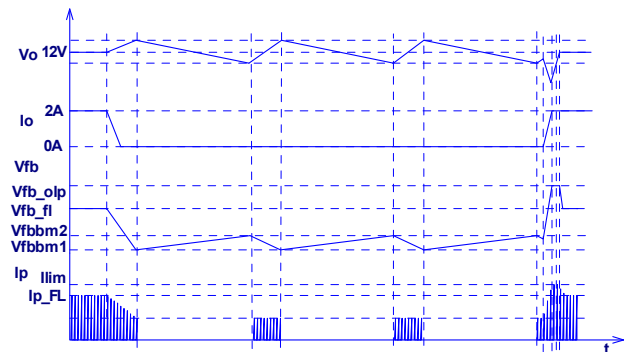
where R_{F1} (R15) and R_{F2} (R16) are top and bottom feedback resistor of the TL431.

No Load Idle Mode

In no load standby mode, the feedback voltage falls below V_{FBBM2} and reaches V_{FBBM1}, ACT513 stop

switching. After it stops, as a result of a feedback reaction, the feedback voltage increases. When the feedback voltage reaches V_{FBBM2}, ACT513 start switching again. Feedback voltage drops again and output voltage starts to bounds back and forward with very small output ripple. ACT513 leaves idle mode when load is added strong enough to pull feedback voltage exceed V_{FBBM2}.

Figure 2:
Idle Mode



Primary Inductor Current Limit Compensation vs Line

The ACT513 integrates a primary inductor peak current limit compensation circuit to achieve constant OLP over wide line.

Frequency Foldback

When the load drops to 75% of full load level, ACT513 starts to reduce the switching frequency, which is proportional to the load current ,to improve the efficiency of the converter.

ACT513's load adaptive switching frequency enables applications to meet all latest green energy standards. The actual minimum average switching frequency is programmable with output capacitance, feedback circuit and dummy load (while still meeting standby power).

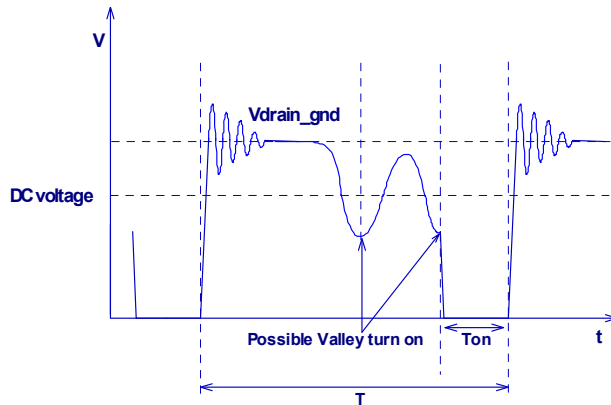
Valley Switching

ACT513 employed valley switching from no load to heavy load to reduce switching loss and EMI. In discontinuous mode operation, the resonant voltage between inductance and parasitic capacitance on MOSFET source pin is coupled by auxiliary winding and reflected on VDET pin through feedback network R5, R6. Internally, the VDET pin is connected to an zero-crossing detector to generate the switch turn on signal when the conditions are met.

FUNCTIONAL DESCRIPTION CONT'D

Figure 3:

Valley Switching



Protection Features

The ACT513 provides full protection functions. The following table summarizes all protection functions.

Auto-Restart Operation

ACT513 will enter into auto-restart mode when a fault is identified. There is a startup phase in the auto-restart mode. After this startup phase the conditions are checked whether the failure is still present. Normal operation proceeds once the failure mode is removed. Otherwise, new startup phase will be initiated again.

To reduce the power loss during fault mode, the startup delay control is implemented. The startup delay time increases over lines.

PROTECTION FUNCTIONS	FAILURE CONDITION	PROTECTION MODE
V _{DD} Over Voltage	V _{DD} > 25V (4 duty cycle)	Auto Restart
V _{DET} Over Voltage/No Voltage	V _{VD} > 2.72V or No switching for 4 cycles	Auto Restart
Over Temperature	T > 135°C	Auto Restart
Short Winding/ Short Diode	V _{CS} > 1.72V	Auto Restart
Over Load/Open Loop	IPK = I _{LIMIT} or V _{FB} = 3.5V + V _{BE} for 320ms	Auto Restart
Output Short Circuit	V _{DET} < 0.58V	Auto Restart
V _{DD} Under Volt- age	V _{DD} < 7.4V	Auto Restart

TYPICAL APPLICATION

Design Example

The design example below gives the procedure for 12V/2A flyback converter using ACT513. Refer to application circuit Figure 4, the design for an adapter application starts with the following specification:

Input Voltage Range	90VAC - 265VAC, 50/60Hz
Output Power, P _O	24W
Output Voltage, V _{OUTCV}	12V
Full Load Current, I _{OUTFL}	2A
OCP Current, I _{OUTMAX}	2.3-2.6A
System Efficiency CV, η	0.88,DOE2.0

The operation for the circuit shown in Figure 4 is as follows: the rectifier bridge D1-D4 and the capacitor C1 convert the AC line voltage to DC bus voltage. This voltage supplies the primary winding of the transformer T1 and the startup circuit of R7/R8 and C4 to VDD pin of ACT513. The primary power current path is formed by the transformer's primary winding, Q1, and the current sense resistor R9. The resistors R3, R2, diode D5 and capacitor C3 create a snubber clamping network that protects Q1 from damage due to high voltage spike during Q1's turn off. The network consisting of capacitor C4, diode D6 and resistor R4 provides a VDD supply voltage for ACT513 from the auxiliary winding of the transformer. The resistor R4 is optional, which filters out spikes and noise to makes VDD more stable. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. During power startup, the current charges C4 through startup resistor R7/R8 from the rectified bus voltage. The diode D8 and the capacitor C5/L2/C6 rectify filter the output voltage. The resistor divider consists of R15 and R16 programs the output voltage. Since a bridge rectifier and bulk input capacitors are used, the resulting minimum and maximum DC input voltages can be calculated:

$$V_{INDC_MIN} = \sqrt{2V_{INAC_MIN}^2 \frac{2P_{OUT} \left(\frac{1}{2f_L} - t_C \right)}{\eta \times C_{IN}}} \quad (2)$$

$$= \sqrt{2 \times 90^2 - \frac{2 \times 24 \times \left(\frac{1}{2 \times 47} - 3.5ms \right)}{0.88 \times 82 \mu F}} \approx 105V$$

$$V_{IN(MAX)DC} = \sqrt{2} \times V_{IN(MAX)AC} \quad (3)$$

$$= \sqrt{2} \times (265V_{AC}) = 375V$$

Where η is the estimated circuit efficiency, f_L is the

line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to be 82μF electrolytic capacitors.

To get minimum primary peak current for saving system efficiency, the maximum duty cycle is set to be 50% at low line voltage 90VAC and the circuit efficiency is estimated to be 88%. Then in CCM the primary to secondary turn ratio N_p/N_s:

$$\frac{N_p}{N_s} = \frac{D_{CCM_max} \times V_{IN_min}}{(1 - D_{CCM_max}) \times V_o} \quad (4)$$

$$= \frac{0.5 \times 105}{(1 - 0.5) \times 12} = 8.75$$

We set all CCM operation at full load in all line, the low line primary average current is:

$$I_{edc} = \frac{P_o}{\eta \times V_{in_min} \times D_{max}} \quad (5)$$

$$= \frac{12 \times 2}{105 \times 0.88 \times 0.5} = 0.52A$$

To get deeply CCM operation, set k=lppk_start/lppk=0.57 in low line, then lppk is:

$$I_{ppk} = \frac{2 \times I_{edc}}{1 + k} \quad (6)$$

$$= \frac{2 \times 0.52}{1 + 0.57} = 0.662A$$

The primary inductance is:

$$L_p = \frac{V_{indc} \times D_{uty}}{(1 - k) \times I_{ppk} \times f_{sw}} \quad (7)$$

$$= \frac{105 \times 0.5}{(1 - 0.57) \times 0.662 \times 45000} = 4mH$$

ER28 core is selected for the transformer. The core minimum Ae is 0.82cm². The minimum turn of the primary winding is:

$$N_p \geq \frac{L_p \times \Delta I_{ppk} \times 10^8}{\Delta B_{max} \times A_{e_min} (gauss \times cm^2)} \quad (8)$$

$$= \frac{0.004 \times (1 - k) \times 0.662 \times 10^8}{1200 \times 0.82} = 116T$$

VDD voltage is set to 13V, base on the data we can get primary, secondly and auxiliary turns:

$$\frac{N_A}{N_s} = \frac{V_{dd} + V_{d_aux}}{V_o + V_{d_sec}} = \frac{13 + 0.7}{12 + 0.45} = 1.1 \quad (9)$$

So base on the result, we can get the turn ratios.

$$N_p = 122T, N_s = 14T, N_a = 15T \quad (10)$$

TYPICAL APPLICATION CONT'D

Determining the value of the current sense resistor (R7) uses the maximum current in the design. So the input primary maximum current at maximum load:

$$I_{p_OCP} = \frac{2 \times L_p \times f_{sw} \times P_{in} + V_{in_min}^2 \times D_{max}^2}{2 \times L_p \times f_{sw} \times V_{in_min} \times D_{max}} \quad (11)$$

$$= \frac{2 \times 4 \times 45 \times \frac{12 \times 2 \times 2.6}{0.88} + 105^2 \times 0.5^2}{2 \times 4 \times 45 \times 105 \times 0.5} = 0.82 A$$

Since the ACT513 internal current limit is set to 0.96V, the design of the current sense resistor is given by:

$$R_{CS} = \frac{V_{CS}}{I_{p_OCP}} = \frac{0.96}{0.82} \approx 1.27 \Omega \quad (12)$$

The voltage feedback resistors are selected according to the design. Because the line UVLO is 70VDC, the upper feedback resistor is given by:

$$R_{FB_UP} = V_{INDC_UVLO} \times \frac{N_A}{N_p \times I_{FB_UVLO}} \quad (13)$$

$$= \frac{70 \times 14}{122 \times 0.15mA} \approx 54.9k\Omega$$

The lower feedback resistor is selected as:

$$R_{FB_LOW} = \frac{V_{FB}}{(V_{OUT} + V_D) \frac{N_A}{N_s} - V_{FB}} R_{FB_UP} \quad (14)$$

$$= \frac{2.2}{(12 + 0.45) \times 1.1 - 2.2} \times 54.9k\Omega \approx 11.7k\Omega$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUT}}{f_{sw} \times V_{RIPPLE}} = \frac{2}{45k \times 50mV} = 889\mu F \quad (15)$$

Three 470μF electrolytic capacitors are used to further reduce the output ripple.

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4) and feedback resistor (R5/R6) should be placed close to VDD and FB pin respectively. There are two main power path loops. One is formed by C1/C2, primary winding, mosfet transistor and current sense resistor (R9). The other is secondary winding, rectifier D8 and output capacitors (C5/C6). Keep these loop areas as small as possible. Connecting

high current ground returns, the input capacitor ground lead, and the ACT513 GND pin to a single point (star ground configuration).

Figure 4:
Universal VAC Input, 12V/2A Output Adaptor

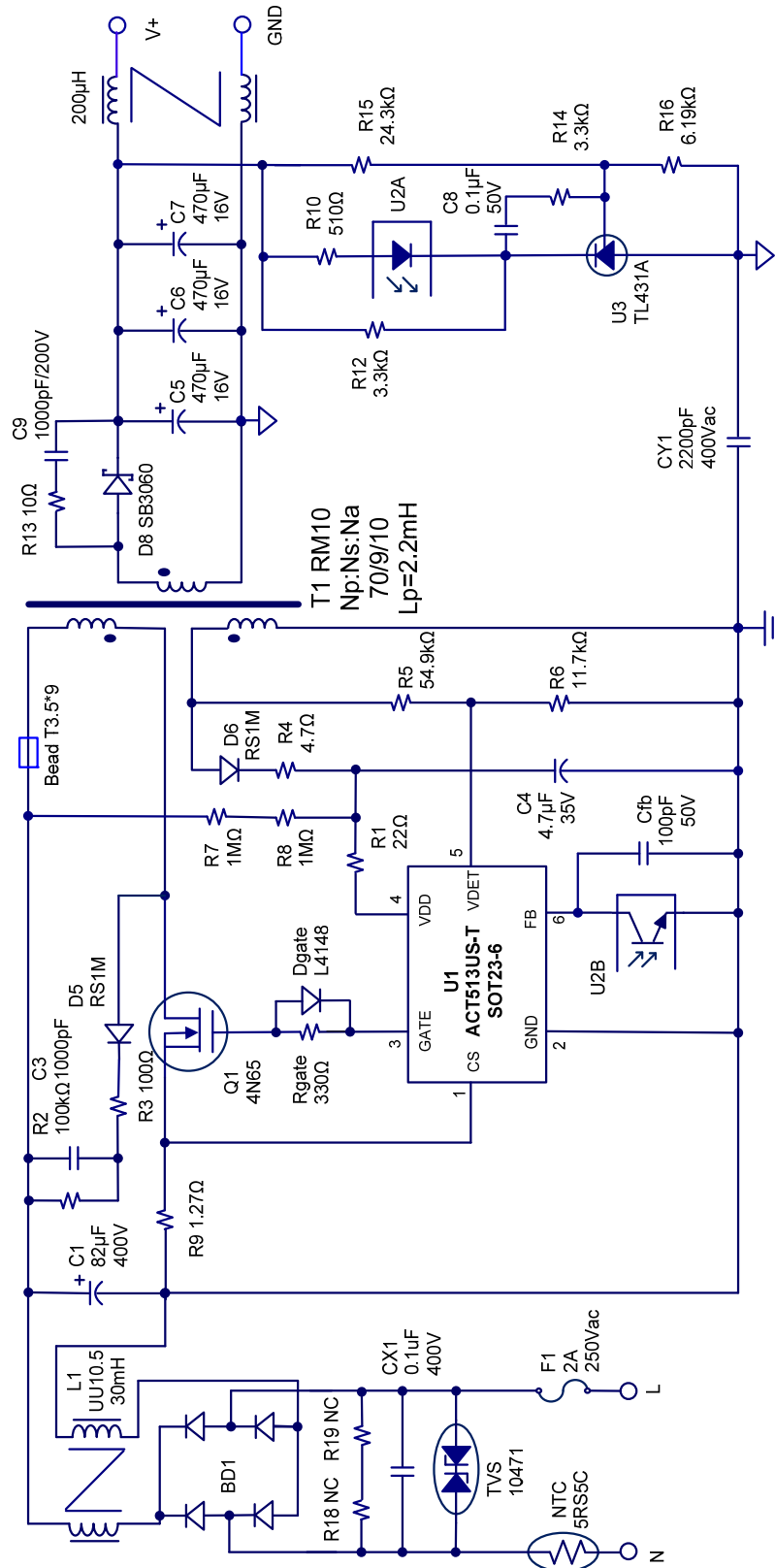
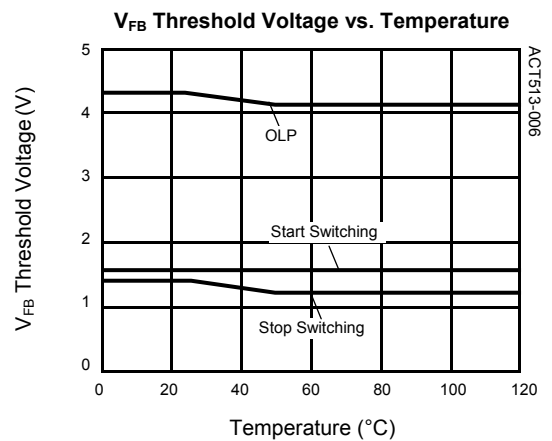
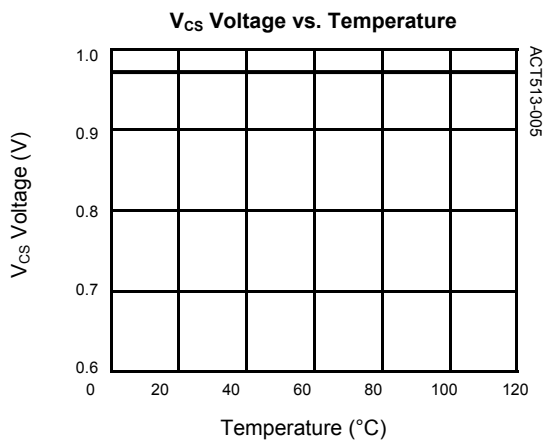
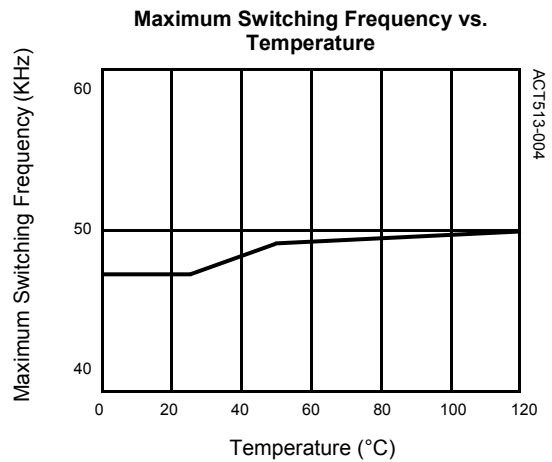
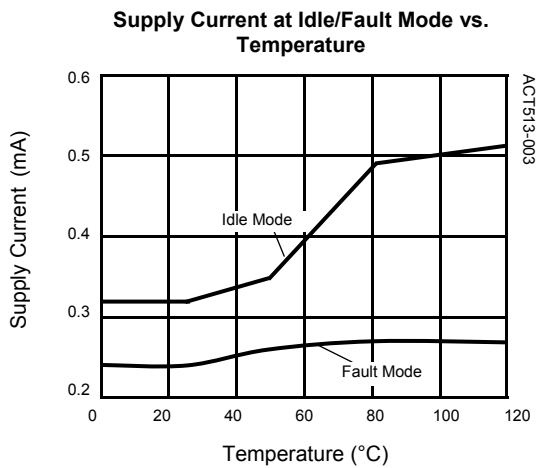
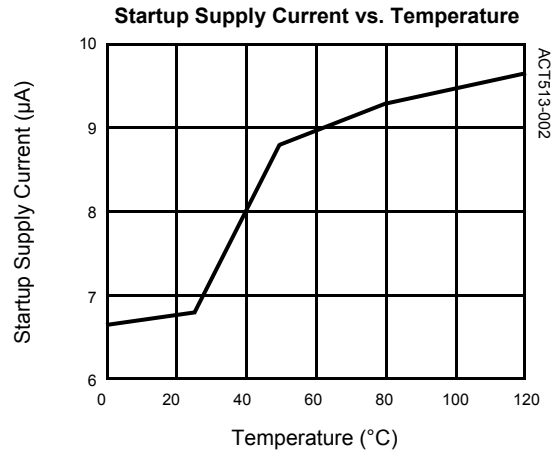
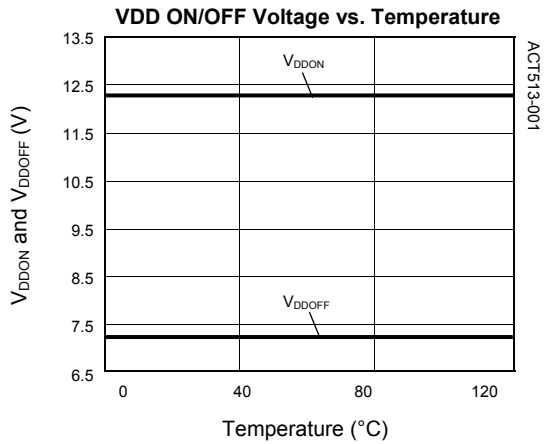


Table 1:
ACT513 12V24W Bill of Materials

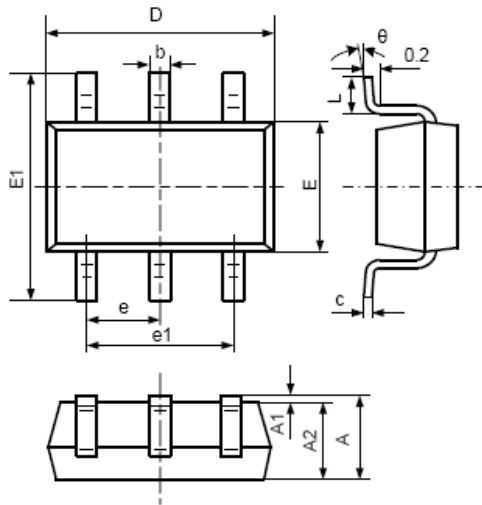
ITEM	REFERENCE	DESCRIPTION	QTY	MANUFACTURER
1	U1	IC, ACT513, SOT23-6	1	Active-Semi
2	C1	Capacitor, Electrolytic, 82µF/400V, 18 × 20mm	1	Rubcon
3	C3	Capacitor, Ceramic, 1000pF/1KV, DIP	1	POE
4	C4	Capacitor, Electrolytic, 4.7µF/35V, 5*11mm	1	KSC
5	C5,C6,C7	Capacitor, Solid, 470µF/16V, 8*16mm	3	Rubcon
6	C8	Capacitor, Ceramic, 0.1µF/50V, 0805, SMD	1	POE
7	C9	Capacitor, Ceramic, 1000pF/100V, 0805, SMD	1	POE
8	Cfb	Capacitor, Ceramic, 100pF/50V, 0805, SMD	1	POE
9	BD1	GBL10 2A/600V 4Pin DIP	1	Good-Ark
10	D5	Diode, Ultra Fast, FR107, 1000V/1.0A, DO-41	1	Good-Ark
11	D6	RS1M SMD	1	Good-Ark
12	D8	Diode, Schottky, 60V/30A, SBR3060, DO-220	1	Diodes
13	Dgate	Diode L4148 SMD	1	Good-Ark
14	LF1	CM Inductor, 50mH, UU10.5	1	SoKa
15	LF2	Axial Inductor, 0.75*5T, 5*7, Dip 200uH	1	SoKa
16	Q1	Mosfet Transistor, 04N65, TO-220F	1	Infineon
17	PCB1	PCB, L*W*T =49x68x1.6mm, Cem-1, Rev:A	1	Jintong
18	F1	Fusible, 2A/250V	1	TY-OHM
19	R1	Chip Resistor, 22 Ω, SMD 0805, 5%	1	TY-OHM
20	R2	metal Resistor, 100K Ω, DIP, 1W, 5%	1	TY-OHM
21	R3	Chip Resistor, 100Ω, 0805, 5%	1	TY-OHM
22	R4	Chip Resistor, 4.7Ω, 0805, 5%	1	TY-OHM
23	R5	Chip Resistor, 54.9kΩ, 0805, 1%	1	TY-OHM
24	R6	Chip Resistor, 11.8KΩ, 0805, 1%	1	TY-OHM
25	R7,R8	Chip Resistor, 1MΩ, 5%	2	TY-OHM
26	R9	metal Resistor, 1.27Ω, 1W, 1%	1	TY-OHM
27	R10	Chip Resistor, 510Ω, 1/4W, 5%	1	TY-OHM
28	R12,R14	Chip Resistor, 3.3KΩ, 0805, 5%	2	TY-OHM
29	R13	Chip Resistor, 10Ω, 0805, 5%	1	TY-OHM
30	R15	Chip Resistor, 24.3kΩ, 0805, 1%	1	TY-OHM
31	R16	Chip Resistor, 6.19KΩ, 0805, 1%	1	TY-OHM
32	Rgate	Chip Resistor, 330Ω, 0805, 5%	1	TY-OHM
33	T1	ER28 Lm=4mH	1	
34	CX1	X capacitance, 0.1µF/400V, X1	1	
35	NTC	Thermistor, SC053	1	TY-OHM
36	TVS	Varistor, 10471	1	TY-OHM
37	CY1	Y capacitance, 1000pF/400V, Y1	1	SEC
38	U2	Opto-coupler, PC817C CTR=200 dip-4	1	Sharp
39	U3	Voltage Regulator, TL431A, Vref=2.5V TO-92	1	ST

TYPICAL PERFORMANCE CHARACTERISTICS



PACKAGE OUTLINE


SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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