



## N-Channel 20-V (D-S) MOSFETs

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
Channel-1	20	0.0086 at V <sub>GS</sub> = 10 V	16 <sup>a</sup>	9.5 nC
		0.0108 at V <sub>GS</sub> = 4.5 V	16 <sup>a</sup>	
Channel-2	20	0.0058 at V <sub>GS</sub> = 10 V	16 <sup>a</sup>	27 nC
		0.0066 at V <sub>GS</sub> = 4.5 V	16 <sup>a</sup>	

### FEATURES

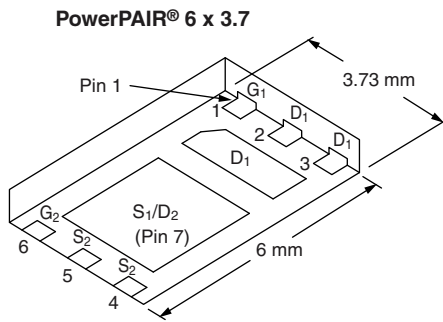
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFETs
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



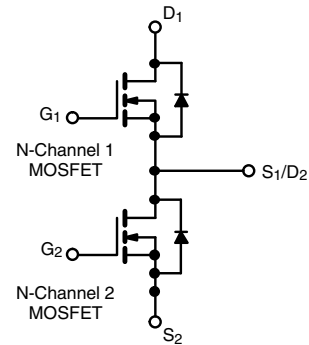
**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Notebook System Power
- POL



**Ordering Information:**  
SiZ700DT-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 16		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	16 <sup>a</sup>	16 <sup>a</sup>
		T <sub>C</sub> = 70 °C	16 <sup>a</sup>	16 <sup>a</sup>
		T <sub>A</sub> = 25 °C	13.1 <sup>b, c</sup>	17.3 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	10.5 <sup>b, c</sup>	13.9 <sup>b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	60	60	A
Source Drain Current Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	14.7	
		T <sub>A</sub> = 25 °C	1.96 <sup>b, c</sup>	2.3 <sup>b, c</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	2.36	2.8
		T <sub>C</sub> = 70 °C	1.5	1.78
		T <sub>A</sub> = 25 °C	1.4 <sup>b, c</sup>	1.47 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	0.9 <sup>b, c</sup>	0.94 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Channel-1		Channel-2		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	39	53	33	45	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	5.7	7.1	3.7	4.6	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 90 °C/W for channel-1 and 85 °C/W for channel-2.

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	20			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	20				
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		21		mV/ $^\circ\text{C}$	
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		21			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-1		- 5.8			
		$I_D = 250\text{ }\mu\text{A}$	Ch-2		- 5.8			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	0.8		2.2	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	0.8		2.2		
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	Ch-1			$\pm 100$	nA	
			Ch-2			$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	$\mu\text{A}$	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			1		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1			10		
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2			10		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	30			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	30				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		0.007	0.0086	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.0047	0.0058		
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1		0.0088	0.0108		
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	Ch-2		0.0054	0.0066		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		60		S	
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		100			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		1300		pF	
			Ch-2		3860			
Output Capacitance	$C_{oss}$		Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		290		
				Ch-2		760		
Reverse Transfer Capacitance	$C_{rss}$	Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		Ch-1		132		
				Ch-2		350		
Total Gate Charge	$Q_g$		$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$	Ch-1		20	35	nC
				Ch-2		55	85	
		Channel-1 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	Ch-1		9.5	15		
			Ch-2		27	45		
Gate-Source Charge	$Q_{gs}$	Channel-2 $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		3.2			
Gate-Drain Charge	$Q_{gd}$		Ch-2		9.2			
			Ch-1		2.4			
			Ch-2		7.1			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	Ch-1	0.3	1.3	2.6	$\Omega$	
			Ch-2	0.2	1	2		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		9	15	ns
			Ch-2		13	20	
Rise Time	$t_r$	Channel-2 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		8	15	
			Ch-2		8	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-1 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		25	40	
			Ch-2		52	80	
Fall Time	$t_f$	Channel-2 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		8	15	
			Ch-2		15	25	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		8	15	
			Ch-2		12	20	
Rise Time	$t_r$	Channel-2 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		9	15	
			Ch-2		8	15	
Turn-Off Delay Time	$t_{d(off)}$	Channel-1 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		25	40	
			Ch-2		47	75	
Fall Time	$t_f$	Channel-2 $V_{DD} = 10\text{ V}$ , $R_L = 10\ \Omega$ $I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		8	15	
			Ch-2		10	15	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			14.7	A
			Ch-2			16	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch-1			60	A
			Ch-2			60	
Body Diode Voltage	$V_{SD}$	$I_S = 2\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V
		$I_S = 2.3\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-2		0.8	1.2	
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		25	50	ns
			Ch-2		40	80	
Body Diode Reverse Recovery Charge	$Q_{rr}$	Channel-2 $I_F = 2.3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		13	25	nC
			Ch-2		31	60	
Reverse Recovery Fall Time	$t_a$	Channel-1 $I_F = 2.3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		12		ns
			Ch-2		21		
Reverse Recovery Rise Time	$t_b$	Channel-2 $I_F = 2.3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		13		
			Ch-2		19		

Notes:

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

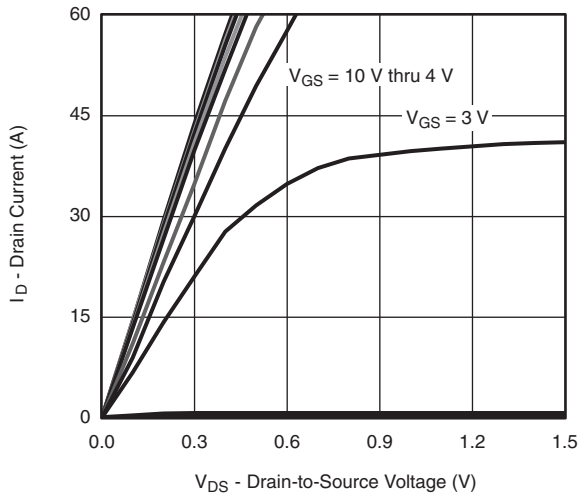
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# SiZ700DT

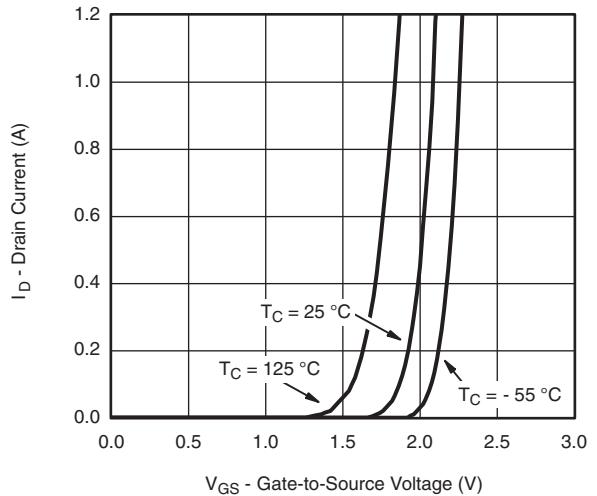
Vishay Siliconix



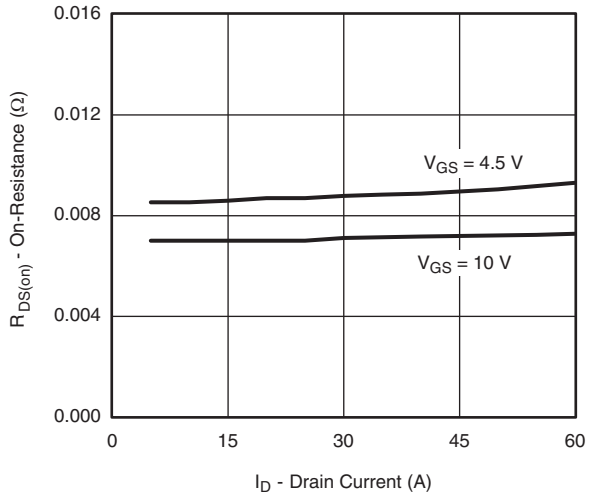
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



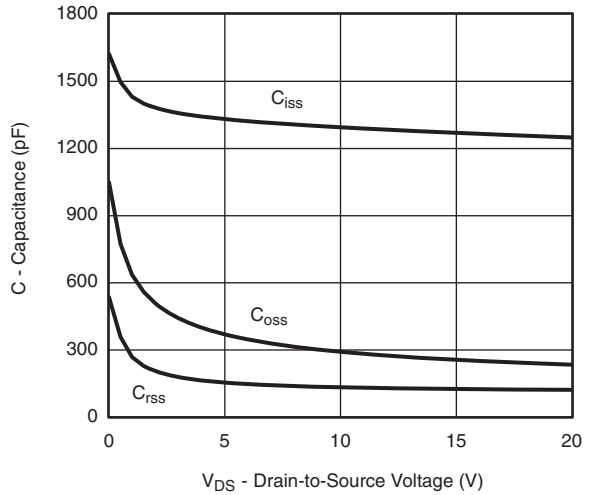
Output Characteristics



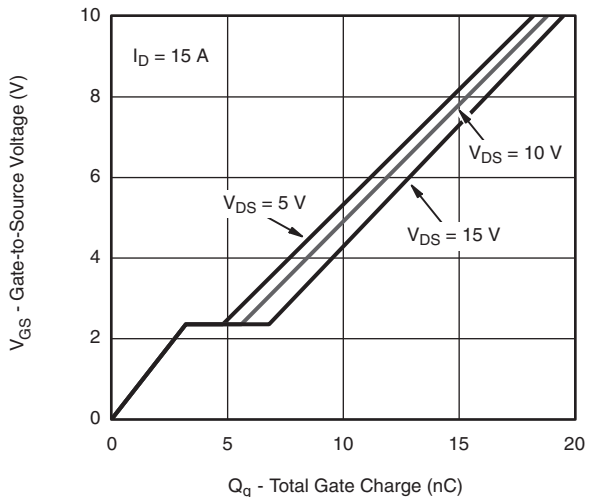
Transfer Characteristics



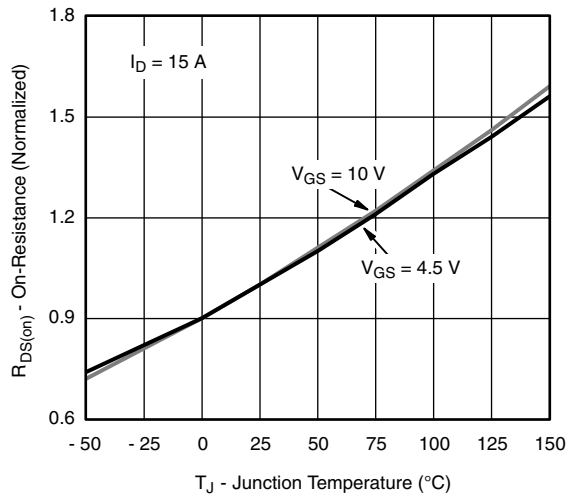
On-Resistance vs. Drain Current



Capacitance



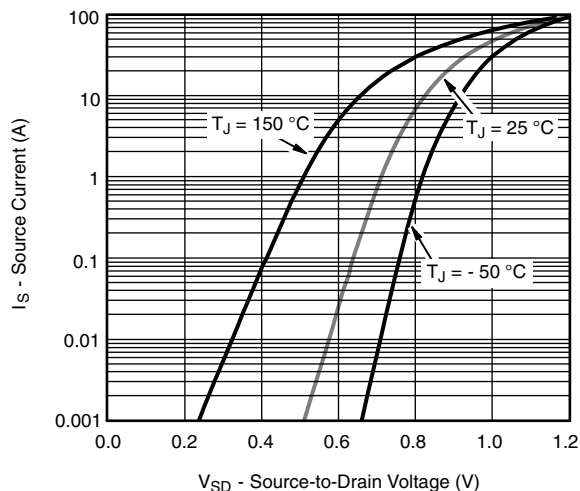
Gate Charge



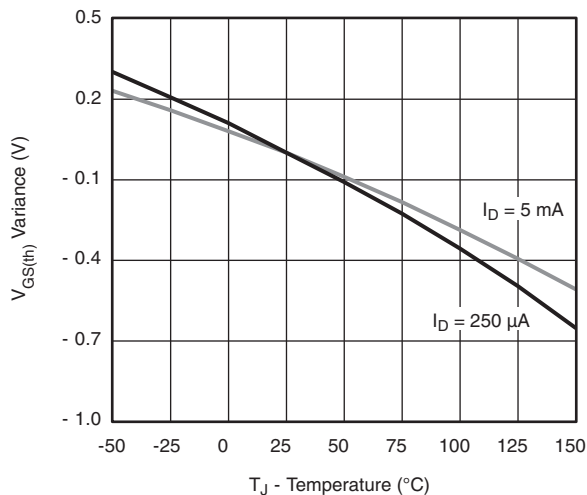
On-Resistance vs. Junction Temperature



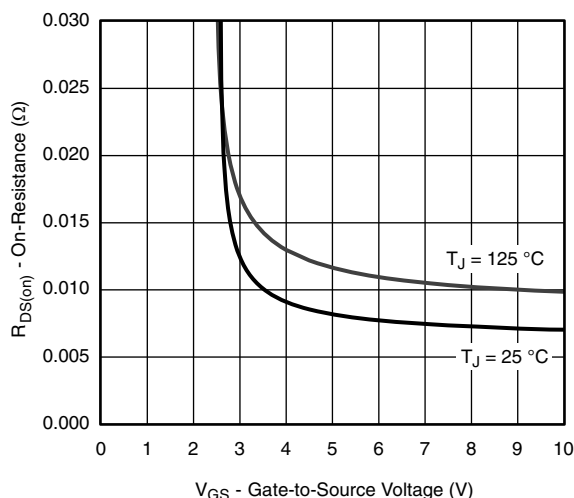
**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



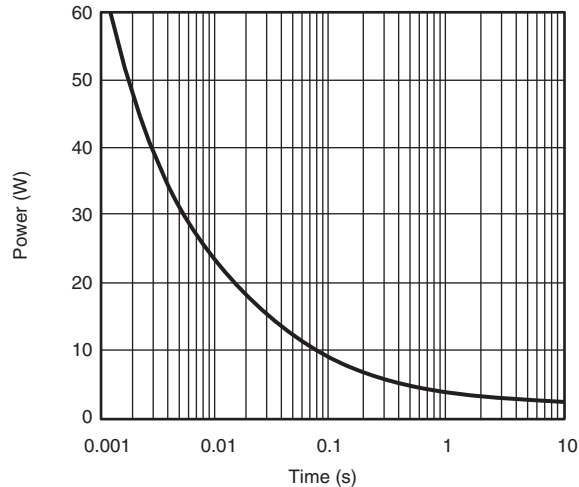
Source-Drain Diode Forward Voltage



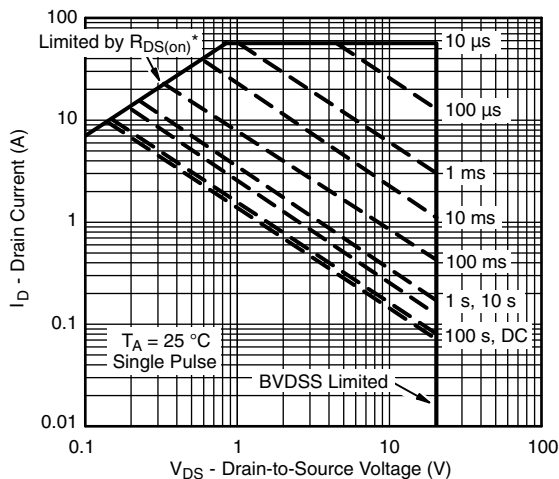
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power



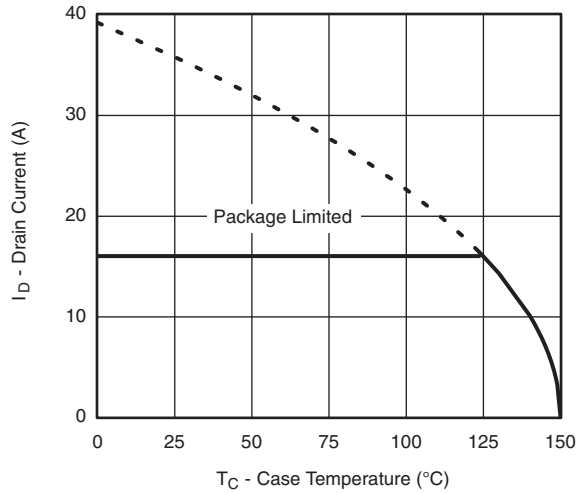
Safe Operating Area, Junction-to-Ambient

# SiZ700DT

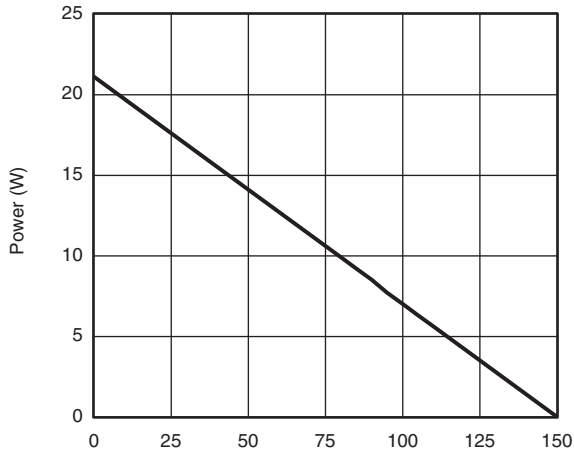
Vishay Siliconix



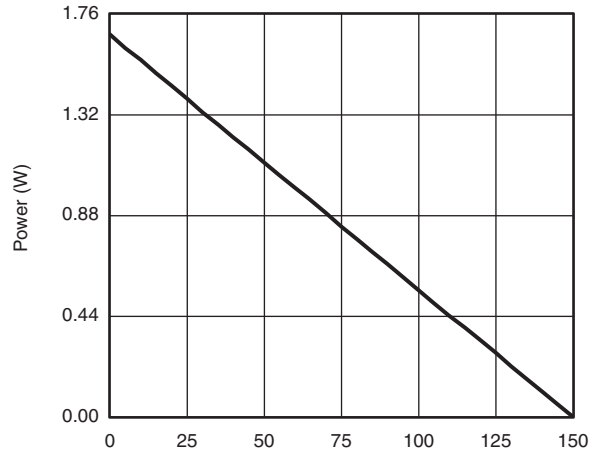
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\***



**Power, Junction-to-Case**

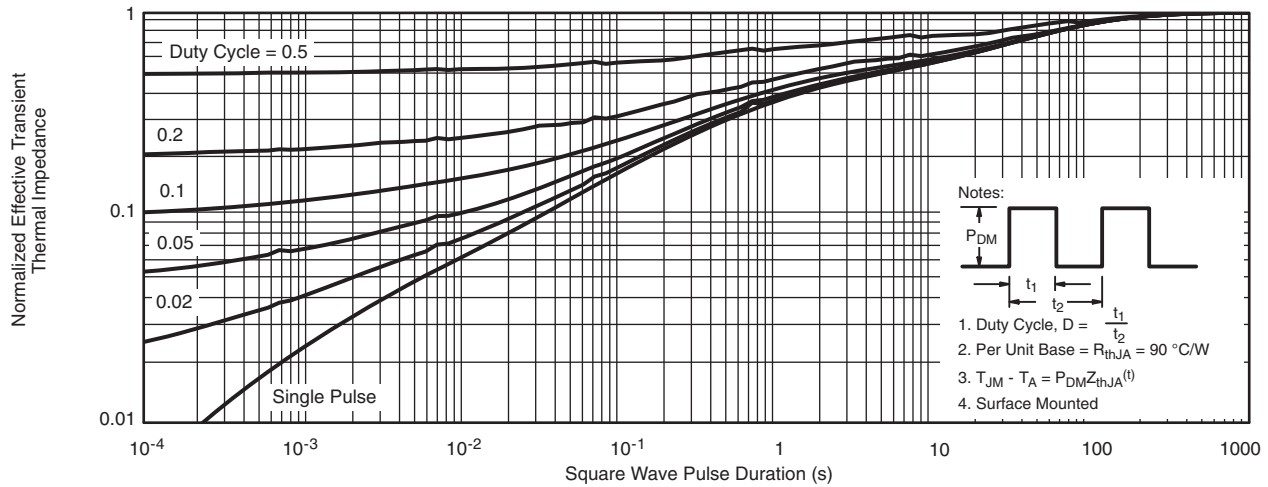


**Power, Junction-to-Ambient**

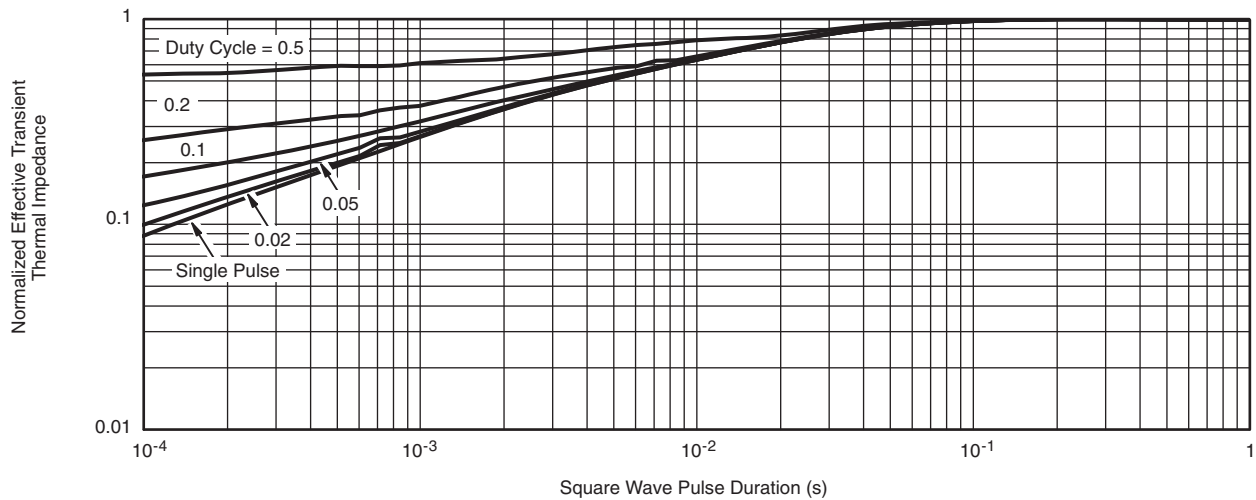
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



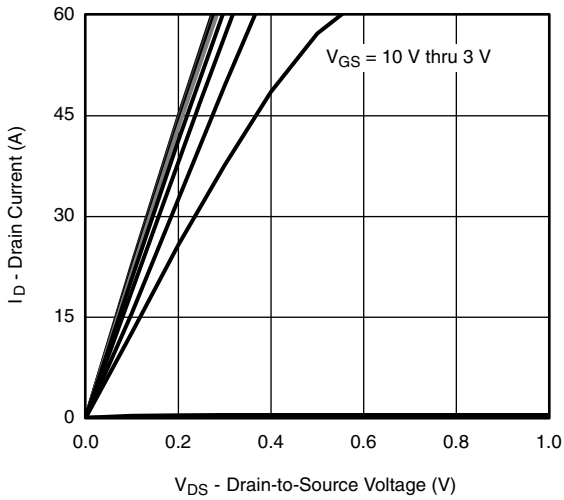
**Normalized Thermal Transient Impedance, Junction-to-Case**

# SiZ700DT

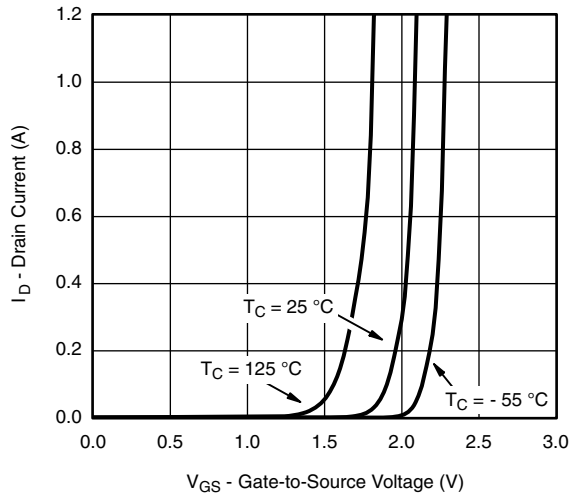
Vishay Siliconix



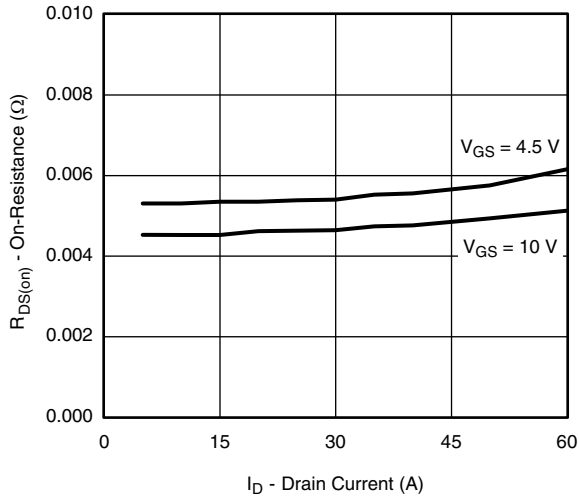
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



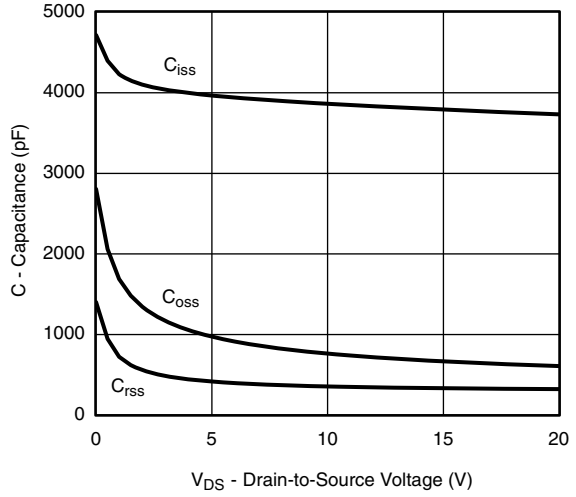
Output Characteristics



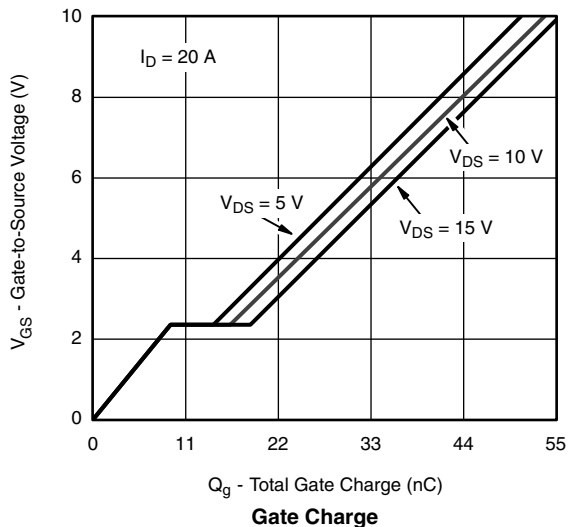
Transfer Characteristics



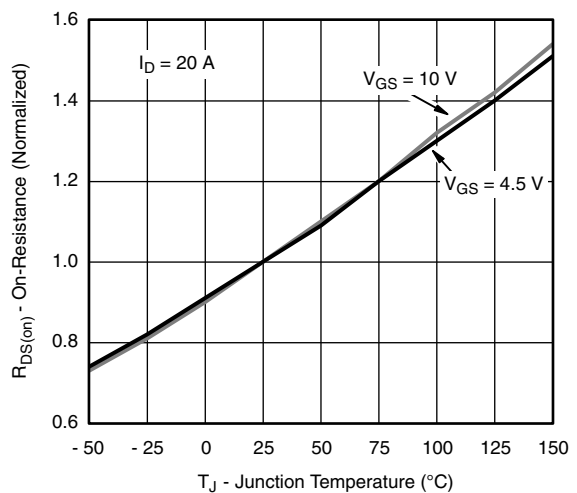
On-Resistance vs. Drain Current



Capacitance



Gate Charge

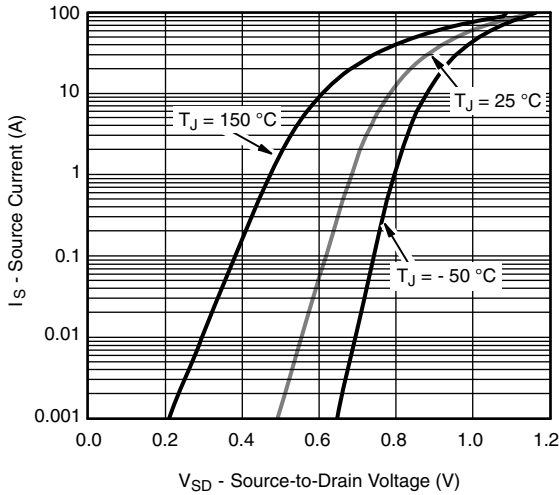


On-Resistance vs. Junction Temperature

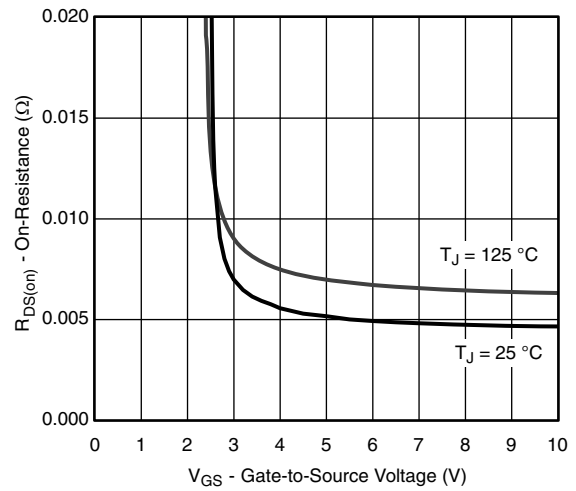




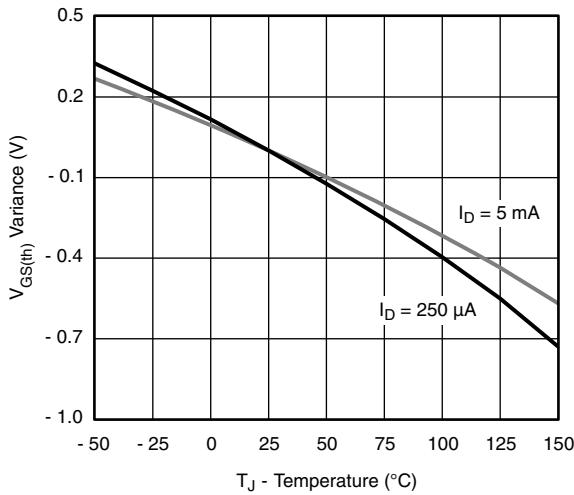
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



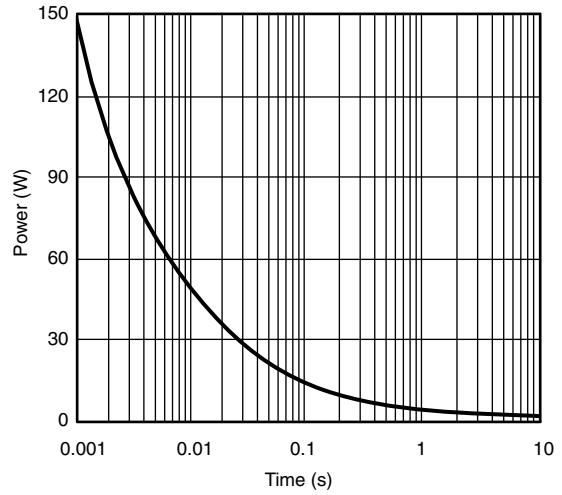
**Source-Drain Diode Forward Voltage**



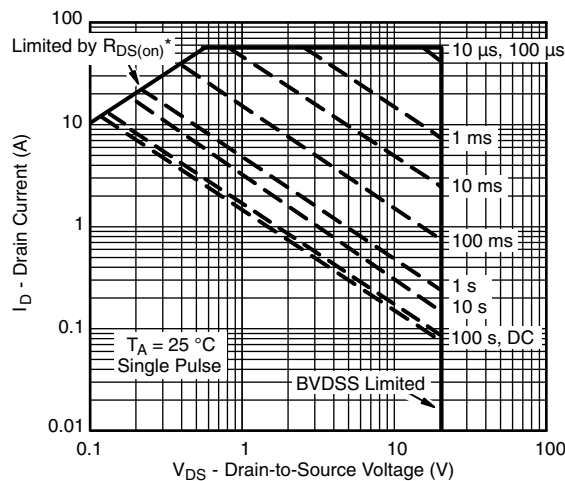
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power**



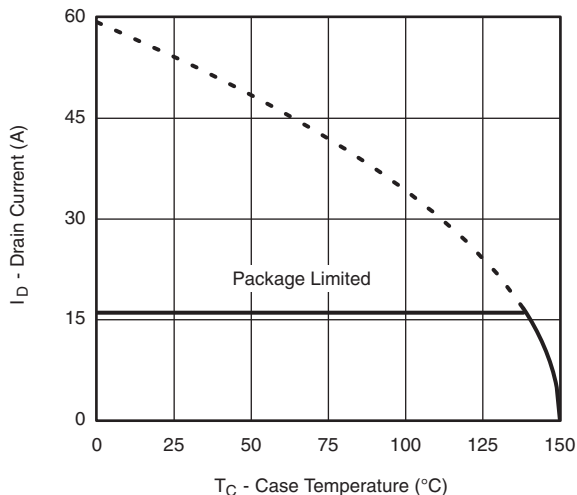
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Ambient**

# SiZ700DT

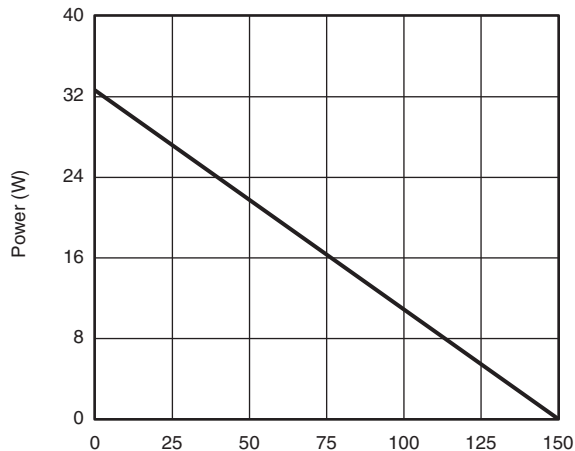
Vishay Siliconix



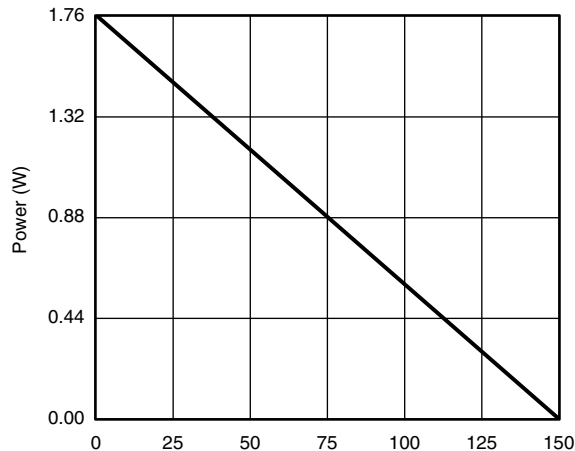
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



$T_C$  - Case Temperature (°C)  
Current Derating\*



$T_C$  - Case Temperature (°C)  
Power, Junction-to-Case

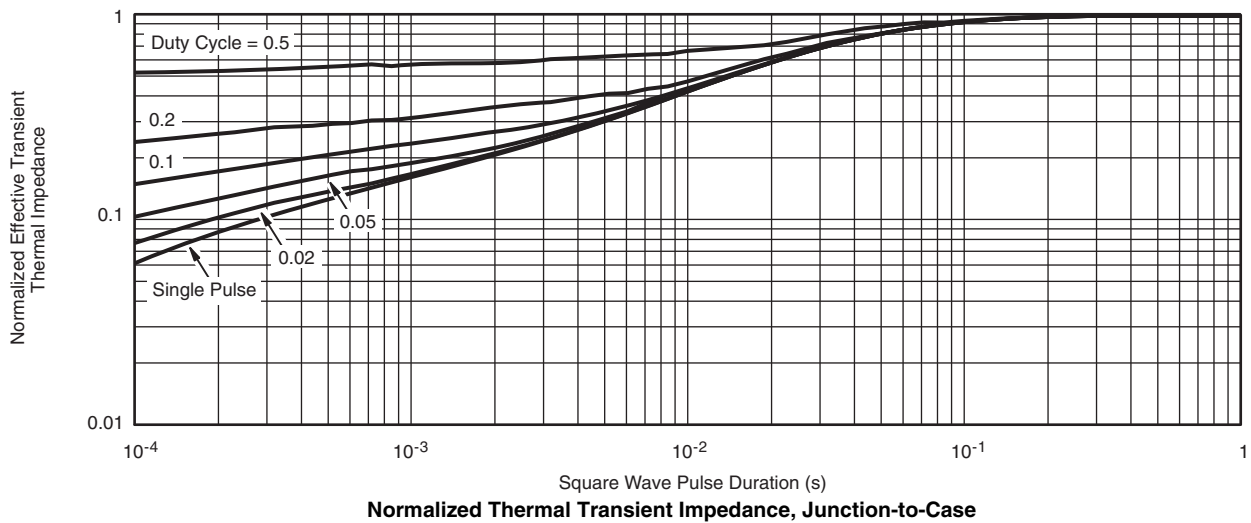
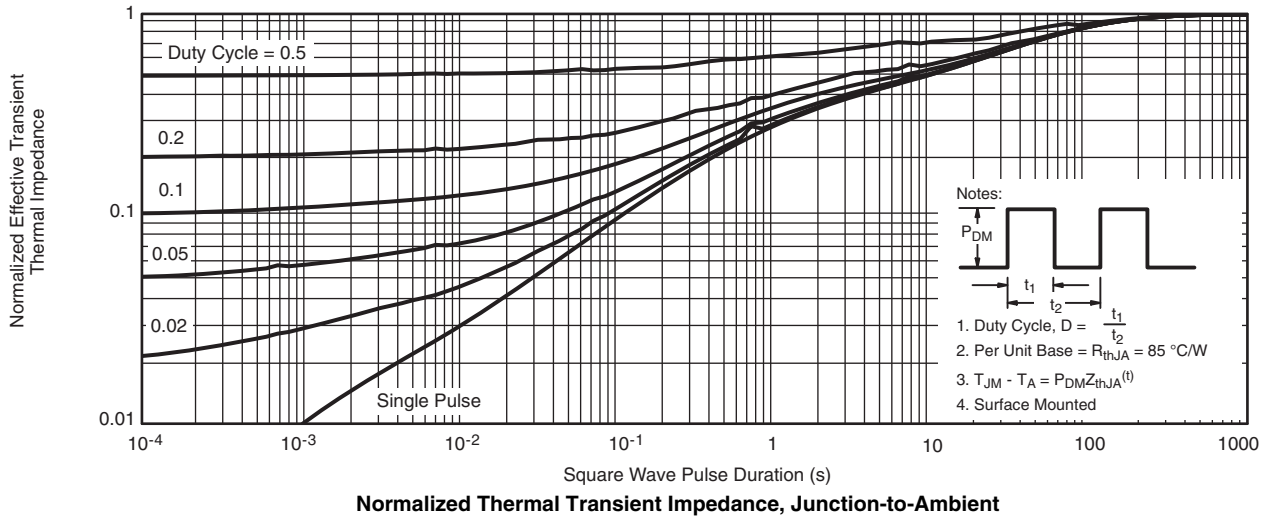


$T_A$  - Ambient Temperature (°C)  
Power, Junction-to-Ambient

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?69090](http://www.vishay.com/ppg?69090).

### PowerPAIR™ 6 x 3.7 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.05	0.000	-	0.002
b	0.46	0.51	0.56	0.018	0.020	0.022
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.65	3.73	3.81	0.144	0.147	0.150
D1	2.41	2.53	2.65	0.095	0.100	0.104
E	5.92	6.00	6.08	0.233	0.236	0.239
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.05 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
K2	0.60 TYP.			0.024 TYP.		
L	0.38	0.43	0.48	0.015	0.017	0.019
ECN: S-82772-Rev. B, 17-Nov-08 DWG: 5979						

**RECOMMENDED PAD FOR PowerPAIR™ 6 x 3.7**



Recommended PAD for PowerPAIR 6 x 3.7  
Dimensions in inches (mm)  
Keep-out 0.3520 (8.94) x 0.4390 (11.151)



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