PIC16F688

PIC16F688 Rev. A3 Silicon/Data Sheet Errata

The PIC16F688 (Rev. A3) parts you have received conform functionally to the Device Data Sheet (DS41203**D**), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the **PIC16F688 silicon**.

1. Module: EUSART – Auto-Baud Timer Overflow Does Not Generate Interrupt

If the auto-baud timer overflows during an Auto-Baud Detect operation, there will be no interrupt. The Auto-Baud Detect sequence completion will still generate an interrupt.

Work around

If using auto-baud during Sleep, ensure there is a secondary interrupt to wake-up the device if the auto-baud overflows but does not complete. Otherwise, poll the auto-baud timer overflow bit during the Auto-Baud Detect sequence to detect the overflow condition and reset the auto-baud process. Check the auto-baud timer overflow bit before using the generated baud rate.

2. Module: EUSART – False Interrupt When ABDEN Cleared

A false interrupt will be incorrectly generated if an Auto-Baud Detect operation is terminated early by clearing the Auto-Baud Enable bit, ABDEN.

Work around

If you must abort Auto-Baud Detect, clear RCIE, PEIE or GIE to block the EUSART RX interrupt before clearing ABDEN, terminating an auto-baud operation. Then read the RCREG to clear the false interrupt before enabling interrupts again.

3. Module: EUSART – WUE Bit Not Clearing

The WUE bit will not clear itself after a Break character if the RCREG is read while RXDA is low and WUE is set.

Work around

Make sure the WUE bit is cleared before reading the RCREG register. If WUE accidentally gets stuck high by reading RCREG, then clear it by software.

4. Module: EUSART – Writing to TXREG Overwrites Values (Synchronous Mode Only)

Writing to the TXREG faster than the baud rate in Synchronous mode will overwrite the previous value instead of double-buffering as in Asynchronous mode.

Work around

Load the first character into TXREG and then wait for a TX interrupt or check the TXIF bit before writing each additional character to the TXREG.

5. Module: EUSART – WUE/ABDEN Set to Wake-up Creates an Extra Interrupt

Setting WUE and auto-baud enable to wake-up on a Break character, followed by a Sync character, will generate an extra interrupt.

Work around

Do not set the Auto-Baud Detect bit before entering Sleep. After the wake-up on Break, wait for the RX pin to go high, signifying the end of a Break character. After the RX pin goes high, enable the Auto-Baud mode.

6. Module: EUSART – Auto-Baud After Break Captures Incorrect Baud Rates

When using WUE and Auto-Baud Detect simultaneously, the auto-baud will start early. This will detect incorrect baud rate.

Work around

Do not set the Auto-Baud Detect bit before entering Sleep. After the wake-up on Break, wait for the RX pin to go high, signifying the end of a Break character. After the RX pin goes high, enable the Auto-Baud mode.

7. Module: EUSART – TX Pin Tri-states When TXEN is Clear

When TXEN is clear, the TX pin will automatically be tri-stated. Note that the TXEN bit is cleared after an auto-baud overflow condition.

Work around

None.

8. Module: EUSART – TX Pin Tri-states After Auto-baud

The TX pin will briefly tri-state for approximately 8 bit times after an auto-baud completes, regardless of setting of TXEN.

Work around

None.

9. Module: EUSART – Auto-Baud Always Completes After 5 Edges on RC Pin

The EUSART auto-baud feature requires 5 edges on the RC pin to complete the auto-baud process. If the auto-baud timer overflows, the EUSART will still require a total of 5 edges before completing the auto-baud. While an auto-baud is in progress, the RCIDL bit will remain active indicating that a receive is in progress. If an overflow occurs, it will require the reception of a second character to complete the auto-baud process. When the auto-baud process completes, the BRGH register will be updated and the RCIDL bit will clear. If an auto-baud overflow occurred, the new BRGH value generated during the second received character will be invalid.

Work around

When an auto-baud overflow occurs, the EUSART cannot be completely reset until a second character is received. Once the second character has arrived, the EUSART can be reset and normal operation can resume, regardless of SPEN.

10. Module: Resets (when WDT times out)

If the OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out. These Resets can occur even when the PSA bit is clear, assigning the prescaler to the Timer0.

Work around

If a `CLRWDT` instruction is issued before the WDT times out and before the OPTION register is modified, this problem is eliminated.

Date Codes that pertain to this issue:

All Rev. A3 silicon PIC16F688 devices.

11. Module: Data EEPROM Memory

The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write. This condition occurs when the EEPROM write timer completes at the same moment that the PIR1 register operation is executed. Register operations are those that have the PIR1 register as the destination and include, but are not limited to, BSF, BCF, ANDWF, IORWF and XORWF.

Work arounds

1. Avoid operations on the PIR1 register when writing to the EEPROM memory.
2. Poll the WR bit (EECON1<1>) to determine when the write is complete.
3. Use a timer interrupt to catch any instances when the EEIF flag is inadvertently cleared. The timer interrupt should be set longer than 8 ms. If EEIF fails, then the timer interrupt occurs as a default time out. The WR and WRERR flags are checked as part of the timer Interrupt Service Routine to verify the EEPROM write success.
4. If periodic interrupts are occurring in addition to the EEIF interrupts, then use a secondary flag to sense write completion. The secondary flag is set whenever EEPROM writes are active. An EEPROM write completion is indicated when the secondary flag is set and the WR flag is clear.

12. Module: EUSART

When BRG16 and BRGH are both set, the first edge of the received Start bit is not measured accurately. This will cause the sampling position for each bit to be up to 25% late. Multiple bytes received back-to-back will see a compounding error and some data could be lost.

Work around

Do not configure the EUSART with BRG16 and BRGH = `1`.

	BRGH = `0`	**BRGH = `1`**
BRG16 = `0`	Good	Good
BRG16 = `1`	Good	Not Recommended

13. Module: EUSART – Transmitter not Reset When Enabled

The EUSART module does not perform a Reset when TXEN is set. This allows data to be written to TXREG before the transmitter is configured.

Work around

None.

Silicon Revision History

Silicon Revision update 9/26/2006, Rev. A3 to A4:

All Silicon Revision A3 issues have been corrected in Revision A4, with the exception of Items 4 regarding auto-baud and Item 13 affecting transmission. Additional changes in Rev. A3 to Rev. A4 Silicon are as follows:

- The POR circuit has been enhanced by raising the rearm voltage to 1.2V.
- The EMI/ESD/EFT performance has been enhanced to improve the devices performance in harsh applications such as: line powered devices, furnace igniters and automotive systems.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (41203**D**), the following clarifications and corrections should be noted.

N/A.

REVISION HISTORY

Rev A Document (02/2004)
Original errata document.

Module 1: “Auto-baud timer overflow does not generate interrupt”.

Module 2: “EUSART – False Interrupt When ABDEN Cleared”. A false interrupt is generated when an EUSART auto-baud operation is terminated early by clearing ABDEN.

Module 3: “EUSART – WUE Bit Not Clearing”. UE bit is not clearing itself after a Break character, if RCREG is read while RXDA is low and WUE is set.

Module 4: “EUSART – Writing to TXREG Overwrites Values (Synchronous Mode Only)”. Writing to TXREG faster than the baud rate in Synchronous mode overwrites previous values.

Module 5: “EUSART – WUE/ABDEN Set to Wake-up Creates an Extra Interrupt”. Setting WUE and auto-baud enable to wake-up on a Break character, followed by a Sync character, will generate an extra interrupt.

Module 6: “EUSART – Auto-Baud After Break Captures Incorrect Baud Rates”. When using WUE and Auto-Baud Detect simultaneously, the auto-baud will start early. This will detect incorrect baud rate.

Rev B Document (08/2004)
Module 7: “EUSART – TX Pin Tri-states When TXEN is Clear”. When TXEN is clear, the TX pin will be tri-stated. Note that the TXEN bit is cleared after an auto-baud overflow condition.

Module 8: “EUSART – TX Pin Tri-states After Auto-baud”. The TX pin will briefly tri-state for approximately 8 bit times after an auto-baud completes.

Module 9: “EUSART – Auto-Baud Always Completes After 5 Edges on RC Pin”. The EUSART auto-baud feature requires 5 edges on the RC pin to complete the auto-baud process.

Module 10: “Resets (when WDT times out)”. When OPTION_REG bits, PS<2:0>, are clear, multiple spurious Resets can occur when the WDT times out.

Rev C Document (11/2004)

Module 11: “Data EEPROM Memory” for the PIC16F688 silicon. The EEIF flag may be cleared inadvertently when performing operations on the PIR1 register simultaneously with the completion of an EEPROM write.

Module 12: EUSART – When BRG16 and BRGH are both set, the first edge of the received Start bit is not measured accurately.

Rev D Document (7/2005)
Added Data Sheet Clarifications/Corrections Section: Added Module 1: New 4x4 QFN Package added.

Rev E Document (7/2006)
Data Sheet Clarifications/Corrections Section: Removed Items 1, which has been incorporated into the data sheet.

Rev F Document (10/2006)
Added Module 13: “EUSART – Transmitter not Reset When Enabled”.

Rev G Document (9/2008)
Updated Silicon Revision History to clarify on Items 4 and 13. Revised Modules: 2, 7-12.

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