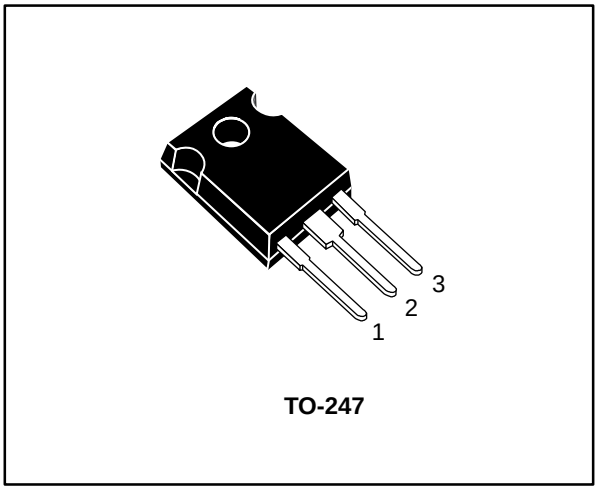
STW21N150K5

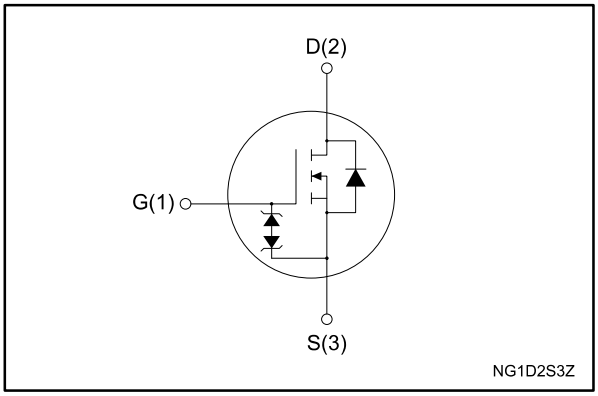
N-channel 1500 V, 0.7 Ω typ.,14 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data



TO-247

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW21N150K5	1500 V	0.9 Ω	14 A	446 W

- Industry's lowest $R_{DS(on)} * area$
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW21N150K5	21N150K5	TO-247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current at T_C = 25 °C	14	A
I_D	Drain current at T_C = 100 °C	8.7	A
I_{DM} (1)	Drain current (pulsed)	56	A
P_{TOT}	Total dissipation at T_C = 25 °C	446	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature	- 55 to 150	°C
T_{stg}	Storage temperature		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 14 A, di/dt ≤ 100 A/µs, V_{Peak} ≤ $V_{(BR)DSS}$

(3)V_{DS} ≤ 1200 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.28	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Max current during repetitive or single pulse avalanche	5	A
E_{AS} (2)	Single pulse avalanche energy	1100	mJ

Notes:

(1)Pulse width limited by T_{Jmax}

(2)Starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1500			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1500 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1500 V, Tc = 125 °C			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7 A		0.7	0.9	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	3145	-	pF
C_{oss}	Output capacitance		-	172	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 V to 1200 V, V_{GS} = 0 V	-	161	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	65	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	2.4	-	Ω
Q_g	Total gate charge	V_{DD} = 1200 V, I_D = 7 A V_{GS} = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	89	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	59	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

(2)Energy related is defined as a constant equivalent capacitance giving the same stored energy as Coss when VDS increases from 0 to 80% VDSS

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 750 V, I_D = 3.5 A, R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 17: "Unclamped inductive load test circuit"*)	-	34	-	ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	134	-	ns
t_f	Fall time		-	26	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM}	Source-drain current (pulsed)		-		28	A
V_{SD}(1)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, V_{DD} = 60 V di/dt = 100 A/µs, (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	448		ns
Q_{rr}	Reverse recovery charge		-	8.24		µC
I_{RRM}	Reverse recovery current		-	36.8		A
t_{rr}	Reverse recovery time	I_{SD} = 7 A,V_{DD} = 60 V di/dt = 100 A/µs, Tj = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	564		ns
Q_{rr}	Reverse recovery charge		-	9.48		µC
I_{RRM}	Reverse recovery current		-	33.6		A

Notes:

(1)Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-		V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

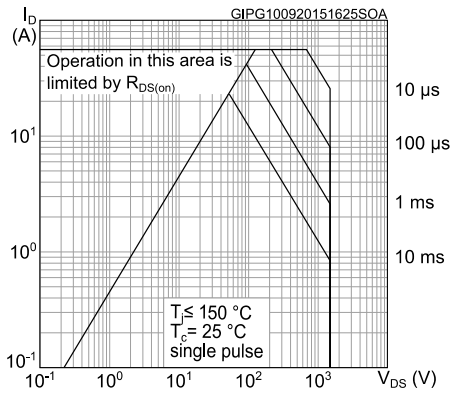


Figure 3: Thermal impedance

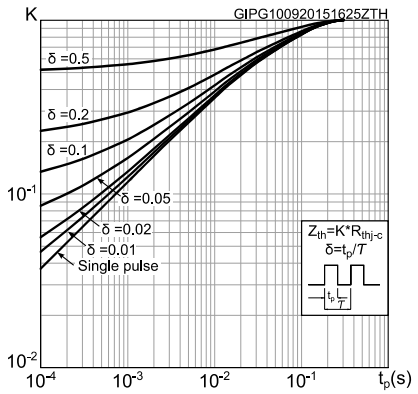


Figure 4: Output characteristics

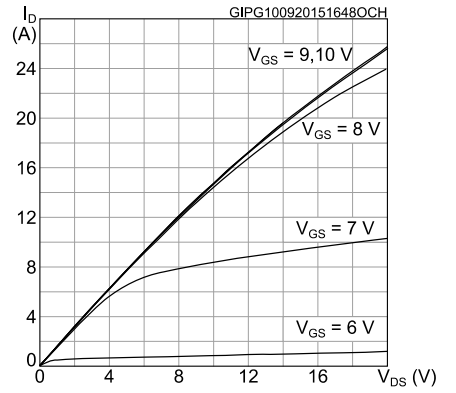


Figure 5: Transfer characteristics

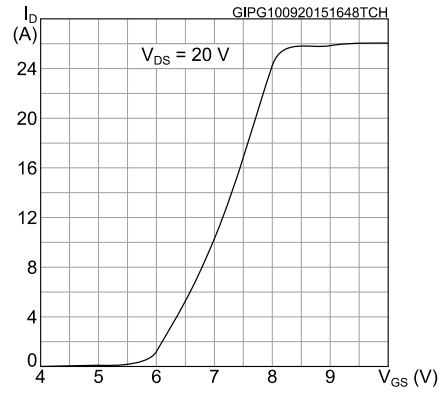


Figure 6: Gate charge vs gate-source voltage

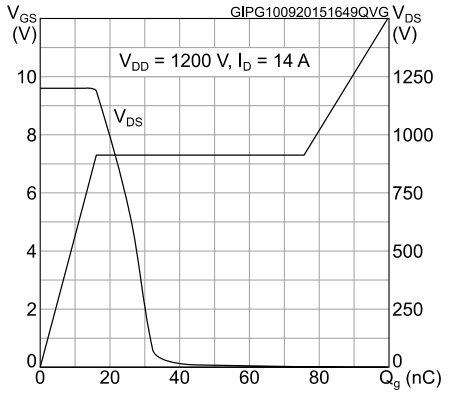


Figure 7: Static drain-source on-resistance

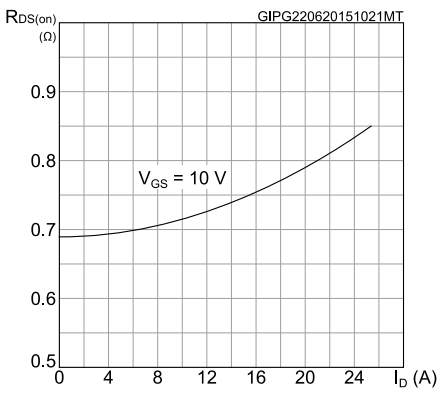


Figure 8: Capacitance variations

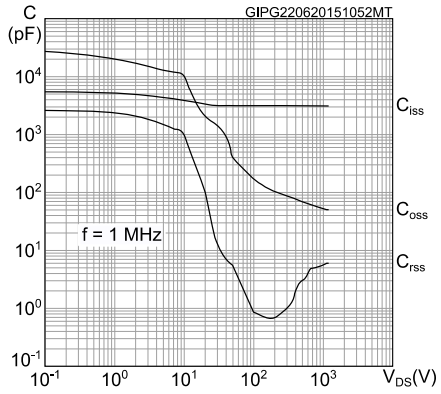


Figure 9: Normalized gate threshold voltage vs temperature

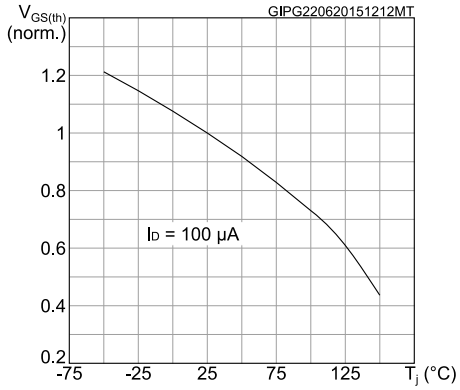


Figure 10: Normalized on-resistance vs temperature

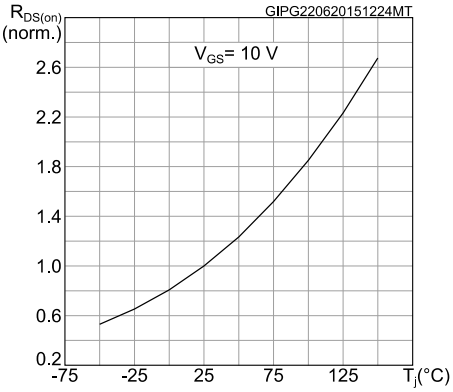


Figure 11: Normalized V(BR)DSS vs temperature

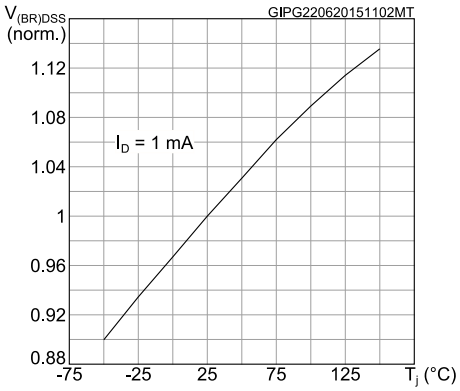


Figure 12: Maximum avalanche energy vs temperature

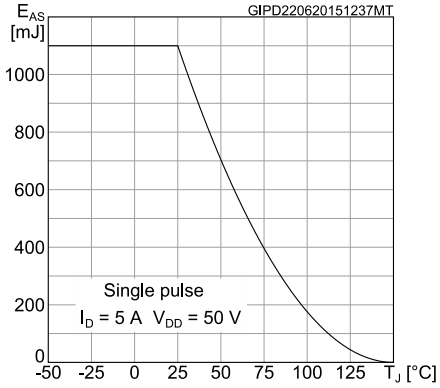
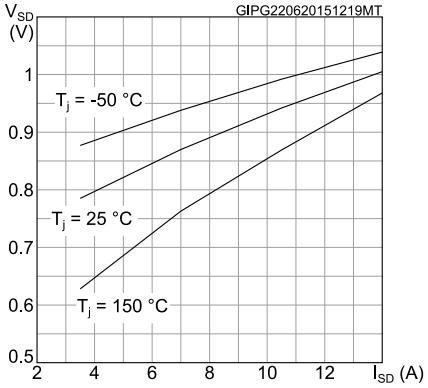


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

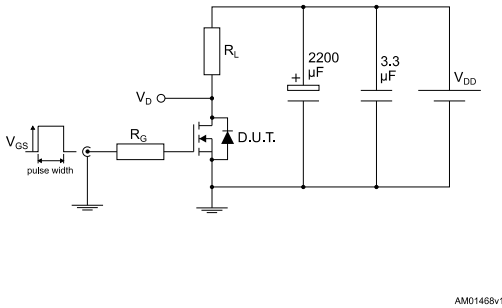


Figure 15: Test circuit for gate charge behavior

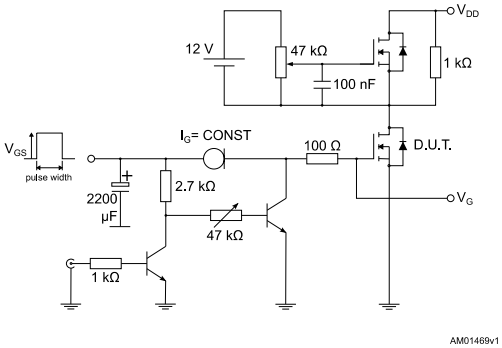


Figure 16: Test circuit for inductive load switching and diode recovery times

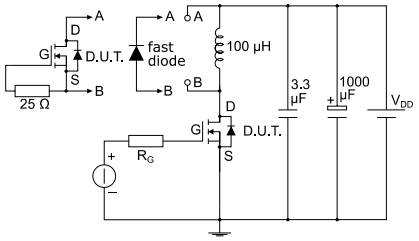


Figure 17: Unclamped inductive load test circuit

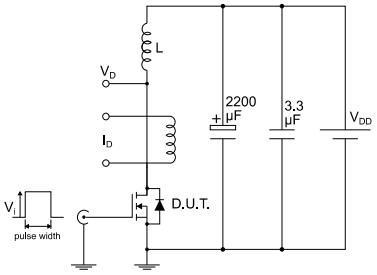


Figure 18: Unclamped inductive waveform

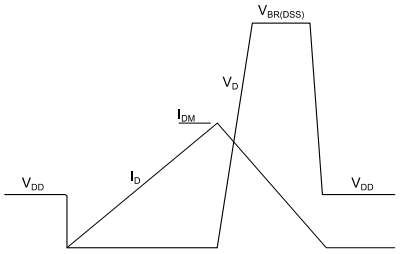
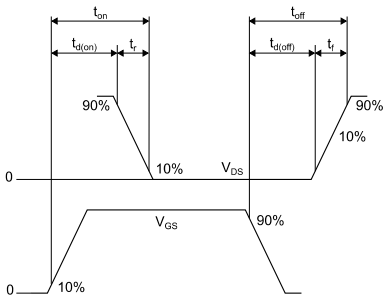


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline

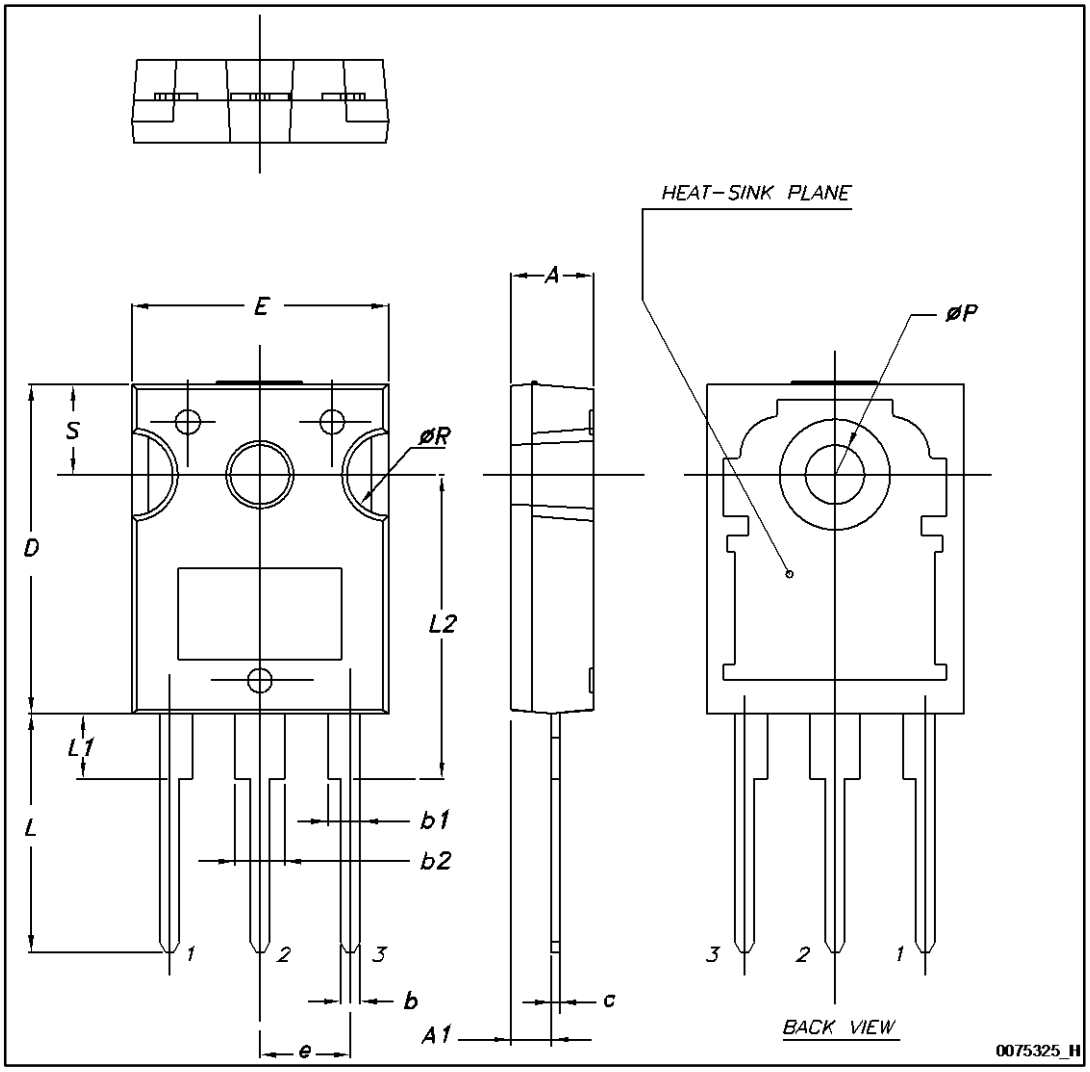


Table 10: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Aug-2015	1	First release.
10-Sep-2015	2	Text and formatting changes throughout document. Updated features on cover page. Updated sections *Electrical ratings* and *Electrical characteristics*. Added section *Electrical characteristics (curves)*. Updated section *TO-247 package information*.
01-Oct-2015	3	On cover page: - updated figure Internal schematic diagram In section Electrical characteristics: - updated and renamed table Static (was On/off states).

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