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# FAN2558/FAN2559

## 180mA Low Voltage CMOS LDO

### Features

- Fixed 1.0V, 1.2V, 1.3V, 1.5V, 1.8V, 2.5V, 3.3V, 3.5V, 3.6V, 3.8V and Adjustable Output
- Power Good Indicator with Open Drain Output
- 180mA Output Current
- 100$\mu$A Ground Current
- $C_{bypass}$ for Low Noise Operation
- Fast Enable for CDMA Applications
- High Ripple Rejection
- Current Limit
- Thermal Shutdown
- Excellent Line and Load Regulation
- Requires Only 1$\mu$F Output Capacitor
- Stable with 0 to 300mΩ ESR
- TTL-level Compatible Enable Input
- Active Output Discharge

### Applications

- Processor Power-up sequencing
- PDAs, Cell Phones
- Portable Electronic Equipment
- PCMCIA Vcc and Vpp regulation/switching

### General Description

The FAN2558/9 low voltage CMOS LDOs feature fixed or adjustable output voltage, 180mA load current, delayed power good output (open drain) and 1% output accuracy with excellent line and load regulation. An external bypass capacitor provides ultra-low noise operation.

The FAN2558/9 low voltage LDOs incorporate both thermal shutdown and short circuit protection. Output is stable with a 1$\mu$F, low ESR capacitor. The FAN2558/9 family is available in 5-Lead SOT-23, 6-Lead SOT-23 and 2x2mm MLP-6 packages.

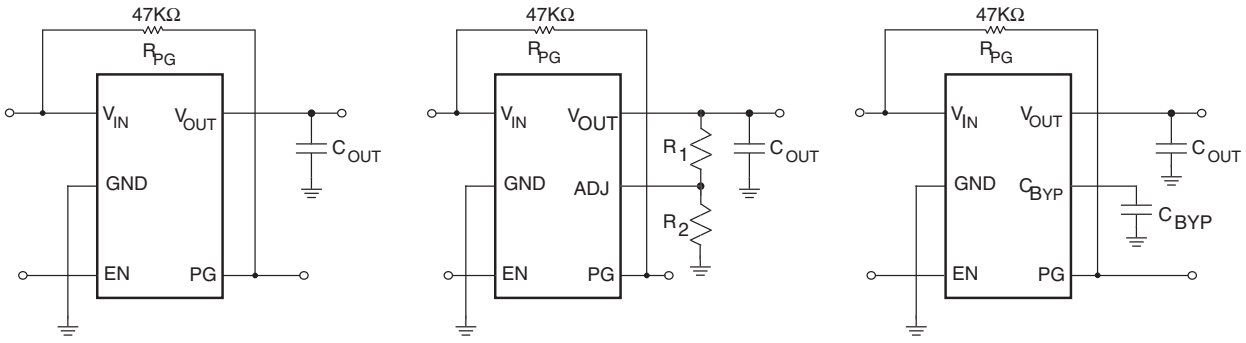
**FAN2558:** Fixed Output LDO with Power Good output

**FAN2558ADJ:** Adjustable Output LDO with Power Good output

**FAN2559:** Fixed Output LDO with Power Good output, Low Noise

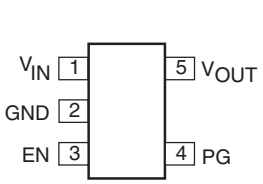
Available standard output voltages are 1.0, 1.2V, 1.3V, 1.5V, 1.8V, 2.5V, 3.3V, 3.5V, 3.6V, and 3.8V. Custom output voltage options are also available.

### Typical Application

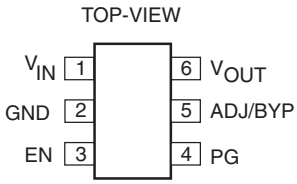



FAN2558 FAN2558ADJ FAN2559

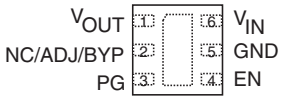
## Pin Assignments




FAN2558
5-Lead SOT-23 PACKAGE




FAN2558ADJ/FAN2559
6-Lead SOT-23 PACKAGE




FAN2558/FAN2558ADJ/FAN2559
2x2mm MLP-6 PACKAGE

| Pin no. | Pin Name | | | | | |
|---|---|---|---|---|---|---|
| | FAN2558 | | FAN2558ADJ | | FAN2559 | |
| | 5SOT-23 | 2x2mm MLP-6 | 6SOT-23 | 2x2mm MLP-6 | 6SOT-23 | 2x2mm MLP-6 |
| 1 | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ |
| 2 | GND. | NC | GND. | ADJ | GND. | BYP |
| 3 | EN | PG | EN | PG | EN | PG |
| 4 | PG | EN | PG | EN | PG | EN |
| 5 | $V_{OUT}$ | GND | ADJ | GND | BYP | GND |
| 6 | | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ | $V_{OUT}$ | $V_{IN}$ |

## Pin Descriptions

| Symbol | Pin Function Description |
|---|---|
| $V_{IN}$ | Power Supply Input |
| $V_{OUT}$ | Regulated Voltage Output |
| GND | Ground Connection |
| PG | Power Good Output, Open Drain |
| ADJ | Ratio of potential divider from $V_{out}$ to ADJ determines output voltage |
| BYP | Reference Noise Bypass |
| EN | Chip Enable Input. The regulator is fully enabled when TTL “H” is applied to this input. The regulator enters into shutdown mode when TTL “L” is applied to this input. |

## Absolute Maximum Ratings

| Parameter | | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{IN}$ to GND | | | 6 | V |
| Voltage on any other pin to GND | | -0.3 | $V_{IN}$ + 0.3 | V |
| Junction Temperature ($T_J$) | | -55 | 150 | °C |
| Storage Temperature | | -65 | 150 | °C |
| Lead Soldering Temperature, 10 seconds | | | 300 | °C |
| Power Dissipation ($P_D$) | | | Internally Limited | W |
| Electrostatic Discharge (ESD) Protection (Note1) | HBM | 4 | | kV |
| | CDM | 1 | | |

## Recommended Operating Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage Range, $V_{IN}$ for $V_{OUT}$ < 2.0V | 2.7 | | 5.5 | V |
| Supply Voltage Range, $V_{IN}$ for $V_{OUT} \geq$ 2.0V | $V_{OUT}$ + $V_{DROPOUT}$ | | 5.5 | V |
| Load Current | | | 180 | mA |
| Enable Input Voltage $V_{EN}$ | 0 | | $V_{IN}$ | V |
| Power Good Output Voltage Range $V_{PG}$ | 0 | | $V_{IN}$ | V |
| Junction Temperature | -40 | | 125 | °C |
| Thermal Resistance-Junction to Ambient SOT-23 (Note 2) | | | 235 | °C/W |
| Thermal Resistance-Junction to Case, 2mm x 2mm 6-lead MLP | | | 75 | |

**Notes:**

1. Using Mil Std. 883E, method 3015.7 (Human Body Model) and EIA/JESD22C101-A (Charge Device Model)
2. Junction to ambient thermal resistance, $\Theta_{JC}$, is a strong function of PCB material, board thickness, thickness and number of copper plains, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics.

## Electrical Characteristics

$V_{IN} = V_{IN}$ min (note 5) to 5.5V, $V_{EN} = V_{IN}$, $I_{LOAD}$ = 100µA, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage Accuracy (Note 3) | $I_{LOAD}$ = 100µA | -2 | 1 | 2 | % |
| $V_{OUT(ADJ)}$ | Output Voltage Range (Adjustable) | $I_{LOAD}$ = 100µA | 1 | | $V_{IN}$ | V |
| $\Delta V_{OUT_LNR}$ | Line Regulation | $V_{IN}$ min < $V_{IN}$ < 5.5V | -0.3 | | 0.3 | %/V |
| $\Delta V_{OUT_LDR}$ | Load Regulation (Note 4) | $I_{LOAD}$ = 0.1mA to 150mA | | 2.5 | 4 | % |
| $I_{SD}$ | Supply Current in Shutdown Mode | $V_{EN}$ < 0.4V<br>PG = No Connection | | 0.1 | | µA |
| $I_{GND}$ | Ground Pin Current (Note 4) | $I_{LOAD}$ = 0mA, $V_{IN}$ = 5.5V | | 90 | 150 | µA |
| | | $I_{LOAD}$ = 150mA, $V_{IN}$ = 5.5V | | 110 | 150 | |
| $I_{LIM}$ | Current Limit | $V_{OUT}$ = 0V | 260 | 350 | 500 | mA |
| $T_{SD}$ | Thermal Shutdown Temperature | | | 150 | | °C |
| | Thermal Shutdown Hysteresis | | | 10 | | °C |
| $V_{ENL}$ | Enable Input Low | $V_{IN}$ = 5.5V, Shutdown | | | 0.4 | V |
| $V_{ENH}$ | Enable Input High | $V_{IN}$ = 5.5V, Enabled | 1.6 | | | V |
| $I_E$ | Enable Input Current | $V_{ENL} \leq$ 0.4V, $V_{IN}$ = 5.5V | | 0.01 | | µA |
| | | $V_{ENH} \geq$ 1.6V, $V_{IN}$ = 5.5V | | 0.01 | | |
| $V_{PG}$ | Low Threshold | % of $V_{OUT}$ PG ON | 89 | | | % |
| | High Threshold | % of $V_{OUT}$ PG OFF | | | 97 | % |
| $V_{PGL}$ | PG Output Low Voltage | $I_{PG_SINK}$ = 100µA,<br>Fault Condition | | 0.02 | 0.1 | V |
| $I_{PG}$ | PG Leakage Current | PG off, $V_{PG}$ =5.5V | | 0.01 | | µA |
| $T_{EN}$ | Enable Response Time | $C_{OUT}$ = 1µF<br>$C_{BYPASS}$ = 10nF | | 30 | 300 | µS |
| $T_{ON}$ | Power "ON" Delay Time | $C_{OUT}$ = 1µF<br>$C_{BYPASS}$ = 10nF<br>$V_{ENL} \geq$ 1.6V,<br>$V_{IN}$ = 0V to $V_{OUT}$ + 1V | | 300 | 500 | µS |
| $D_{PG}$ | PG Delay time | | 1 | | 5 | mS |
| $V_{DROP-OUT}$ | Dropout Voltage (For Adjustable Output Version) | $V_{OUT}$ > 2.7V and<br>$I_{LOAD}$ = 180mA | | 400 | | mV |
| $V_{FB_ADJ}$ | Feedback Voltage (For Adjustable Output Version) | | | 0.59 | | V |

**Note:**

3. Guaranteed ±1% output voltage accuracy parts are available on customer request.
4. Measured at constant junction temperature using low duty cycle pulse testing.
5. $V_{IN}$ min = 2.7V or ($V_{OUT}$ + 1V), whichever is greater.

## DC Electrical Characteristics (Continued)

$V_{IN} = V_{IN}$ min (note 5) to 5.5V, $V_{EN} = V_{IN}$, $I_{LOAD}$ = 100µA, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| PSRR | Power Supply Rejection Ratio | DC to 100kHz<br>$C_{OUT}$ =1µF<br>$C_{BYPASS}$= 10nF<br>$I_{LOAD}$ = 0 to 150mA<br>$V_{OUT} \leq$ 1.8V | | 50 | | dB |
| $e_N$ | Output Noise | BW: 300Hz to 50kHz<br>$C_{OUT}$ =1µF<br>$C_{BYPASS}$= 10nF<br>$I_{LOAD}$ = 0 to 150mA | | 30 | | $\mu V_{RMS}$ |

# Functional Description

Utilizing BiCMOS technology, the FAN2525/FAN2559 product family is optimized for use in compact battery powered systems. These LDOs offer a unique combination of high ripple rejection, low noise, low power consumption, high tolerance for a variety of output capacitors, and less than 1$\mu$A "OFF" current. In the circuit, a differential current sense amplifier controls a series-pass P-Channel MOSFET to achieve high ripple rejection. A separate error amplifier compares the load voltage at the output with an onboard trimmed low voltage bandgap reference for output regulation.

Thermal shutdown and current limit circuits protect the device under extreme conditions. When the device temperature reaches 150°C, the output is disabled. When the device cools down by 10°C, it is re-enabled. The user can shut down the device using the Enable control pin at any time. The current limit circuit is trimmed, which leads to consistent power on /enable delays, and provides safe short circuit current densities even in narrow traces of the PCB.

A carefully optimized control loop accommodates a wide range of ESR values in the output bypass capacitor, allowing the user to optimize space, cost, and performance requirements.

An Enable pin shuts down the regulator output to conserve power, reducing supply current to less than 1$\mu$A.

The fixed-voltage FAN2559 has a noise bypass pin. Power Good is available as a diagnostic function to indicate that the output voltage has reduced within 5% of the nominal value.

The six pin adjustable-voltage version utilizes pin 5 to connect to an external voltage divider which feeds back to the regulator error amplifier, thus setting the output voltage to the desired value.

# Applications Information

### External Capacitors – Selection

The FAN2558/FAN2559 gives the user the flexibility to utilize a wide variety of capacitors compared to other LDOs. An innovative design approach offers significantly reduced sensitivity to ESR, which degrades regulator loop stability in older designs. While the improvements featured in the FAN2558/FAN2559 family greatly simplify the design task, capacitor quality still must be considered if the designer is to achieve optimal circuit performance. In general, ceramic capacitors offer superior ESR performance, and a smaller case size than tantalum capacitors.

### Input Capacitor

An input capacitor of 2.2$\mu$F (nominal value) or greater, connected between the Input pin and Ground, placed in close proximity to the device, will improve transient response and ripple rejection. Higher values will further improve ripple rejection and transient response. An input capacitor is recommended when the input source, either a battery or a regulated AC voltage, is located far from the device. Any good quality ceramic, tantalum, or metal film capacitor will give acceptable performance; however, in extreme cases capacitor surge current ratings may have to be considered.

### Output Capacitor

An output capacitor is required to maintain regulator loop stability. Stable operation will be achieved with a wide variety of capacitors with ESR values ranging from 0mΩ up to 400mΩ. Multilayer ceramic, tantalum or aluminum electrolytic capacitors may be used. A nominal value of at least 1$\mu$F is recommended. Note that the choice of output capacitor affects load transient response, ripple rejection, and it has a slight effect on noise performance as well.

An internal resistor of approximately 100Ω is connected between $V_{OUT}$ and GND in shutdown mode, to discharge the output capacitor at a faster rate.

### Bypass Capacitor (FAN2559 Only)

In the fixed-voltage configuration, connecting a capacitor between the bypass pin and ground can significantly reduce output noise. Values ranging from 0pF to 47nF can be used, depending on the sensitivity to output noise in the application.

At the high-impedance Bypass pin, care must be taken in the PCB layout to minimize noise pickup, and capacitors must be selected to minimize current loading (leakage). Noise pickup from external sources can be considerable. Leakage currents into the Bypass pin will directly affect regulator accuracy and should be kept as low as possible; thus, high-quality ceramic and film types are recommended for their low leakage characteristics. Cost-sensitive applications not concerned with noise can omit this capacitor.

## Control Functions

### Enable Pin

Connecting 2V or greater to the Enable pin will enable the output, while 0.4V or less will disable it while reducing the quiescent current consumption to less than 1$\mu$A. If this shutdown function is not needed, the pin can simply be connected permanently to the $V_{IN}$ pin. Allowing this pin to float will cause erratic operation.

### Error Flag (Power Good)

Fault conditions such as input voltage dropout (low $V_{IN}$), overheating, or overloading (excessive output current), will set an error flag. The PG pin which is an open-drain output, will go LOW when $V_{OUT}$ is less than 95% or the specified output voltage. When the voltage at $V_{OUT}$ is greater than 95% of the specified output voltage, the PG pin is HIGH. A logic pull-up resistor of 47KΩ is recommended at this output. The pin can be left disconnected if unused.

### Thermal Protection

The FAN2558/FAN2559 is designed to supply high peak output currents for brief periods, however sustained excessive output load at high input - output voltage difference will increase the device's temperature and exceed maximum ratings due to power dissipation. During output overload conditions, when the die temperature exceeds the shutdown limit temperature of 150°C, an onboard thermal protection will disable the output until the temperature drops approximately 10°C below the limit, at which point the output is re-enabled. During a thermal shutdown, the user may assert the power-down function at the Enable pin, reducing power consumption to a minimum.

## Thermal Characteristics

The FAN2558/FAN2559 is designed to supply 180mA at the specified output voltage with an operating die (junction) temperature of up to 125°C. Once the power dissipation and thermal resistance is known, the maximum junction temperature of the device can be calculated. While the power dissipation is calculated from known electrical parameters, the actual thermal resistance depends on the thermal characteristics of the SOT23-5 surface-mount package and the surrounding PC board copper to which it is mounted.

The power dissipation is equal to the product of the input-to-output voltage differential and the output current plus the ground current multiplied by the input voltage,
or:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

The ground pin current $I_{GND}$ can be found in the charts provided in the Electrical Characteristics section.

The relationship describing the thermal behavior of the package is:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\theta_{JA}} \right\}$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die, which is 125°C, and $T_A$ is the ambient operating temperature. $\theta_{JA}$ is dependent on the surrounding PC board layout and can be empirically obtained. While the $\theta_{JC}$ (junction-to-case) of the SOT23-5 package is specified at 130°C /W, the $\theta_{JA}$ of the minimum PWB footprint will be at least 235°C /W. This can be improved by providing a heat sink of surrounding copper ground on the PWB. Depending on the size of the copper area, the resulting $\theta_{JA}$ can range from approximately 180°C /W for one square inch to nearly 130°C /W for 4 square inches. The addition of backside copper with through-holes, stiffeners, and other enhancements can also aid in reducing thermal resistance. The heat contributed by the dissipation of other devices located nearby must be included in the design considerations. Once the limiting parameters in these two relationships have been determined, the design can be modified to ensure that the device remains within specified operating conditions. If overload conditions are not considered, it is possible for the device to enter a thermal cycling loop, in which the circuit enters a shutdown condition, cools, re-enables, and then again overheats and shuts down repeatedly due to an unmanaged fault condition.

## Adjustable Version

The FAN2558ADJ includes an input pin ADJ which allows the user to select an output voltage ranging from 1V to near $V_{IN}$, using an external resistor divider. The voltage $V_{ADJ}$ presented to the ADJ pin is fed to the onboard error amplifier which adjusts the output voltage until $V_{ADJ}$ is equal to the onboard bandgap reference voltage of 1.00V(typ). The equation is:

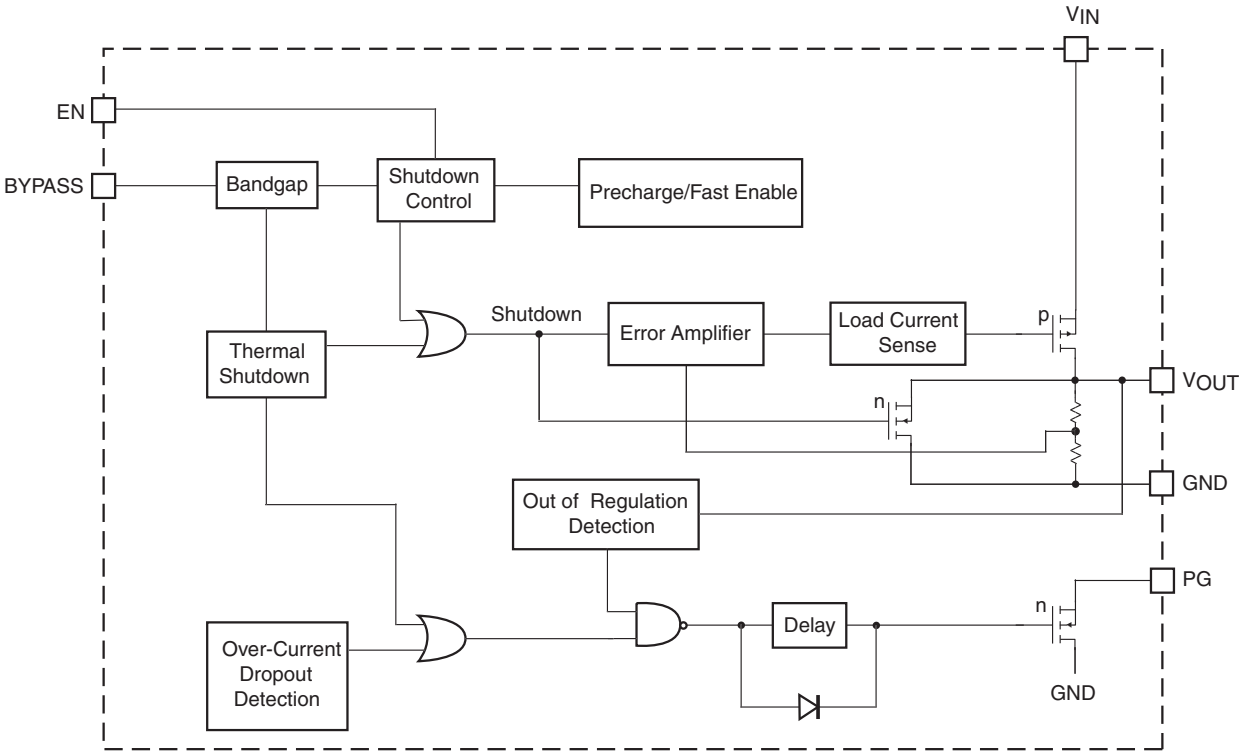
$$V_{OUT} = 0.59V \times \left[ 1 + \frac{R_1}{R_2} \right]$$

Since the bandgap reference voltage is trimmed, 1% initial accuracy can be achieved. The total value of the resistor chain should not exceed 250KOhm total to keep the error amplifier biased during no-load conditions. Programming output voltages very near $V_{IN}$ need to allow for the magnitude and variation of the dropout voltage $V_{DO}$ over load, supply, and temperature variations. Note that the low-leakage FET input to the CMOS error amplifier induces no bias current error to the calculation.

## General PCB Layout Considerations

For optimum device performance, careful circuit layout and grounding techniques must be used. Establishing a small local ground, to which the GND pin, and the output and bypass capacitors are connected, is recommended. The input capacitor should be grounded to the main ground plane. The quiet local ground is then routed back to the main ground plane using feed through via. In general, the high-frequency compensation components (input, bypass, and output capacitors) should be located as close to the device as possible. Close proximity of the output capacitor is especially important to achieve optimum performance, especially during high load conditions. A large copper area in the local ground serves as heat sink (as discussed above) when high power dissipation significantly increases device temperature. Component-side copper provides significantly better thermal performance. Added feed through connecting the device side ground plane to the back plane further reduces thermal resistance.

## Block Diagram (Note 6)



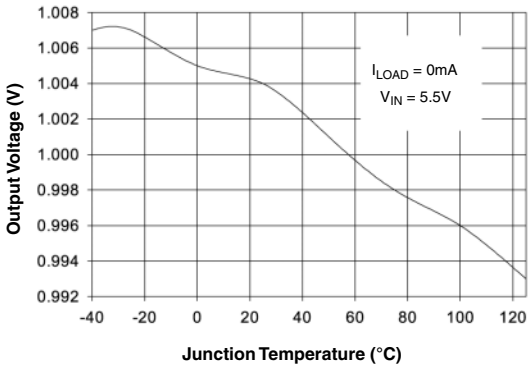

**Note:**

6. Fixed output voltage version. BYPASS pin is available for FAN2559 only.

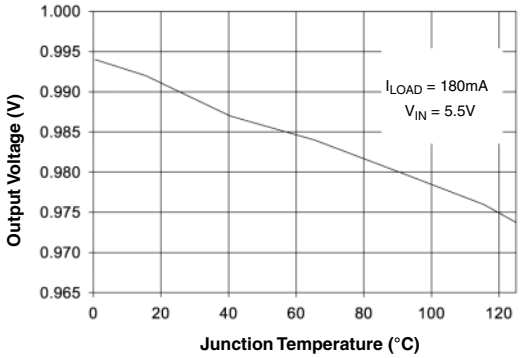
# Typical Performance Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu F$, $R_{PG} = 47k\Omega$, $T_A = 25°C$, $EN = V_{IN}$

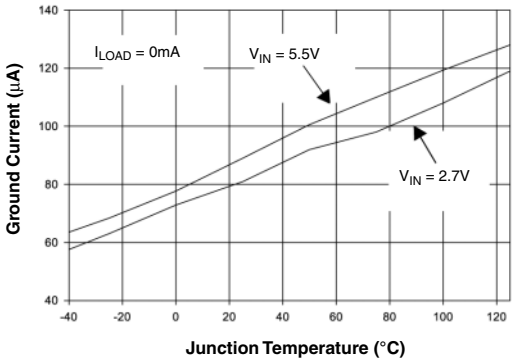
**Output Voltage vs. Temperature**



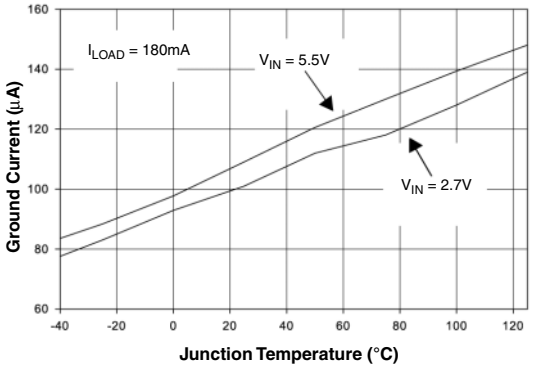

**Output Voltage vs. Temperature**



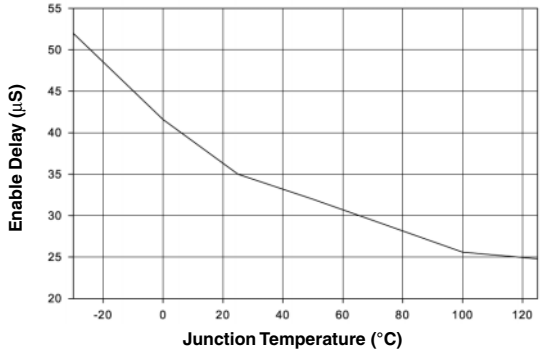

**Ground Current vs. Temperature**



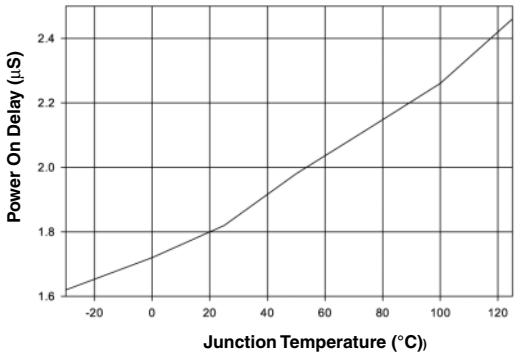

**Ground Current vs. Temperature**




**Enable Response Time vs. Temperature**



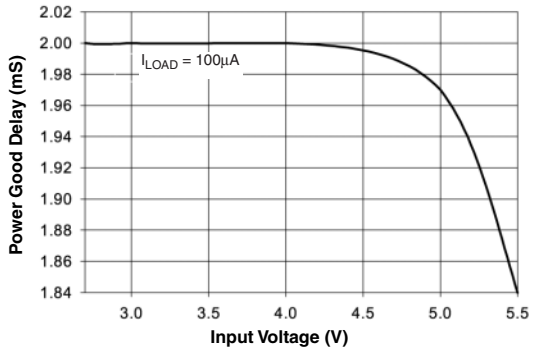

**Power On Response Time vs. Temperature**



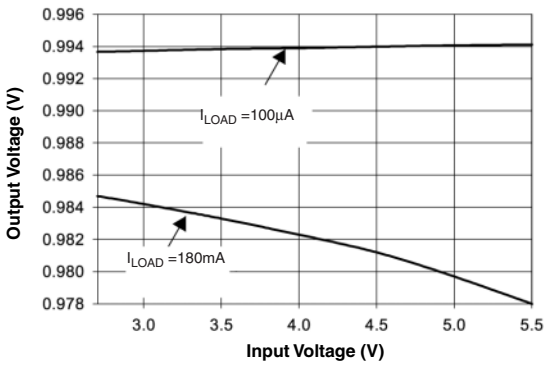
## Typical Performance Characteristics (Continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu F$, $R_{PG} = 47k\Omega$, $T_A = 25°C$, EN = $V_{IN}$

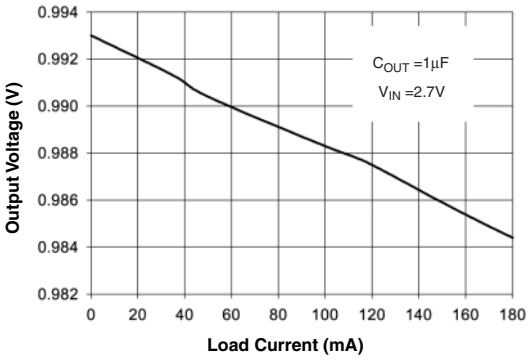
**Power Good Delay vs. Input Voltage**



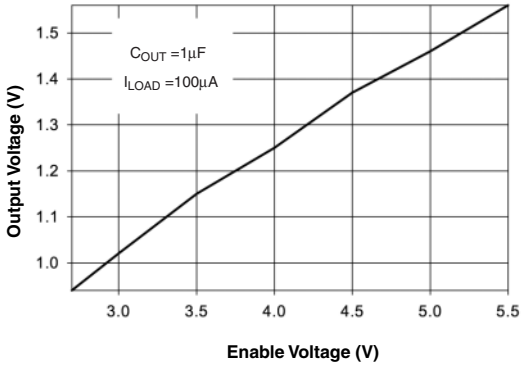

**Output Voltage vs. Input Voltage**



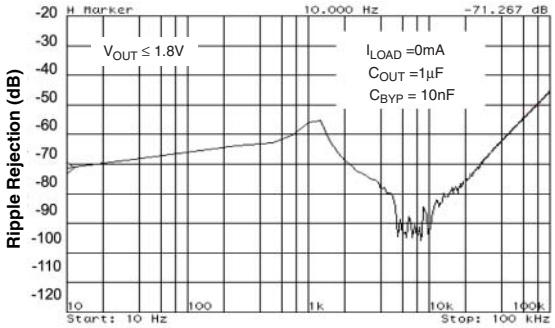

**Output Voltage vs. Load Current**



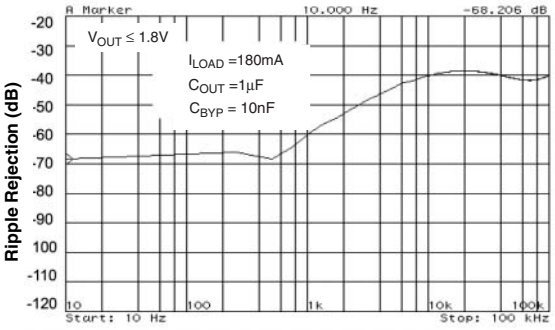

**Output Voltage vs. Enable Voltage**




**Ripple Rejection vs. Frequency**



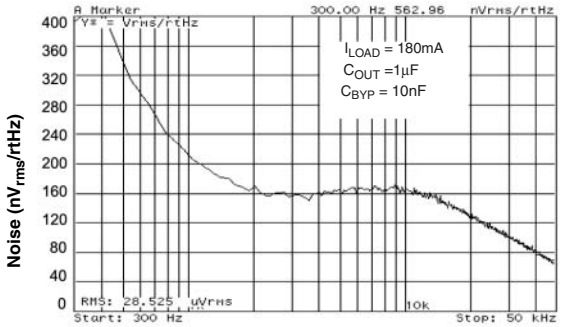

**Ripple Rejection vs. Frequency**

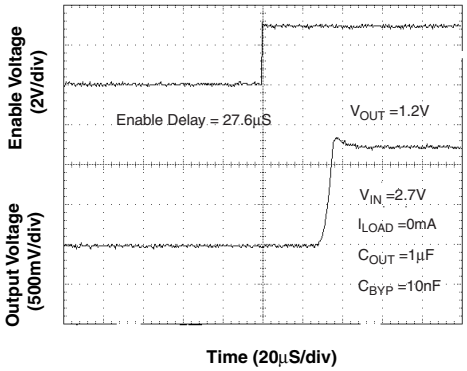


## Typical Performance Characteristics (Continued)

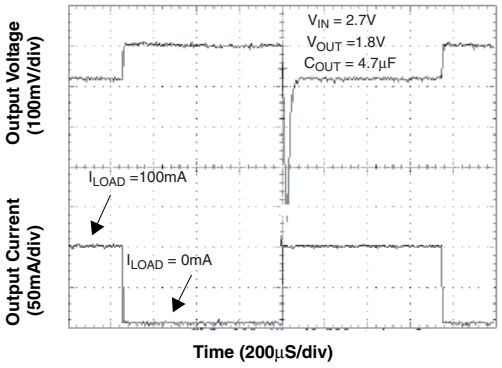
Unless otherwise specified, $C_{IN} = C_{OUT} = 1\mu F$, $R_{PG} = 47k\Omega$, $T_A = 25°C$, EN = $V_{IN}$

**Output Spectral Noise Density**

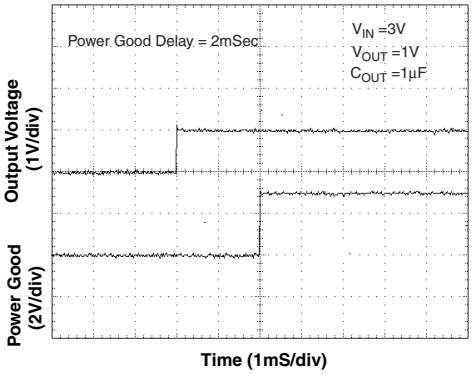


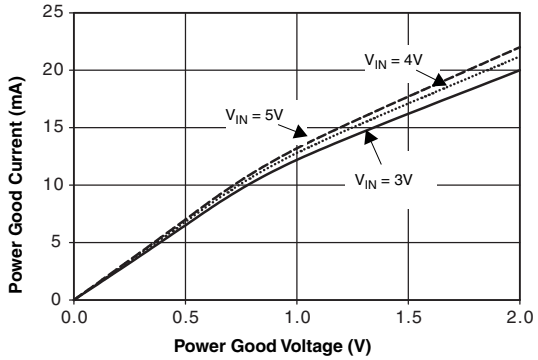

**Load Transient Response**




**Power Good Delay**

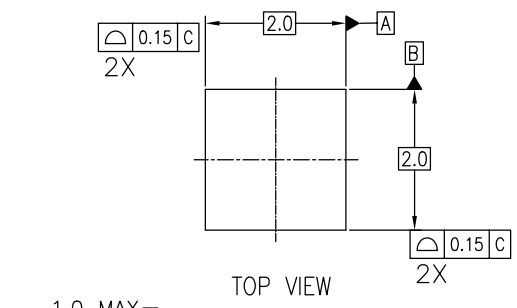


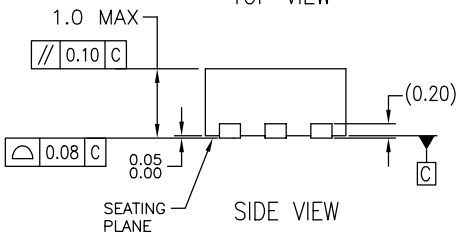

**Power Good in Fail Condition**

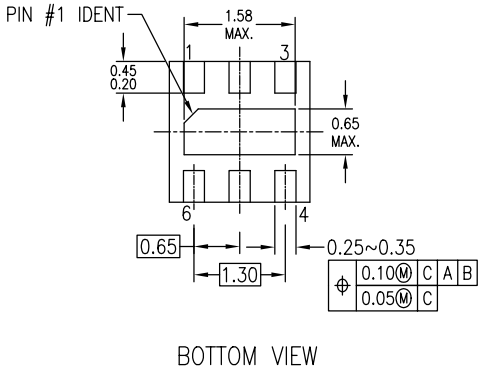


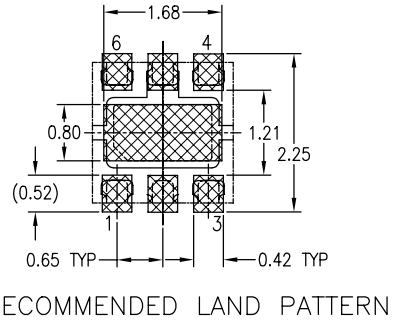
# Mechanical Dimensions

### 2x2mm 6-Lead MLP



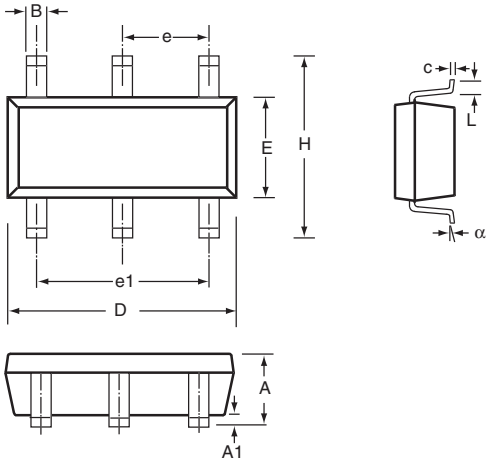



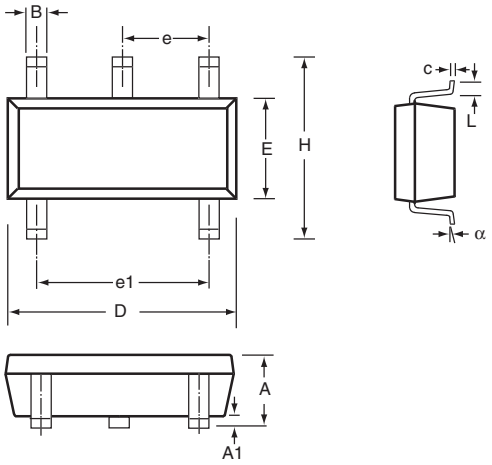



# Mechanical Dimensions

## 6-Lead SOT-23 Package




## 5-Lead SOT-23 Package




| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| A | .035 | .057 | .90 | 1.45 | |
| A1 | .000 | .006 | .00 | .15 | |
| B | .008 | .020 | .20 | .50 | |
| c | .003 | .010 | .08 | .25 | |
| D | .106 | .122 | 2.70 | 3.10 | |
| E | .059 | .071 | 1.50 | 1.80 | |
| e | .037 BSC | | .95 BSC | | |
| e1 | .075 BSC | | 1.90 BSC | | |
| H | .087 | .126 | 2.20 | 3.20 | |
| L | .004 | .024 | .10 | .60 | |
| α | 0° | 10° | 0° | 10° | |

**Notes:**

7. Package outline exclusive of mold flash & metal burr.
8. Packageoutline exclusive of solder plating.
9. EIAJ Ref Number SC_74A

## Ordering Information

$T_A$= -40°C to 85°C

| Part Number | Output Voltage | Package Marking | Package | Order Code |
|---|---|---|---|---|
| FAN2558 | 1.0V | 58T | 5-Lead SOT-23 | FAN2558S10X |
| | 1.2V | 58U | | FAN2558S12X |
| | 1.3V | 58X | | FAN2558S13X |
| | 1.5V | 58V | | FAN2558S15X |
| | 1.8V | 58O | | FAN2558S18X |
| | 2.5V | 58J | | FAN2558S25X |
| | 3.3V | 58K | | FAN2558S33X |
| | 3.5V | 58P | | FAN2558S35X |
| | 3.6V | 58Q | | FAN2558S36X |
| | 3.8V | 58I | | FAN2558S38X |
| | 1.0V | 58T | 2mm x 2mm 6-Lead MLP | FAN2558MP10X |
| | 1.2V | 58U | | FAN2558MP12X |
| | 1.3V | 58X | | FAN2558MP13X |
| | 1.5V | 58V | | FAN2558MP15X |
| | 1.8V | 58O | | FAN2558MP18X |
| | Adjustable | 58R | 6-Lead SOT-23 | FAN2558SX |
| | | 58R | 2mm x 2mm 6-Lead MLP | FAN2558MPX |
| FAN2559 | 1.0V | 59T | 6-Lead SOT-23 | FAN2559S10X |
| | 1.2V | 59U | | FAN2559S12X |
| | 1.3V | 59X | | FAN2559S13X |
| | 1.5V | 59V | | FAN2559S15X |
| | 1.8V | 59O | | FAN2559S18X |
| | 1.0V | 59T | 2mm x 2mm 6-Lead MLP | FAN2559MP10X |
| | 1.2V | 59U | | FAN2559MP12X |
| | 1.3V | 59X | | FAN2559MP13X |
| | 1.5V | 59V | | FAN2559MP15X |
| | 1.8V | 59O | | FAN2559MP18X |

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