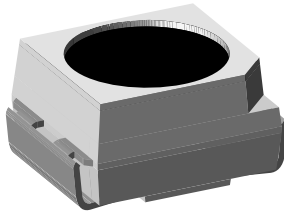


Silicon NPN Phototransistor



19032

DESCRIPTION

VEMT3700F is a high speed silicon NPN epitaxial planar phototransistor in a miniature PLCC-2 package. The integrated daylight blocking filter is matched to 950 nm IR emitters.

FEATURES

- Package type: surface mount
- Package form: PLCC-2
- Dimensions (L x W x H in mm): 3.5 x 2.8 x 1.75
- High radiant sensitivity
- Fast response times
- Daylight blocking filter matched with 870 nm to 950 nm emitters
- Angle of half sensitivity: $\varphi = \pm 60^\circ$
- Package notch indicates collector
- Package matched with IR emitter series VSML3710
- Floor life: 168 h, MSL 3, acc. J-STD-020
- Lead (Pb)-free reflow soldering
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC



RoHS
COMPLIANT
GREEN
(5-2008)**

APPLICATIONS

- Photo interrupters
- Miniature switches
- Counters
- Encoders
- Position sensors

PRODUCT SUMMARY

COMPONENT	I_{ca} (mA)	φ (deg)	$\lambda_{0.5}$ (nm)
VEMT3700F	0.5	± 60	870 to 1050

Note

- Test conditions see table "Basic Characteristics"

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
VEMT3700F-GS08	Tape and reel	MOQ: 7500 pcs, 1500 pcs/reel	PLCC-2
VEMT3700F-GS18	Tape and reel	MOQ: 8000 pcs, 8000 pcs/reel	PLCC-2

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Collector emitter voltage		V_{CEO}	70	V
Emitter collector voltage		V_{ECO}	5	V
Collector current		I_C	50	mA
Collector peak current	$t_p/T \leq 0.1, t_p \leq 10 \mu\text{s}$	I_{CM}	100	mA
Power dissipation		P_V	100	mW
Junction temperature		T_j	100	$^\circ\text{C}$
Operating temperature range		T_{amb}	- 40 to + 100	$^\circ\text{C}$
Storage temperature range		T_{stg}	- 40 to + 100	$^\circ\text{C}$
Soldering temperature	Acc. reflow solder profile fig. 10	T_{sd}	260	$^\circ\text{C}$
Thermal resistance junction/ambient	Soldered on PCB with pad dimensions: 4 mm x 4 mm	R_{thJA}	400	K/W

** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

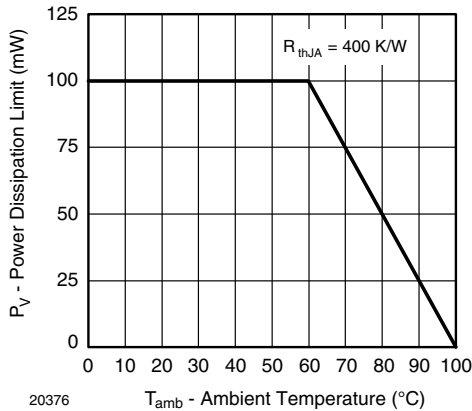


Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

BASIC CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Collector emitter breakdown voltage	I _C = 1 mA	V _{(BR)CEO}	70			V
Collector emitter dark current	V _{CE} = 20 V, E = 0	I _{CEO}		1	200	nA
Collector emitter capacitance	V _{CE} = 5 V, f = 1 MHz, E = 0	C _{CEO}		3		pF
Collector lighth current	E _e = 1 mW/cm ² , λ = 950 nm, V _{CE} = 5 V	I _{ca}	0.25	0.5		mA
Angle of half sensitivity		φ		± 60		deg
Wavelength of peak sensitivity		λ _p		940		nm
Range of spectral bandwidth		λ _{0.5}		870 to 1050		nm
Collector emitter saturation voltage	E _e = 1 mW/cm ² , λ = 950 nm, I _C = 0.1 mA	V _{CEsat}		0.15	0.3	V
Rise time, fall time	V _S = 5 V, I _C = 1 mA, λ = 950 nm, R _L = 1 kΩ	t _r /t _f		6		μs
	V _S = 5 V, I _C = 1 mA, λ = 950 nm, R _L = 100 Ω	t _r /t _f		2		μs
Cut-off frequency	V _S = 5 V, I _C = 2 mA, R _L = 100 Ω	f _c		180		kHz

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

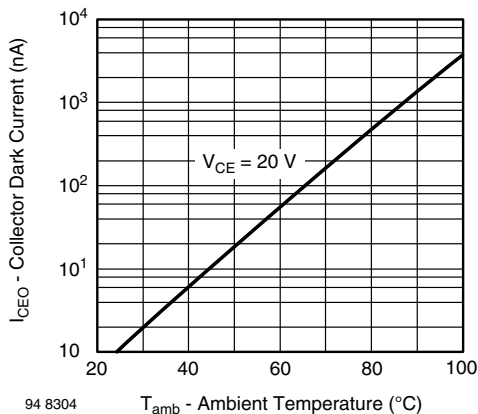


Fig. 2 - Collector Dark Current vs. Ambient Temperature

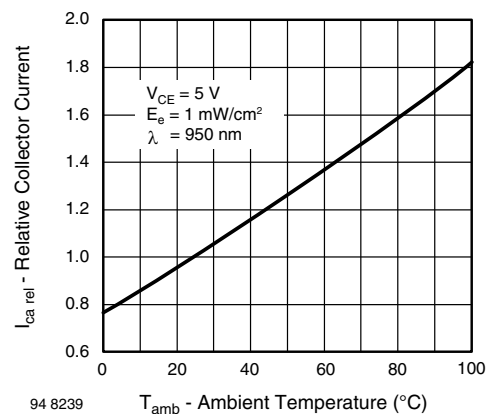


Fig. 3 - Relative Collector Current vs. Ambient Temperature

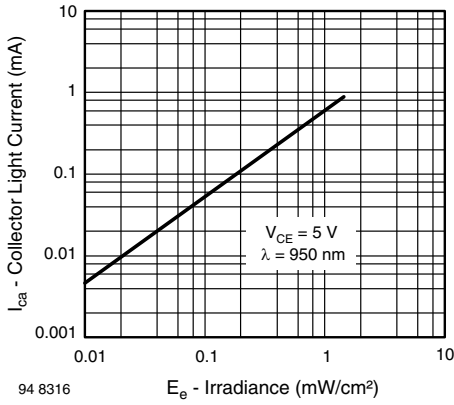


Fig. 4 - Collector Light Current vs. Irradiance

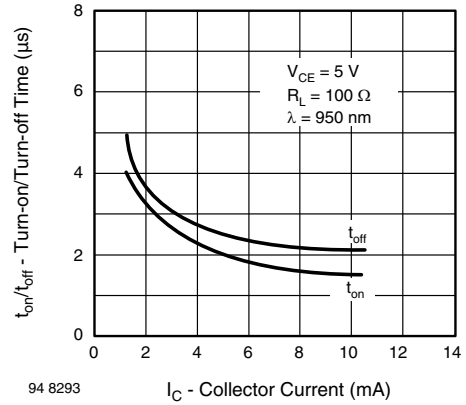


Fig. 7 - Turn-on/Turn-off Time vs. Collector Current

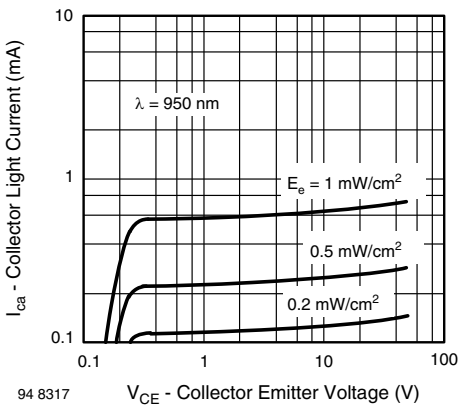


Fig. 5 - Collector Light Current vs. Collector Emitter Voltage

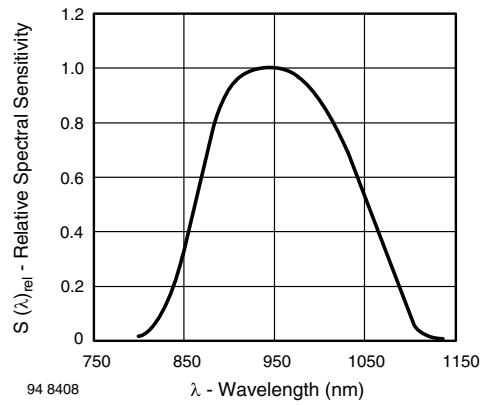


Fig. 8 - Relative Spectral Sensitivity vs. Wavelength

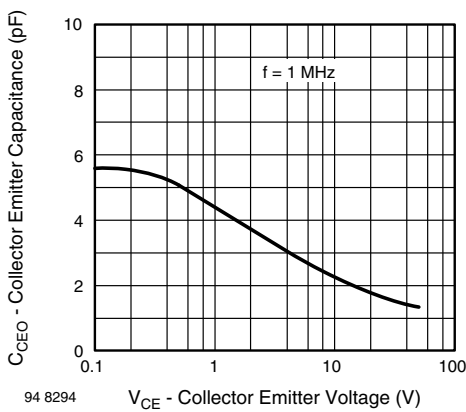


Fig. 6 - Collector Emitter Capacitance vs. Collector Emitter Voltage

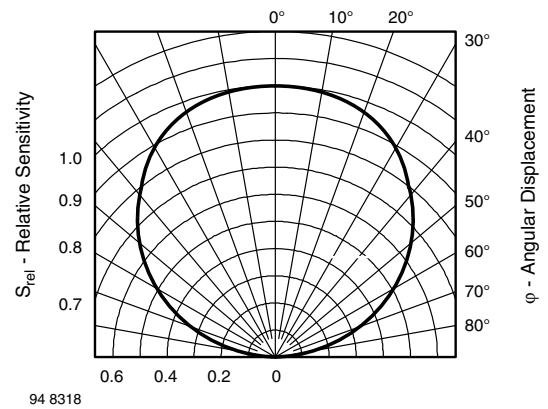
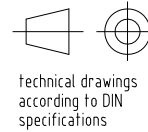
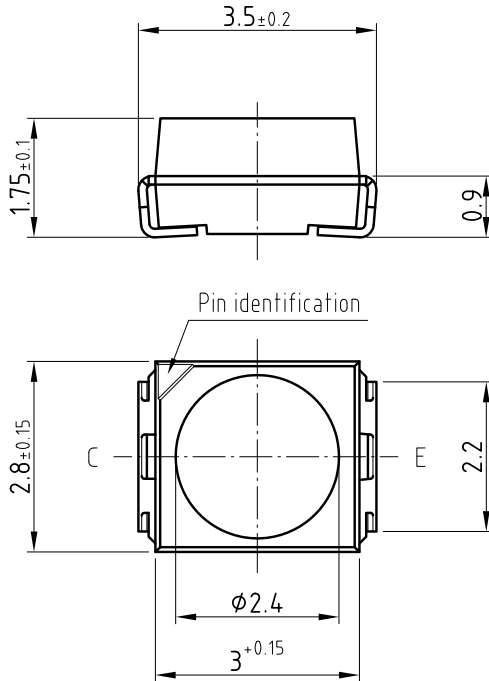
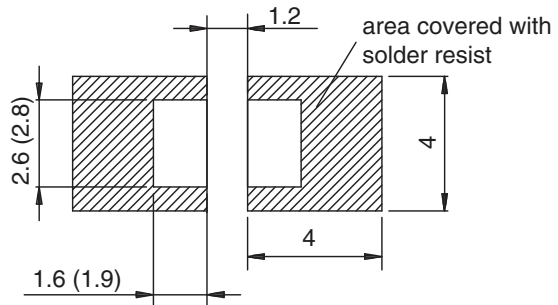


Fig. 9 - Relative Radiant Sensitivity vs. Angular Displacement

PACKAGE DIMENSIONS in millimeters



Mounting Pad Layout



Drawing-No.: 6.541-5067.03-4
Issue: 1; 30.05.07
20873

SOLDER PROFILE

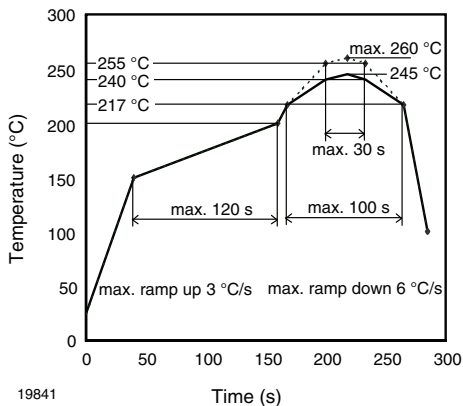


Fig. 10 - Lead (Pb)-free Reflow Solder Profile acc. J-STD-020

DRYPACK

Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.

FLOOR LIFE

Floor life (time between soldering and removing from MBB) must not exceed the time indicated on MBB label:

Floor life: 168 h

Conditions: $T_{amb} < 30\text{ °C}$, $RH < 60\%$

Moisture sensitivity level 3, acc. to J-STD-020.

DRYING

In case of moisture absorption devices should be baked before soldering. Conditions see J-STD-020 or label. Devices taped on reel dry using recommended conditions 192 h at 40 °C ($+ 5\text{ °C}$), $RH < 5\%$.

TAPE AND REEL

PLCC-2 components are packed in antistatic blister tape (DIN IEC (CO) 564) for automatic component insertion. Cavities of blister tape are covered with adhesive tape.

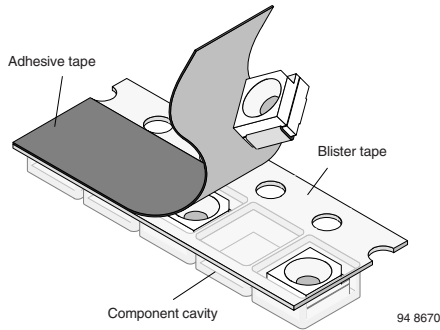


Fig. 11 - Blister Tape

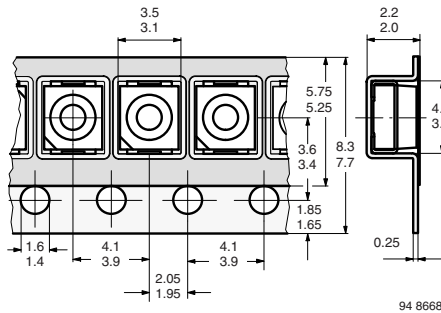


Fig. 12 - Tape Dimensions in mm for PLCC-2

MISSING DEVICES

A maximum of 0.5 % of the total number of components per reel may be missing, exclusively missing components at the beginning and at the end of the reel. A maximum of three consecutive components may be missing, provided this gap is followed by six consecutive components.

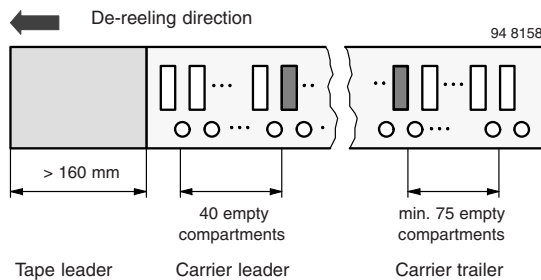


Fig. 13 - Beginning and End of Reel

The tape leader is at least 160 mm and is followed by a carrier tape leader with at least 40 empty compartments. The tape leader may include the carrier tape as long as the cover tape is not connected to the carrier tape. The least component is followed by a carrier tape trailer with a least 75 empty compartments and sealed with cover tape.

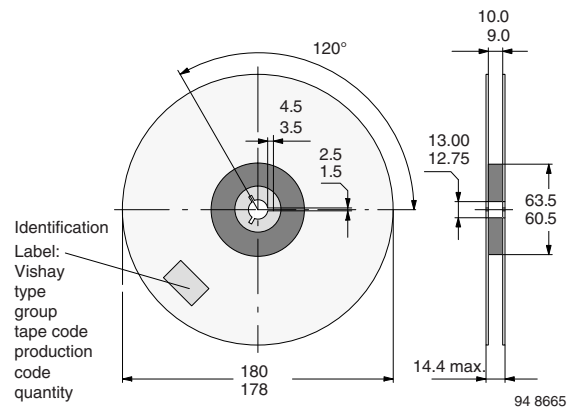


Fig. 14 - Dimensions of Reel-GS08

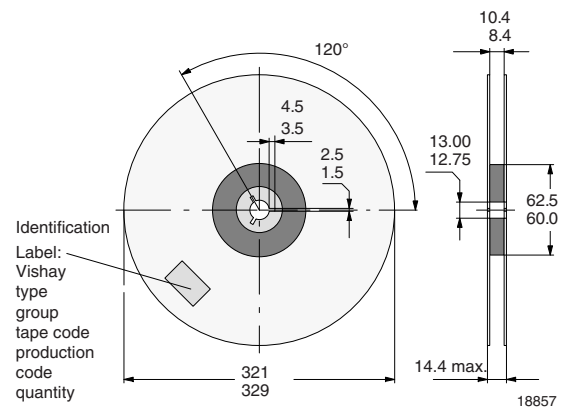


Fig. 15 - Dimensions of Reel-GS18

COVER TAPE REMOVAL FORCE

The removal force lies between 0.1 N and 1.0 N at a removal speed of 5 mm/s. In order to prevent components from popping out of the blisters, the cover tape must be pulled off at an angle of 180° with regard to the feed direction.



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