

FDD9409LE085

N-Channel Logic Level PowerTrench[®] MOSFET

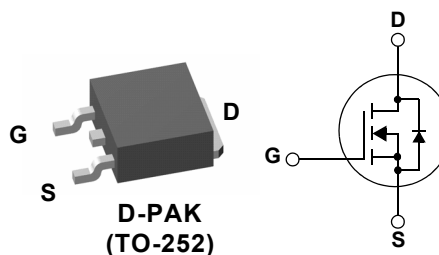
40 V, 90 A, 2.6 mΩ

Features

- Typical $R_{DS(on)}$ = 2.1 mΩ at $V_{GS} = 10V$, $I_D = 80 A$
- Typical $Q_{g(tot)}$ = 52 nC at $V_{GS} = 10V$, $I_D = 80 A$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (Note 1)	$T_C = 25^\circ C$	A
	Pulsed Drain Current	$T_C = 25^\circ C$	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	33.7	mJ
P_D	Power Dissipation	150	W
	Derate Above 25°C	1	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	52	°C/W

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^\circ C$, $L = 15\mu H$, $I_{AS} = 67A$, $V_{DD} = 40V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche.
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD9409L	FDD9409LE085	D-PAK(TO-252)	13"	16mm	2500units

Typical Characteristics

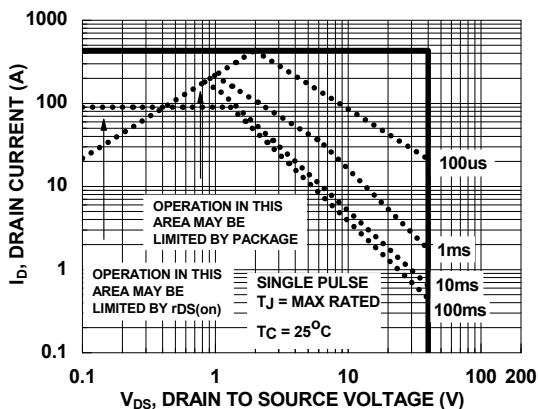
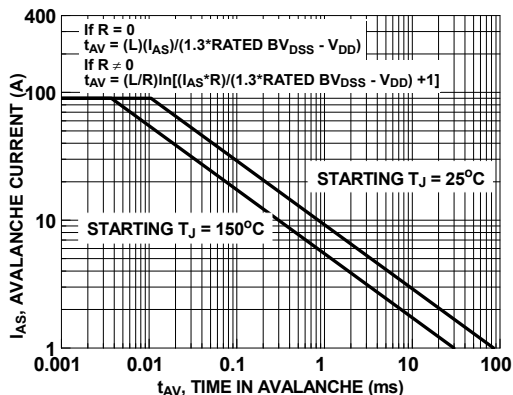


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to On Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

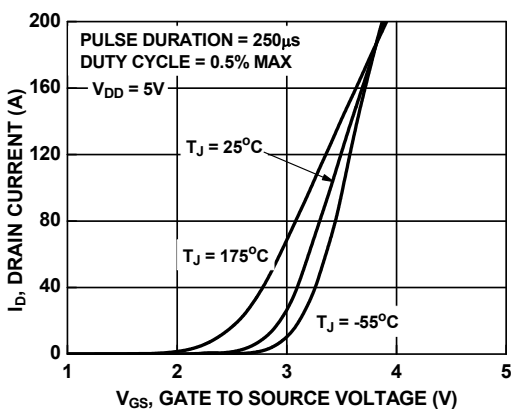


Figure 7. Transfer Characteristics

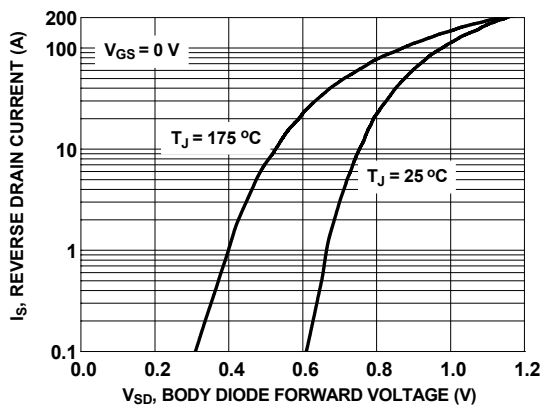


Figure 8. Forward Diode Characteristics

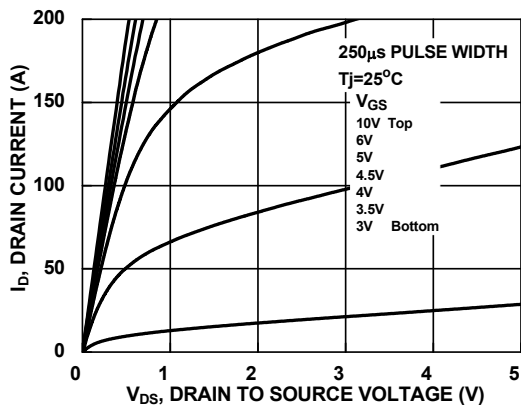


Figure 9. Saturation Characteristics

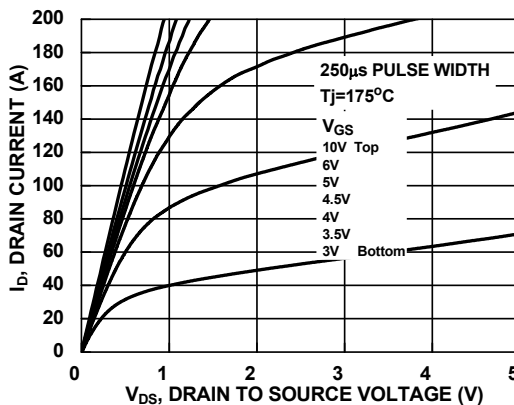


Figure 10. Saturation Characteristics

Typical Characteristics

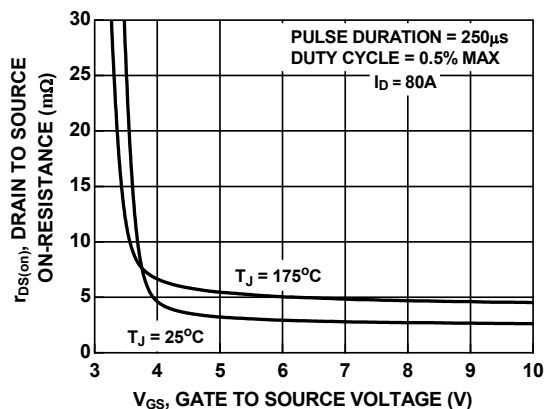


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

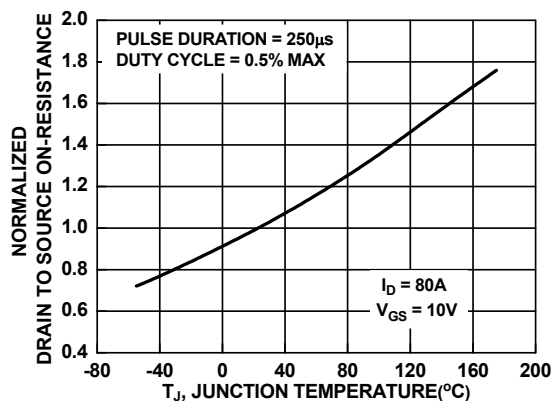


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

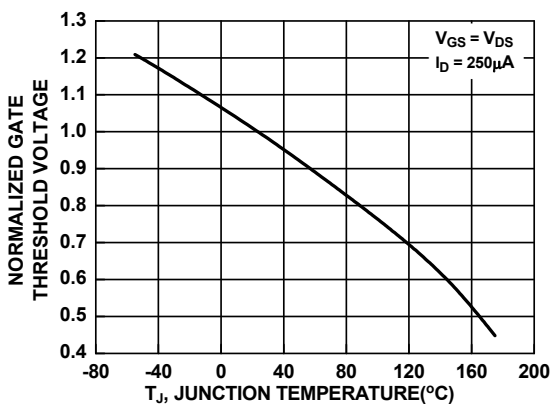


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

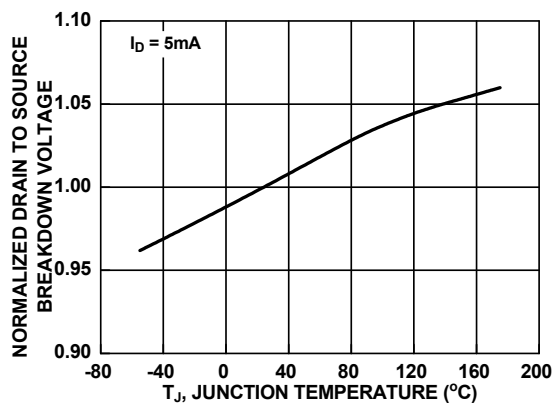


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

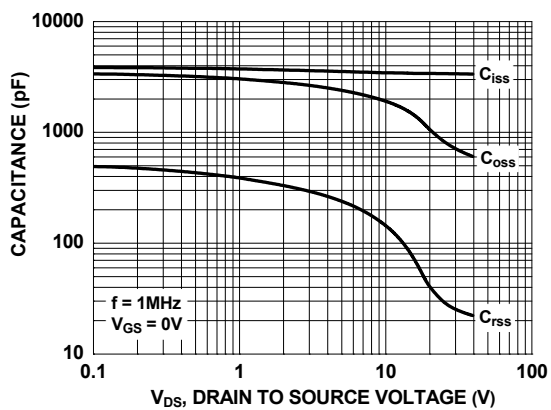


Figure 15. Capacitance vs. Drain to Source Voltage

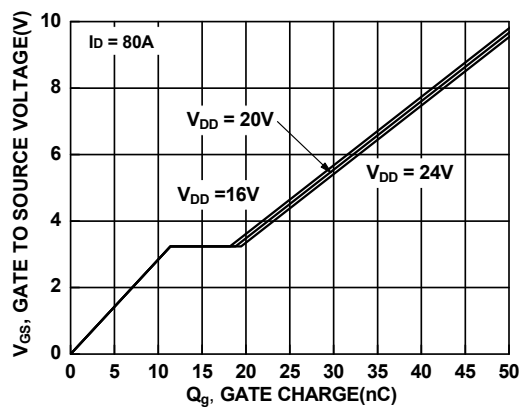


Figure 16. Gate Charge vs. Gate to Source Voltage