±15kV ESD Protected, +3.3V, 1µA, 250kbps, RS-232 Transmitters/Receivers

ICL3221EM, ICL3221EF

The Intersil ICL3221EM and ICL3221EF devices are 3.3V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Efficient on-chip charge pumps, coupled with manual and automatic power-down functions, reduce the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. These devices are fully compatible with 3.3V-only systems.

The ICL3221EM and ICL3221EF feature an automatic power-down function, which powers down the on-chip power-supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically without changes to the hardware or operating system. These devices power up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 summarizes the features of the ICL3221EM and ICL3221EF.

Related Literature

- For a full list of related documents, visit our web page
  - ICL3221EM product page
  - ICL3221EF product page

Features

- ESD protection for RS-232 I/O pins to ±15kV (IEC61000)
- RS-232 compatible with V_{CC} = 2.7V
- Meets EIA/TIA-232 and V.28/V.24 specifications at 3V
- Latch-up free
- On-chip voltage converters require only four external 0.1µF capacitors
- Manual and automatic power-down features
- Receiver hysteresis for improved noise immunity
- Guaranteed minimum data rate 250kbps
- Power supply range . . . . . single +3.0V to +3.6V
- Low supply current in power-down state. 1µA
- Pb-free (RoHS compliant)

Applications

- Any system requiring RS-232 communication ports
  - Battery powered, hand-held, and portable equipment
  - Modems, printers, and other peripherals

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NUMBER OF Tx	NUMBER OF Rx	DATA RATE (kbps)	RECEIVER ENABLE FUNCTION?	READY OUTPUT?	MANUAL POWER-DOWN?	AUTOMATIC POWER-DOWN FUNCTION?
ICL3221EM	1	1	250	Yes	No	Yes	Yes
ICL3221EF	1	1	250	Yes	No	Yes	Yes

Ordering Information

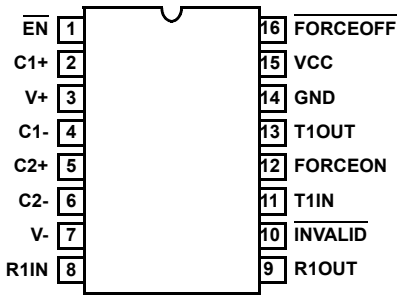
PART NUMBER (Notes 3, 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ICL3221EMVZ (Note 1)	3221 EMVZ	-55 to +125	16 Ld TSSOP	M16.173
ICL3221EFVZ (Note 2)	3221 EFVZ	-40 to +125	16 Ld TSSOP	M16.173

NOTES:

1. Add “-T” suffix for 2.5k unit tape and reel option. Refer to TB347 for details on reel specifications.
2. Add “-T” suffix for 2.5k unit or “-T7A” suffix for 250 unit tape and reel options. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see device information page for ICL3221EM, ICL3221EF. For more information on MSL, see techbrief TB363.

Pin Configuration

ICL3221EM, ICL3221EF
(16 LD TSSOP)
TOP VIEW



Pin Descriptions

PIN	PIN NUMBER	FUNCTION
$\overline{EN}$	1	Active low receiver enable control
C1+	2	External capacitor (voltage doubler) is connected to this lead.
V+	3	Internally generated positive transmitter supply (+5.5V).
C1-	4	External capacitor (voltage doubler) is connected to this lead.
C2+	5	External capacitor (voltage inverter) is connected to this lead.
C2-	6	External capacitor (voltage inverter) is connected to this lead.
V-	7	Internally generated negative transmitter supply (-5.5V).
R1IN	8	±15kV ESD protected, RS-232 compatible receiver inputs.
R1OUT	9	TTL/CMOS level receiver outputs.
$\overline{INVALID}$	10	Active low output that indicates if no valid RS-232 levels are present on any receiver input.
T1IN	11	TTL/CMOS compatible transmitter Inputs.
FORCEON	12	Active high input to override automatic power-down circuitry thereby keeping transmitters active ($\overline{FORCEOFF}$ must be high).
T1OUT	13	±15kV ESD protected, RS-232 level (nominally ±5.5V) transmitter outputs.
GND	14	Ground connection.
VCC	15	System power supply input (3.0V to 3.6V).
$\overline{FORCEOFF}$	16	Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (see Table 2 on page 7).

Typical Operating Circuit

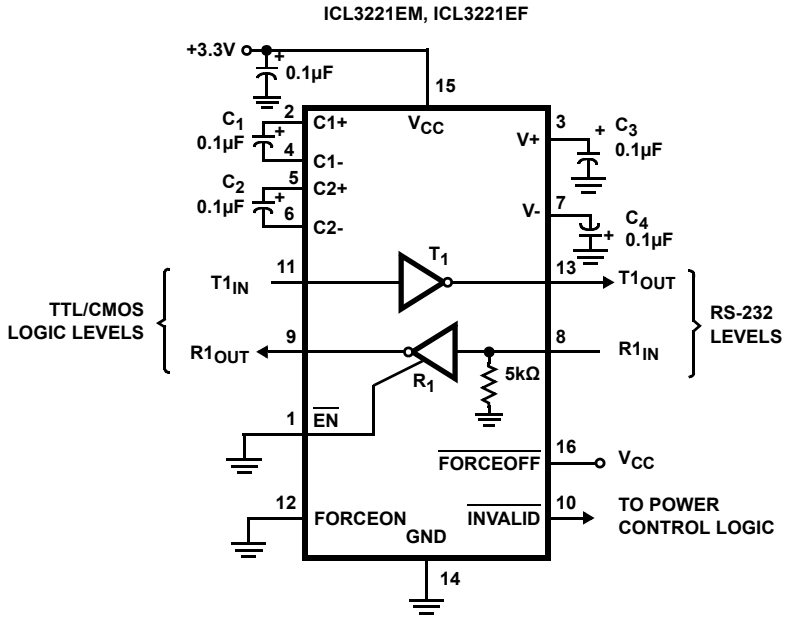


FIGURE 1. TYPICAL OPERATING CIRCUIT

Absolute Maximum Ratings

VCC to GND . . . . . -0.3V to 6V
V+ to GND . . . . . -0.3V to 7V
V- to GND . . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$ . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT}, $\overline{INVALID}$ . . . . . -0.3V to VCC +0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See specification table on page 5

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
16 Ld TSSOP Package	145

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Operating Conditions

Operating Voltage Range . . . . . +3.0V to +3.6V
Temperature Range (ICL3221EM) . . . . . -55°C to +125°C
Temperature Range (ICL3221EF) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test conditions: V_{CC} = 3.3V ±10%, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals at T_A = +25°C.
Boldface limits apply across the operating temperature ranges, -55°C to +125°C (ICL3221EM) and -40°C to +125°C (ICL3221EF).

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
DC CHARACTERISTICS						
Supply Current, Automatic Power-Down	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	Full	-	1.0	**10**	µA
Supply Current, Power-Down	$\overline{FORCEOFF}$ = GND	Full	-	1.0	**10**	µA
Supply Current, Automatic Power-Down Disabled	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = V_{CC}, V_{CC} = 3.15V	Full	-	0.3	**1.8**	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$	Full	-	-	**0.8**	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, V_{CC} = 3.3V	Full	**2.0**	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$	Full	-	±0.01	**±10**	µA
Output Leakage Current	$\overline{FORCEOFF}$ = GND or $\overline{EN}$ = V_{CC}	Full	-	±0.05	**±10**	µA
Output Voltage Low	I_{OUT} = 1.6mA	Full	-	-	**0.4**	V
Output Voltage High	I_{OUT} = -1.0mA	Full	**V_{CC} - 0.6**	V_{CC} - 0.1	-	V
AUTOMATIC POWER-DOWN (FORCEON = GND, FORCEOFF = VCC)						
Receiver Input Thresholds to Enable Transmitters	Power-up (see Figure 7)	Full	**-2.7**	-	**2.7**	V
Receiver Input Thresholds to Disable Transmitters	Power-down (see Figure 7)	Full	**-0.3**	-	**0.3**	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA	Full	-	-	**0.4**	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA	Full	**V_{CC} - 0.6**	-	-	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})		25	-	100	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay (t_{INVH})		25	-	1	-	µs

Electrical Specifications

Test conditions: V_{CC} = 3.3V ±10%, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals at T_A = +25°C. **Boldface limits apply across the operating temperature ranges, -55°C to +125°C (ICL3221EM) and -40°C to +125°C (ICL3221EF). (Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Receiver Positive or Negative Threshold to $\overline{\text{INVALID}}$ Low Delay (t_{INVL})			25	-	30	-	µs
RECEIVER INPUT							
Input Voltage Range			25	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			25	3	5	7	kΩ
TRANSMITTER OUTPUT							
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		Full	**±5.0**	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, transmitter output = ±2V		Full	**300**	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	**±60**	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 3.6V, automatic power-down or $\overline{\text{FORCEOFF}}$ = GND		Full	-	-	**±25**	µA
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		Full	**250**	500	-	kbps
Receiver Propagation Delay	Receiver input to receiver output, C_L = 150pF	t_{PHL}	25	-	0.15	-	µs
		t_{PLH}	25	-	0.15	-	µs
Receiver Output Enable Time	Normal operation		25	-	200	-	ns
Receiver Output Disable Time	Normal operation		25	-	200	-	ns
Transmitter Skew	t_{PHL} to t_{PLH} (Note 6)		25	-	100	1000	ns
Receiver Skew	t_{PHL} to t_{PLH}		25	-	50	1000	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured from 3V to -3V or -3V to 3V	C_L = 150pF to 2500pF	25	4	-	30	V/µs
		C_L = 150pF to 1000pF	25	6	-	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (TOUT, RIN)	Human body model		25	-	±15	-	kV
	IEC61000-4-2 contact discharge		25	-	±8	-	kV
	IEC61000-4-2 air gap discharge		25	-	±15	-	kV
All Other Pins	Human body model		25	-	±2	-	kV

NOTES:

6. Transmitter skew is measured at the transmitter zero crossing points.
7. Parts are 100% tested at +25°C. Full temperature limits are established by bench and tester characterization.

Detailed Description

ICL3221EM and ICL3221EF interface ICs operate from a single +3V supply, guarantee a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: charge pump, transmitters, and receivers.

Charge-Pump

Intersil's ICL3221EM and ICL3221EF utilize regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See "Capacitor Selection" on page 9 and Table 3 on page 9 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

The transmitter output disables and assumes a high impedance state when the device enters the power-down mode (see Table 2 on page 7). These outputs may be driven to ±12V when disabled.

All devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

Transmitter inputs float if left unconnected, and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

Receivers

The ICL3221EM and ICL3221EF devices contain standard inverting receivers that three-state via the $\overline{EN}$ or $\overline{FORCEOFF}$ control lines. The receivers convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 2) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

The ICL3221EM's and ICL3221EF's inverting receivers are disabled only when $\overline{EN}$ is driven high (see Table 2 on page 7).

Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 3 and 4 on page 7). This renders them useless for wake up functions, but the corresponding monitor receiver can be dedicated to this task as shown in Figure 4.

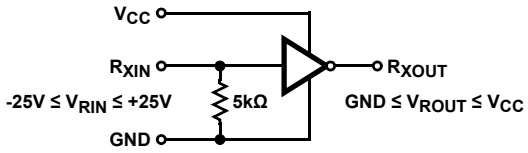


FIGURE 2. INVERTING RECEIVER CONNECTIONS

Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, during normal operation (not in power-down mode). This is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by switching to this new family.

Pin Compatible Replacements for 5V Devices

The ICL3221EM and ICL3221EF are pin compatible with existing 5V RS-232 transceivers - see the "Features" section on page 1 for details.

This pin compatibility coupled with the low I_{CC} and wide operating supply range, make the ICL3221EM and ICL3221EF potential lower power, higher performance drop-in replacements for existing 5V applications. As long as the ±5V RS-232 output swings are acceptable, and transmitter input pull-up resistors aren't required, the ICL3221EM, ICL3221EF should work in most 5V applications.

When replacing a device in an existing 5V application, it is acceptable to terminate C_3 to V_{CC} as shown on the "Typical Operating Circuit" on page 3. Nevertheless, terminate C_3 to GND if possible, as slightly better performance results from this configuration.

Power-Down Functionality

The already low current requirement drops significantly when the device enters power-down mode. In power-down, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter outputs three-state. Inverting receiver outputs may or may not disable in power-down; refer to Table 2 for details. This micro-power mode makes these devices ideal for battery powered and portable applications.

Software Controlled (Manual) Power-Down

The ICL3221EM and ICL3221EF devices provide a pin that allows the user to force the IC into the low power, standby state. Driving this pin high enables normal operation, while driving it low forces the IC into its power-down state. Connect $\overline{FORCEOFF}$ to V_{CC} if the power-down function isn't needed. Note that all the receiver outputs remain enabled during shutdown (see Table 2). For the lowest power consumption during power-down, the receivers should also be disabled by driving the $\overline{EN}$ input high (see Figures 3 and 4).

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	$\overline{\text{FORCEOFF}}$ INPUT	FORCEON INPUT	$\overline{\text{EN}}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
ICL3221EM, ICL3221EF							
No	H	H	L	Active	Active	L	Normal Operation (Auto Power-Down Disabled)
No	H	H	H	Active	High-Z	L	
Yes	H	L	L	Active	Active	H	Normal Operation (Auto Power-Down Enabled)
Yes	H	L	H	Active	High-Z	H	
No	H	L	L	High-Z	Active	L	Power-Down Due to Auto Power-Down Logic
No	H	L	H	High-Z	High-Z	L	
Yes	L	X	L	High-Z	Active	H	Manual Power-Down
Yes	L	X	H	High-Z	High-Z	H	Manual Power-Down with Receiver Disabled
No	L	X	L	High-Z	Active	L	Manual Power-Down
No	L	X	H	High-Z	High-Z	L	Manual Power-Down with Receiver Disabled

The ICL3221EM and ICL3221EF utilize a two pin approach where the FORCEON and $\overline{\text{FORCEOFF}}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{\text{FORCEOFF}}$ are both strapped high. To switch between active and power-down modes, under logic or software control, only the $\overline{\text{FORCEOFF}}$ input need be driven. The FORCEON state isn't critical, as $\overline{\text{FORCEOFF}}$ dominates over FORCEON. Nevertheless, if strictly manual control over power-down is desired, the user must strap FORCEON high to disable the automatic power-down circuitry.

The $\overline{\text{INVALID}}$ output always indicates whether or not a valid RS-232 signal is present at any of the receiver inputs (see Table 2), giving the user an easy way to determine when the interface block should power down. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{\text{INVALID}}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{\text{INVALID}}$ switches high, and the power management logic wakes up the interface block. $\overline{\text{INVALID}}$ can also be used to indicate the DTR or RING INDICATOR signal, as long as the other receiver inputs are floating, or driven to GND (as in the case of a powered down driver). Connecting $\overline{\text{FORCEOFF}}$ and FORCEON together disables the automatic power-down feature, enabling them to function as a manual $\overline{\text{SHUTDOWN}}$ input (see Figure 5 on page 8).

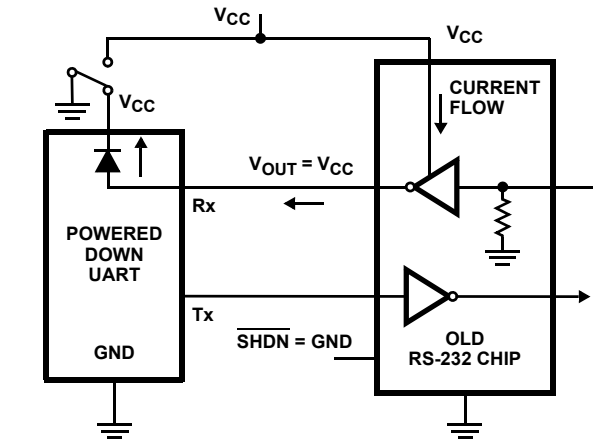


FIGURE 3. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

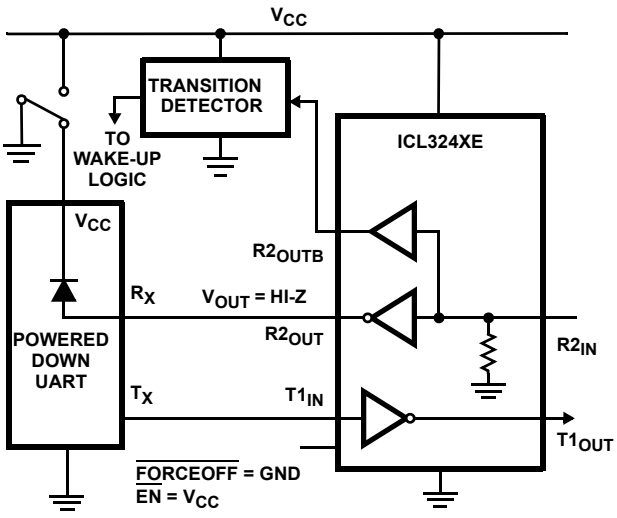


FIGURE 4. DISABLED RECEIVERS PREVENT POWER DRAIN

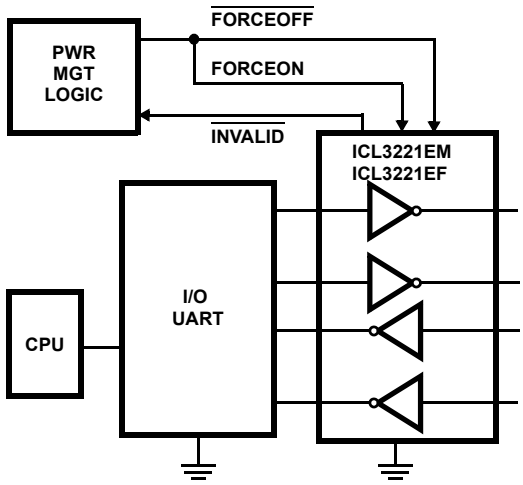


FIGURE 5. CONNECTIONS FOR MANUAL POWER-DOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

With any of the control schemes, the time required to exit power-down, and resume transmission is only 100µs. A mouse, or other application, may need more time to wake up from shutdown. If automatic power-down is being utilized, the RS-232 device will re-enter power-down if valid receiver levels aren't reestablished within 30µs of the ICL3221EM, ICL3221EF powering up. Figure 6 illustrates a circuit that keeps the ICL3221EM, ICL3221EF from initiating automatic power-down for 100ms after powering up. This gives the slow-to-wake peripheral circuit time to reestablish valid RS-232 output levels.

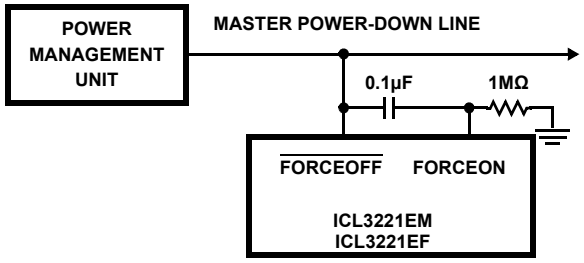


FIGURE 6. CIRCUIT TO PREVENT AUTO POWER-DOWN FOR 100ms AFTER FORCED POWER-UP

Automatic Power-Down

Even greater power savings is available by using the devices which feature an automatic power-down function. When no valid RS-232 voltages (see Figure 7) are sensed on any receiver input for 30µs, the charge pump and transmitters power-down, thereby reducing supply current to 1µA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ICL3221EM, ICL3221EF powers back up whenever it detects a valid RS-232 voltage level on any receiver input. This automatic power-down feature provides additional system power savings without changes to the existing operating system.

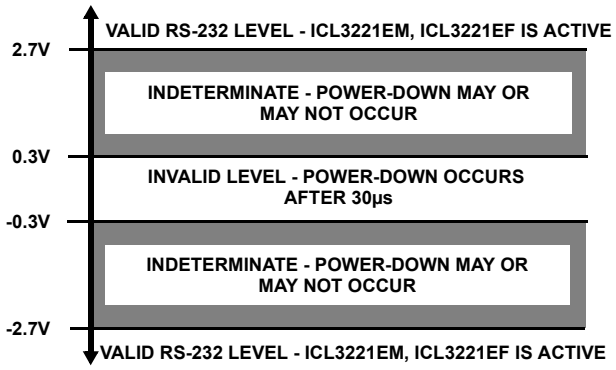


FIGURE 7. DEFINITION OF VALID RS-232 RECEIVER LEVELS

Automatic power-down operates when the FORCEON input is low, and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic power-down, but manual power-down is always available via the overriding $\overline{\text{FORCEOFF}}$ input. Table 2 on page 7 summarizes the automatic power-down functionality.

Devices with the automatic power-down feature include an $\overline{\text{INVALID}}$ output signal, which switches low to indicate that invalid levels have persisted on all of the receiver inputs for more than 30µs (see Figure 8). $\overline{\text{INVALID}}$ switches high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic power-down, or forced on), so it is also useful for systems employing manual power-down circuitry. When automatic power-down is utilized, $\overline{\text{INVALID}}$ = 0 indicates that the ICL3221EM, ICL3221EF is in power-down mode.

The time to recover from automatic power-down mode is typically 100µs.

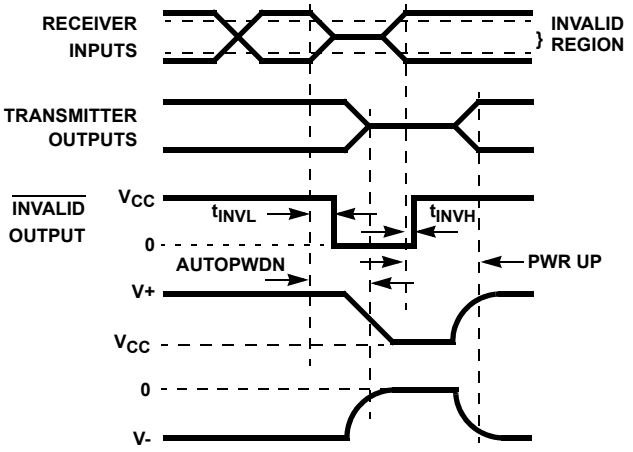


FIGURE 8. AUTOMATIC POWER-DOWN AND $\overline{\text{INVALID}}$ TIMING DIAGRAMS

Receiver ENABLE Control

Several devices also feature an $\overline{\text{EN}}$ input to control the receiver outputs. Driving $\overline{\text{EN}}$ high disables all the inverting (standard) receiver outputs placing them in a high impedance state. This is useful to eliminate supply current, due to a receiver output forward biasing the protection diode, when driving the input of a powered down (V_{CC} = GND) peripheral (see Figure 3 on page 7).

Capacitor Selection

The charge pumps require 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 3 for capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value, however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's Equivalent Series Resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

TABLE 3. REQUIRED CAPACITOR VALUES

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Operation Down to 2.7V

The ICL3221EM, ICL3221EF transmitter outputs meet RS-562 levels (±3.7V), at full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

Transmitter Outputs when Exiting Power-Down

Figure 9 shows the response of two transmitter outputs when exiting power-down mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

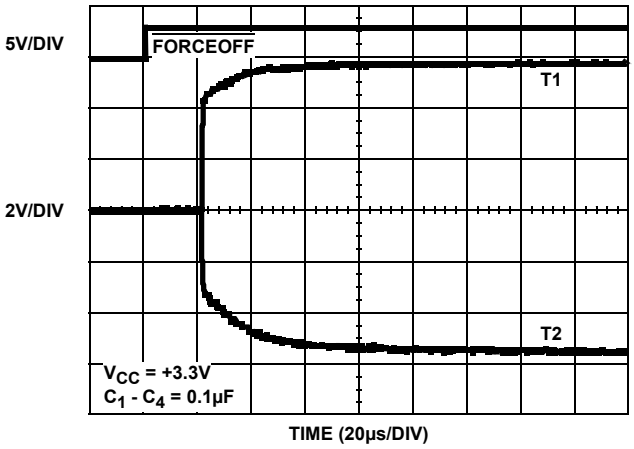


FIGURE 9. TRANSMITTER OUTPUTS WHEN EXITING POWER-DOWN

High Data Rates

The ICL3221EM, ICL3221EF maintains the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 10 details a transmitter loopback test circuit, and Figure 11 on page 10 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 12 on page 10 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

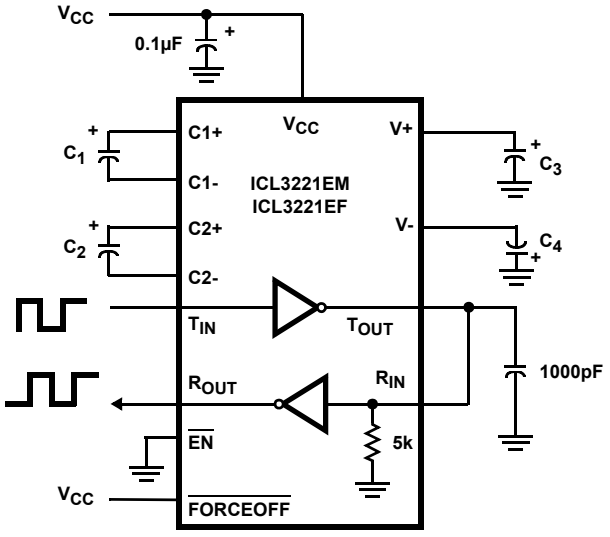


FIGURE 10. TRANSMITTER LOOPBACK TEST CIRCUIT

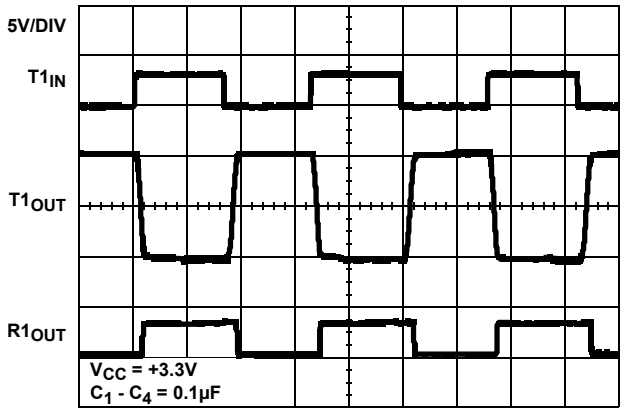


FIGURE 11. LOOPBACK TEST AT 120kbps

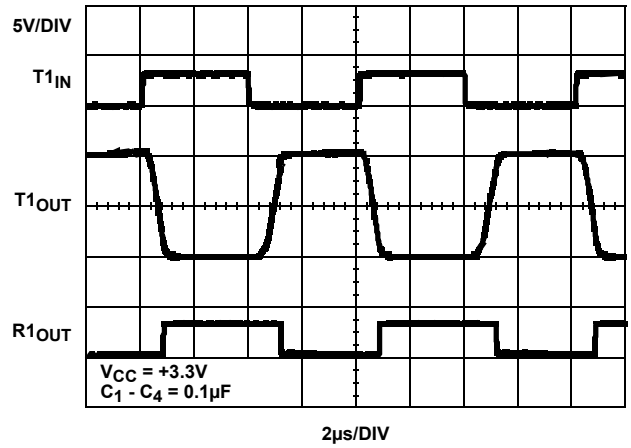


FIGURE 12. LOOPBACK TEST AT 250kbps

Interconnection with 3V and 5V Logic

The ICL3221EM, ICL3221EF directly interfaces with 5V CMOS and TTL logic families. Nevertheless, with the ICL3221EM, ICL3221EF at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL3221EM, ICL3221EF inputs, but ICL3221EM, ICL3221EF outputs do not reach the minimum V_{IH} for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.

±15kV ESD Protection

All pins on ICL3221EM and ICL3221EF devices include ESD protection structures, but the families incorporate advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latch-up mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test, which utilizes a 330Ω limiting resistor. The HBM method determines an IC's ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting Level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C.

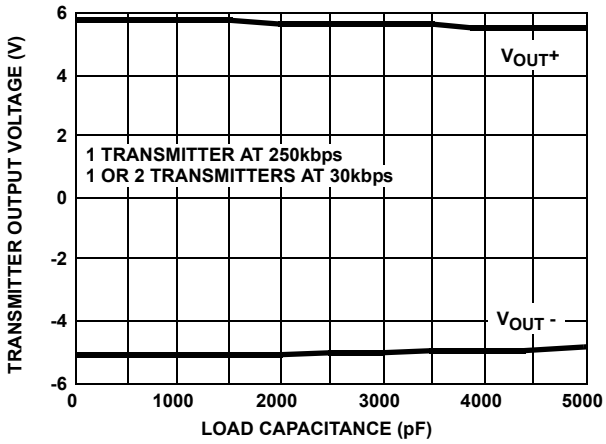


FIGURE 13. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

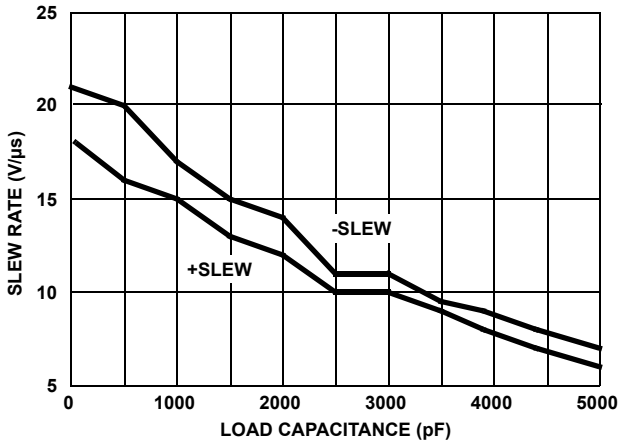


FIGURE 14. SLEW RATE vs LOAD CAPACITANCE

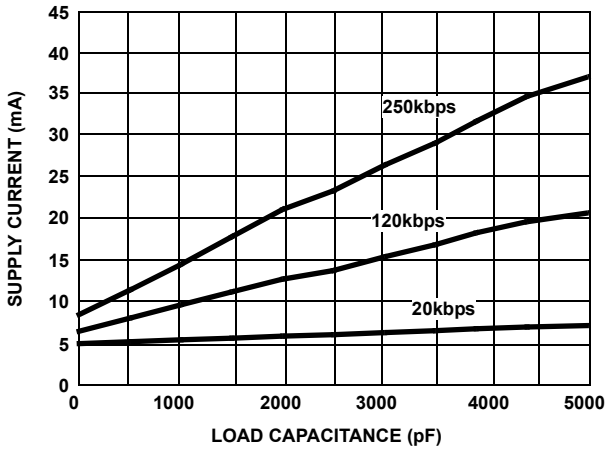


FIGURE 15. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

Die Characteristics

Substrate Potential (Powered Up):

GND

TRANSISTOR COUNT:

ICL3221EM, ICL3221EF: 286

PROCESS:

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 13, 2016	FN7552.1	Updated datasheet with new standards. In the first sentence on page 1 changed “3.0V” to “3.3V”. Removed second Features bullet on page 1. Removed PDAs, palmtops, notebooks, laptops, digital cameras, cellular/mobile phones application references on page 1. Added ICL3221EF information throughout datasheet. Added Revision History and About Intersil sections. Updated M16.173 package outline drawing to the most current revision, changes are as follows: -Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

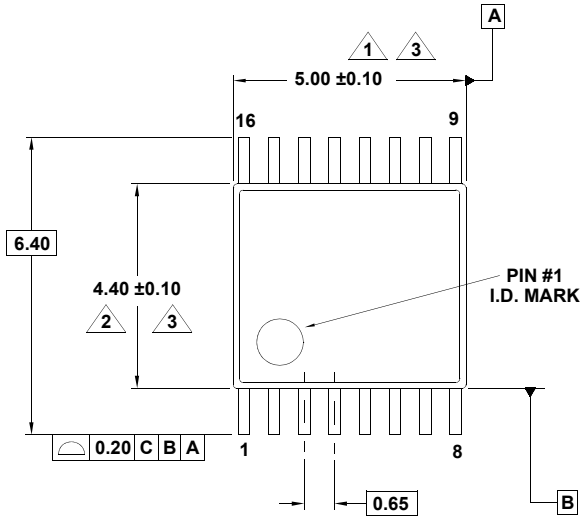
Package Outline Drawing

For the most recent package outline drawing, see M16.173.

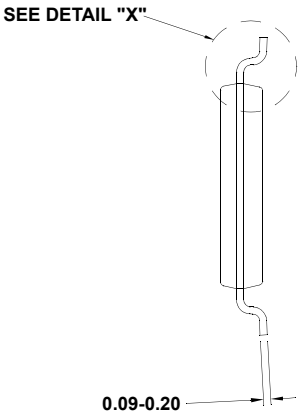
M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

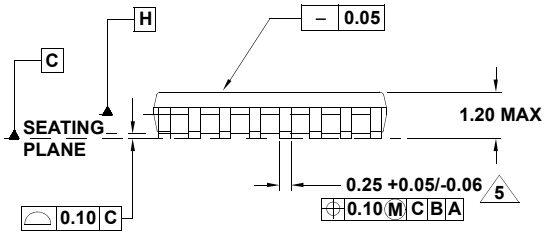
Rev 2, 5/10



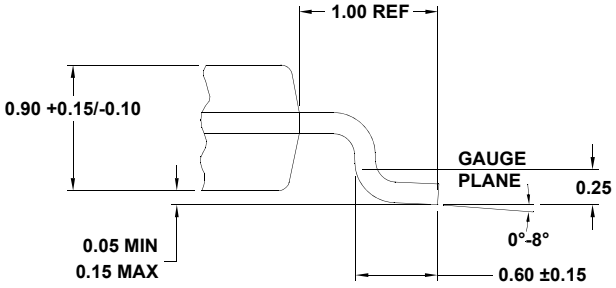
TOP VIEW



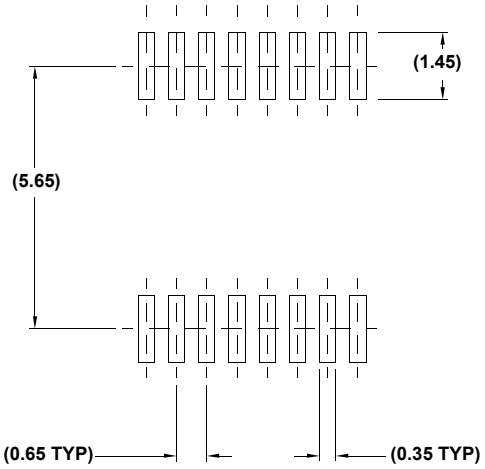
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.