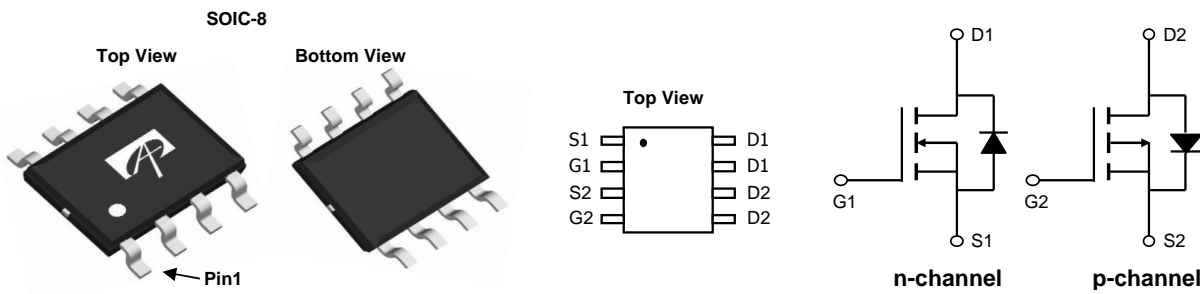


### General Description

The AO4622 uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

### Product Summary

N-Channel	P-Channel
$V_{DS}$ (V) = 20V	-20V
$I_D$ = 7.3A ( $V_{GS}=4.5V$ )	-5A ( $V_{GS}=-4.5V$ )
$R_{DS(ON)}$	$R_{DS(ON)}$
< 23m $\Omega$ ( $V_{GS}=10V$ )	< 53m $\Omega$ ( $V_{GS} = -4.5V$ )
< 30m $\Omega$ ( $V_{GS}=4.5V$ )	< 87m $\Omega$ ( $V_{GS} = -2.5V$ )
< 84m $\Omega$ ( $V_{GS}=2.5V$ )	
100% UIS Tested	100% UIS Tested
100% Rg Tested	100% Rg Tested



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	20	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	$\pm 12$	V
Continuous Drain Current <sup>A</sup>	$I_D$	7.3	-5	A
$T_A=25^\circ\text{C}$		6.2	-4.2	
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	35	-25	
Power Dissipation	$P_D$	2	2	W
		$T_A=25^\circ\text{C}$	1.44	
Avalanche Current <sup>B</sup>	$I_{AR}$	13	13	A
Repetitive avalanche energy 0.3mH <sup>B</sup>	$E_{AR}$	25	25	mJ
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	n-ch	48	62.5	$^\circ\text{C/W}$
		Steady-State	74	110	
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	n-ch	35	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	p-ch	48	62.5	$^\circ\text{C/W}$
		Steady-State	74	110	
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	p-ch	35	40	$^\circ\text{C/W}$

N-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=16\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 16\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	0.6	1.25	2	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}$ , $V_{DS}=5\text{V}$	35			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=7.3\text{A}$ $T_J=125^\circ\text{C}$		19 28	23 33.6	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=6.4\text{A}$		24	30	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}$ , $I_D=2\text{A}$		67	84	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=7.3\text{A}$		17		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$		0.7	1	V
$I_S$	Maximum Body-Diode Continuous Current				3	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=10\text{V}$ , $f=1\text{MHz}$		900	1100	pF
$C_{oss}$	Output Capacitance		162		pF	
$C_{riss}$	Reverse Transfer Capacitance		105		pF	
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		0.9	1.35	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=10\text{V}$ , $I_D=6.5\text{A}$		15	18	nC
$Q_g(4.5\text{V})$	Total Gate Charge		7.2	9	nC	
$Q_{gs}$	Gate Source Charge		1.8		nC	
$Q_{gd}$	Gate Drain Charge		2.8		nC	
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DS}=10\text{V}$ , $R_L=1.4\Omega$ , $R_{GEN}=3\Omega$		4.5		ns
$t_r$	Turn-On Rise Time		9.2		ns	
$t_{D(off)}$	Turn-Off DelayTime		18.7		ns	
$t_f$	Turn-Off Fall Time		3.3		ns	
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=7.3\text{A}$ , $di/dt=100\text{A}/\mu\text{s}$		18		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=7.3\text{A}$ , $di/dt=100\text{A}/\mu\text{s}$		9.5		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.  $R_{\theta JL}$  and  $R_{\theta JC}$  are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

F: The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.

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**N-CHANNEL TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

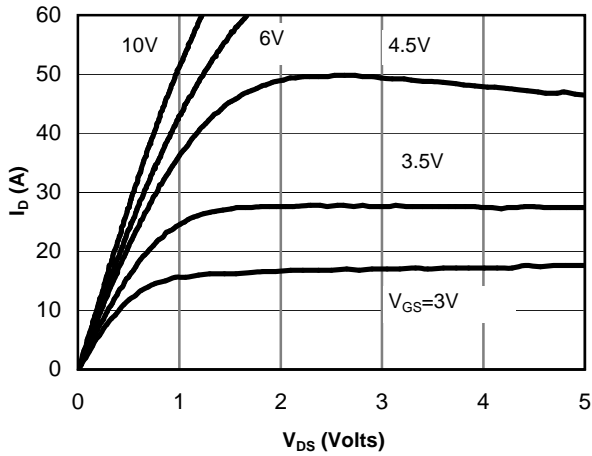


Figure 1: On-Region Characteristics

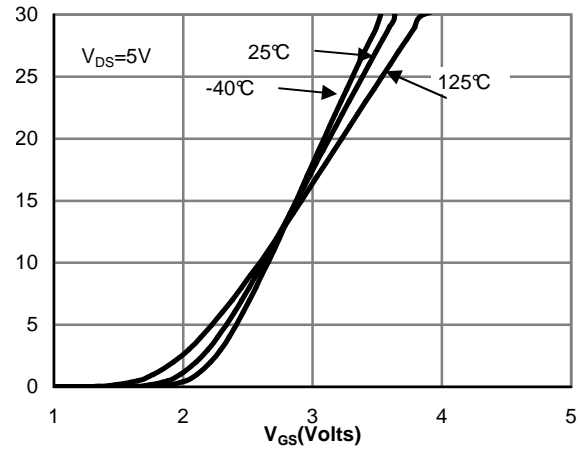


Figure 2: Transfer Characteristics

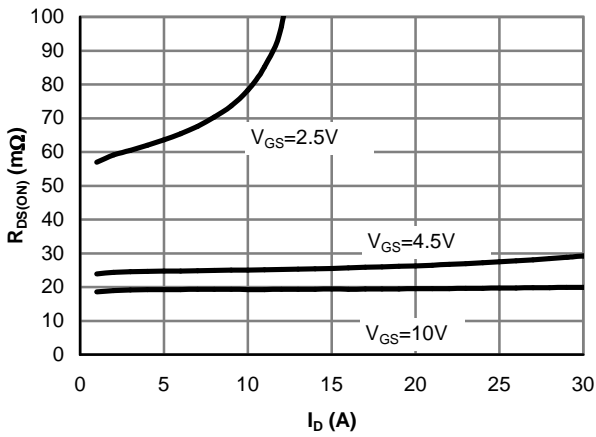


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

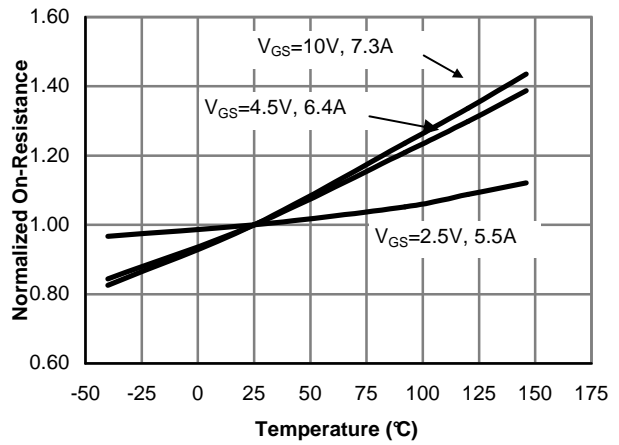


Figure 4: On-Resistance vs. Junction Temperature

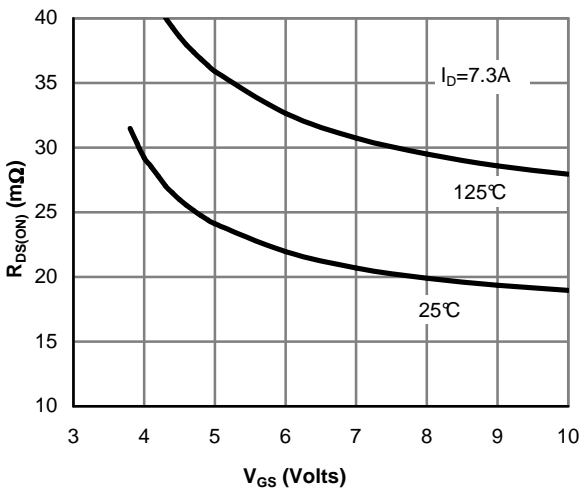


Figure 5: On-Resistance vs. Gate-Source Voltage

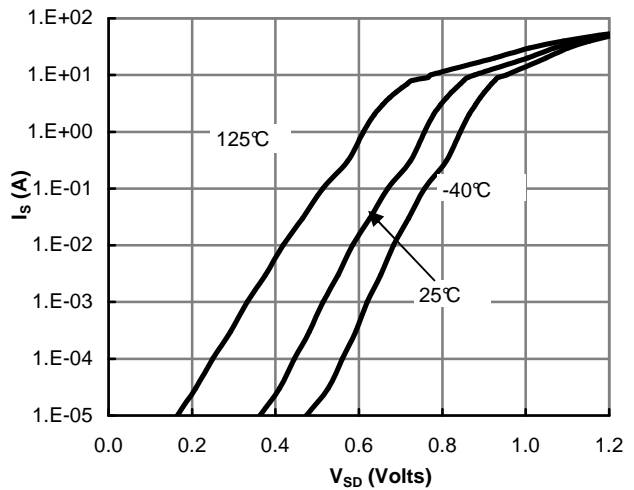


Figure 6: Body-Diode Characteristics

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

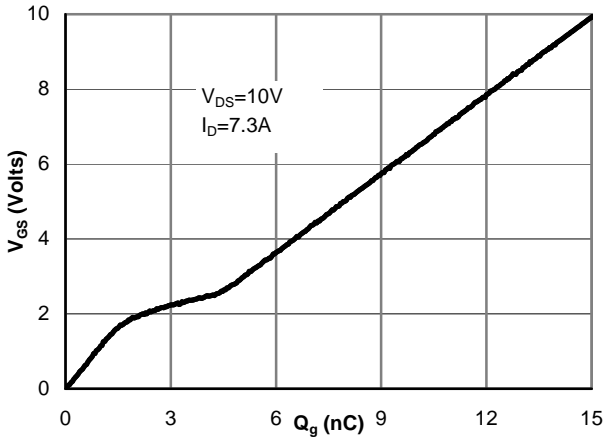


Figure 7: Gate-Charge Characteristics

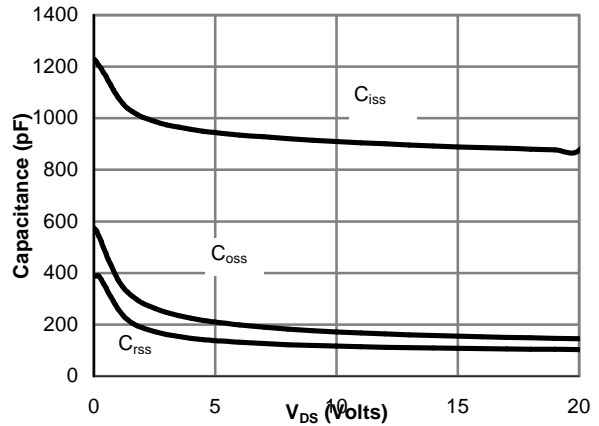


Figure 8: Capacitance Characteristics

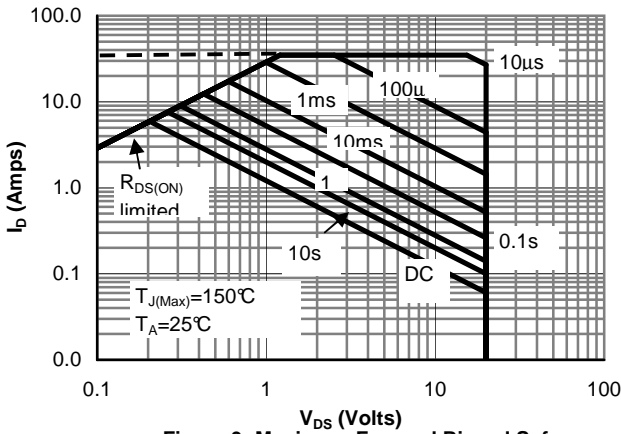


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

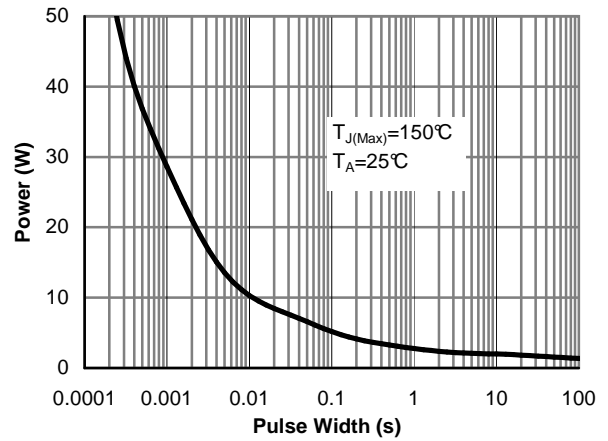


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

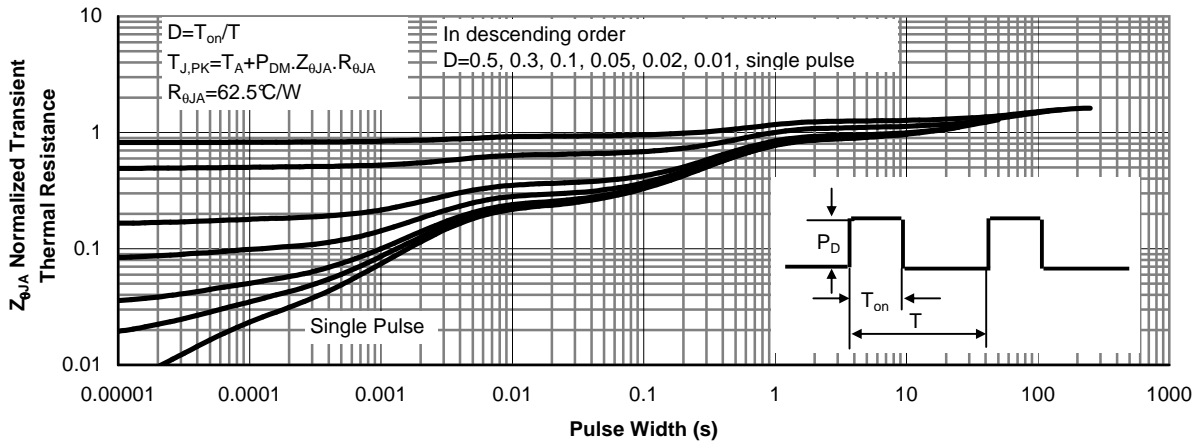
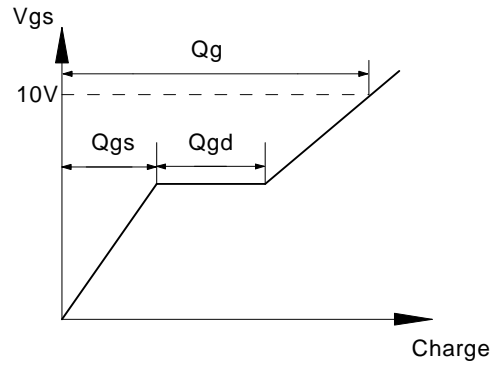
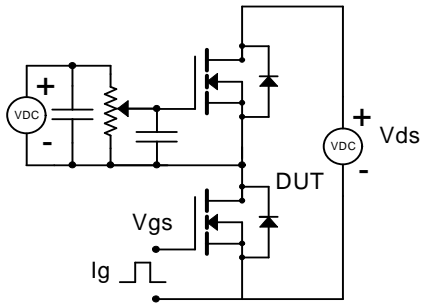
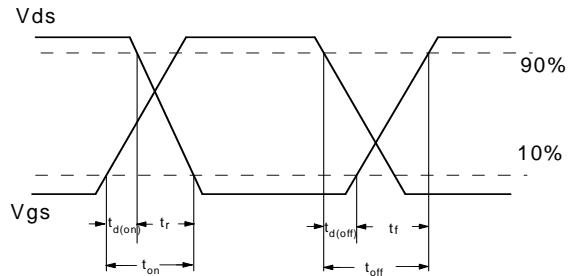
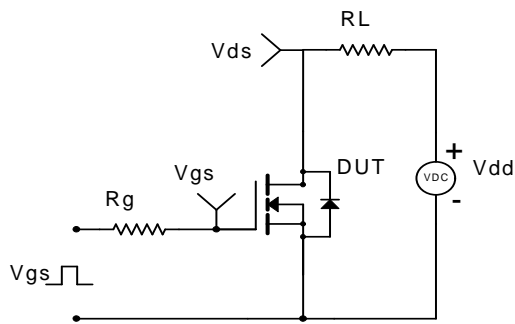


Figure 11: Normalized Maximum Transient Thermal Impedance

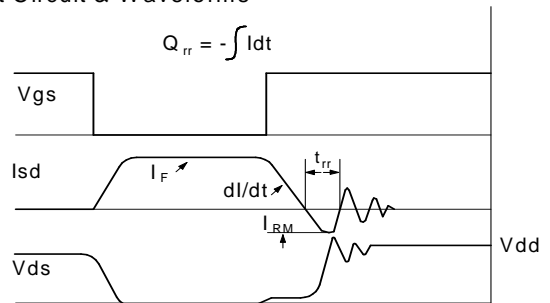
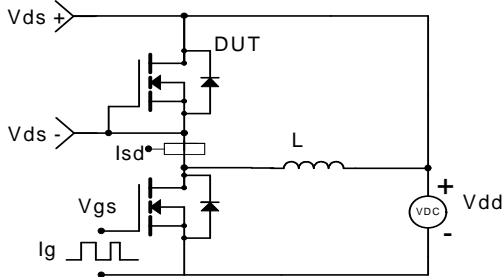
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V			-1	μA
		T <sub>J</sub> =55°C			-5	
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.3	-0.9	-0.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-5V	-25			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A		44	53	mΩ
		T <sub>J</sub> =125°C		59	71	
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4.2A		67	87	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-5A		13		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.76	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-10V, f=1MHz		800	960	pF
C <sub>oss</sub>	Output Capacitance			131		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			103		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		6.7	10	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge (10V)	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-4.5A		15.5		nC
Q <sub>g</sub> (4.5V)	Total Gate Charge (4.5V)			7.4		nC
Q <sub>gs</sub>	Gate Source Charge			1.3		nC
Q <sub>gd</sub>	Gate Drain Charge			2.9		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, R <sub>L</sub> =2Ω, R <sub>GEN</sub> =3Ω		4.4		ns
t <sub>r</sub>	Turn-On Rise Time			7.6		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			44		ns
t <sub>f</sub>	Turn-Off Fall Time			13.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-5A, dI/dt=100A/μs		20		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-5A, dI/dt=100A/μs		9		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient. R<sub>θJL</sub> and R<sub>θJC</sub> are equivalent terms referring to thermal resistance from junction to drain lead.

D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

F. The current rating is based on the t ≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

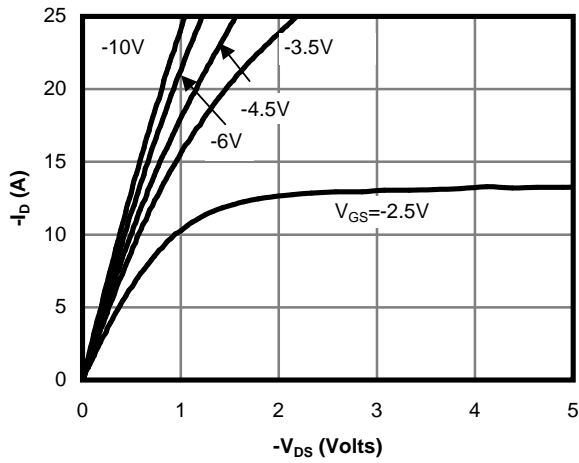


Fig 1: On-Region Characteristics

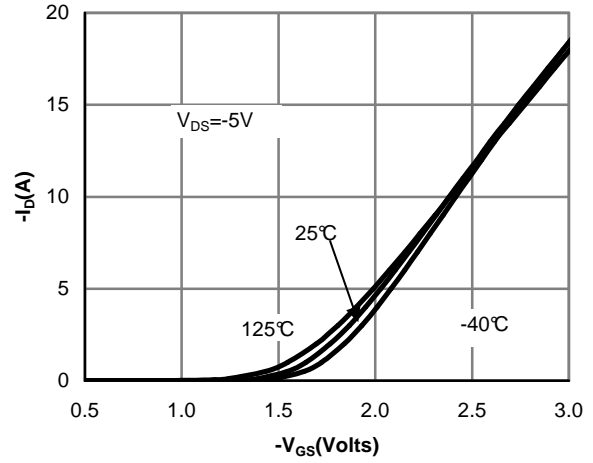


Figure 2: Transfer Characteristics

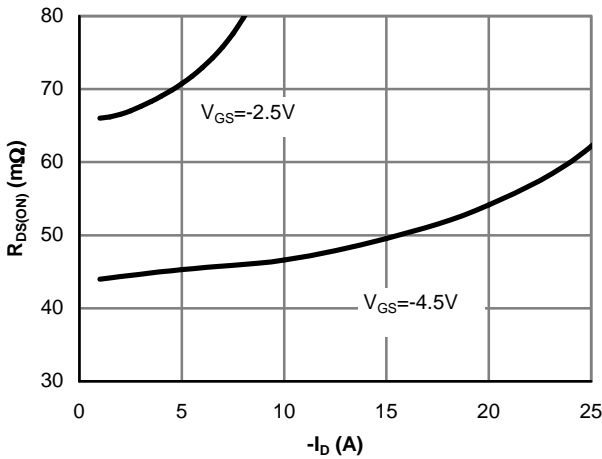


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

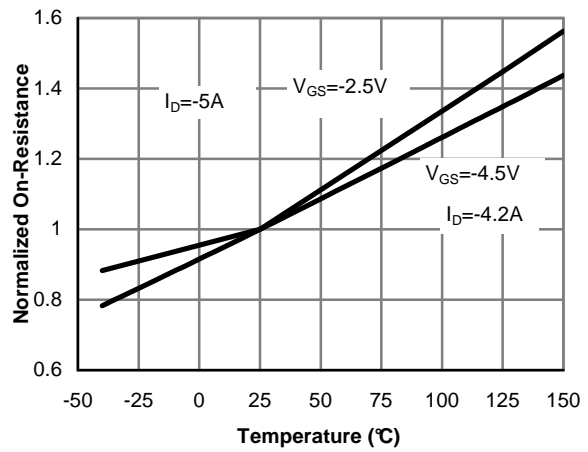


Figure 4: On-Resistance vs. Junction Temperature

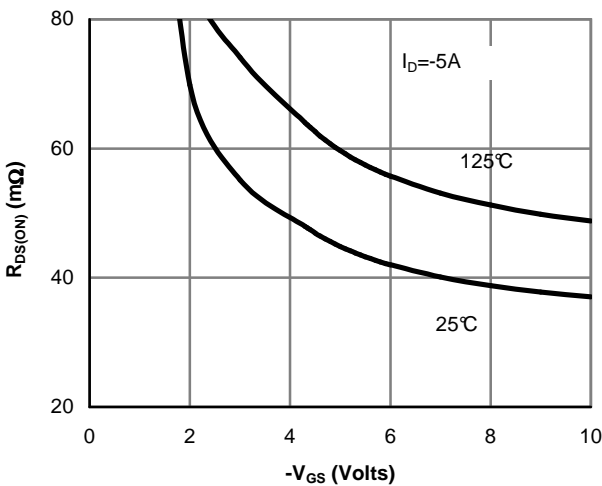


Figure 5: On-Resistance vs. Gate-Source Voltage

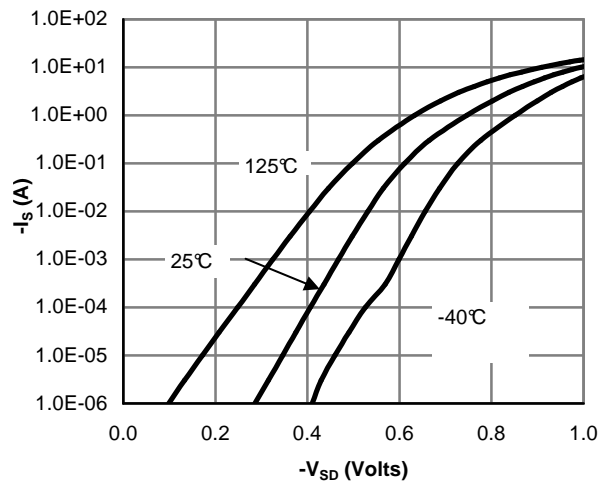


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

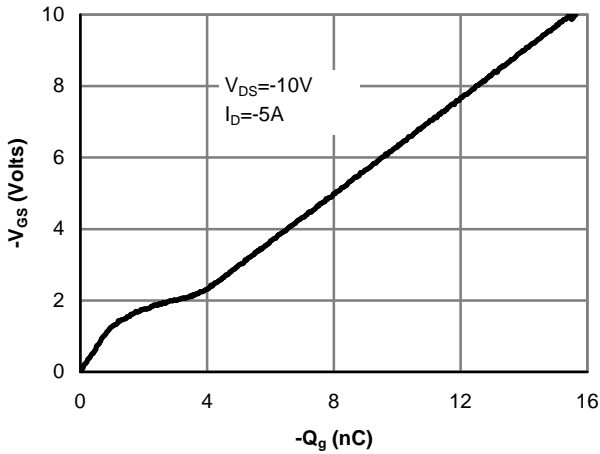


Figure 7: Gate-Charge Characteristics

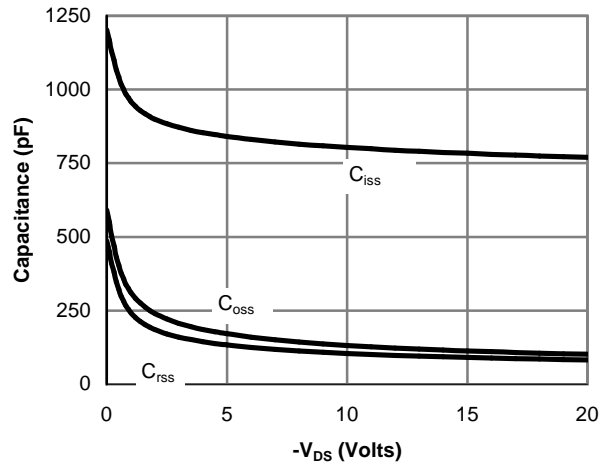


Figure 8: Capacitance Characteristics

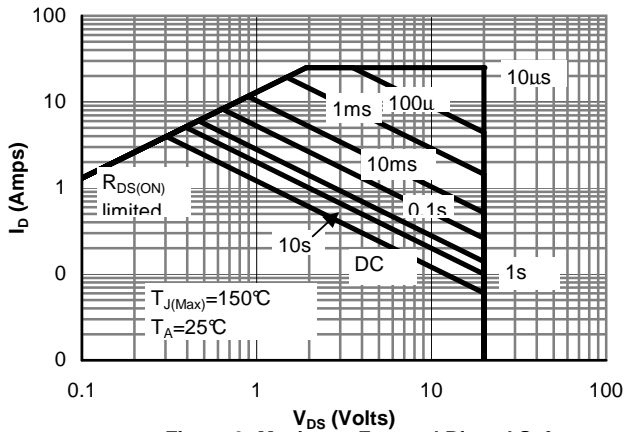


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

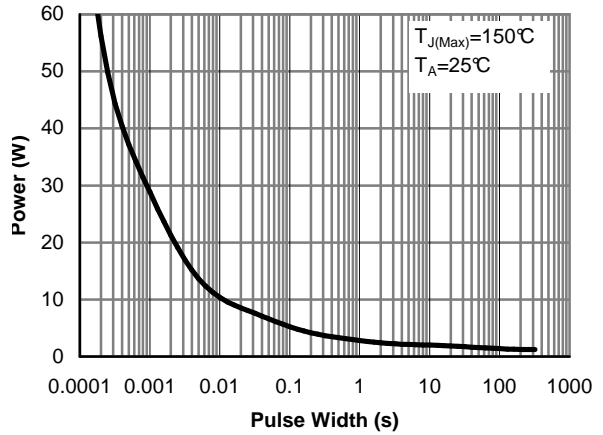


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

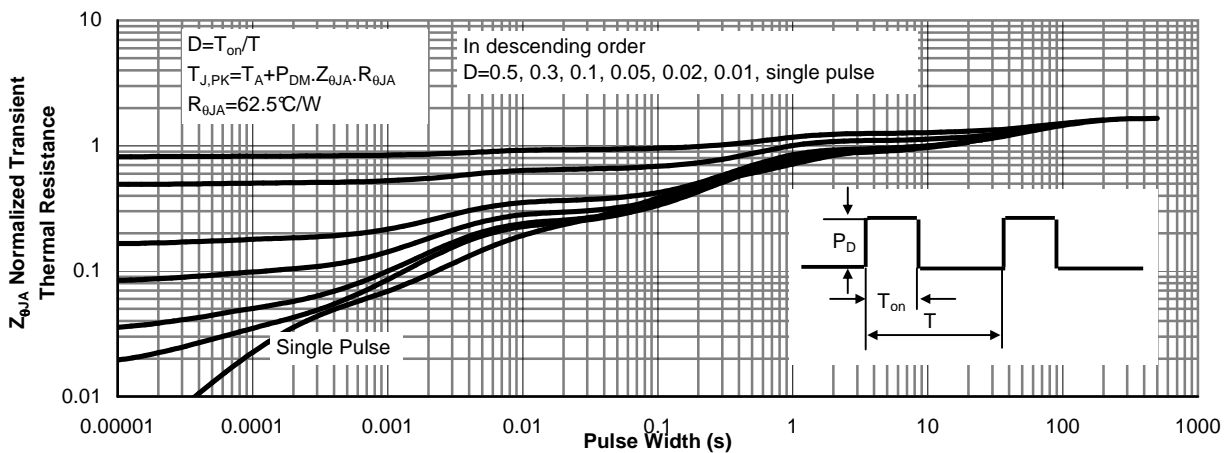
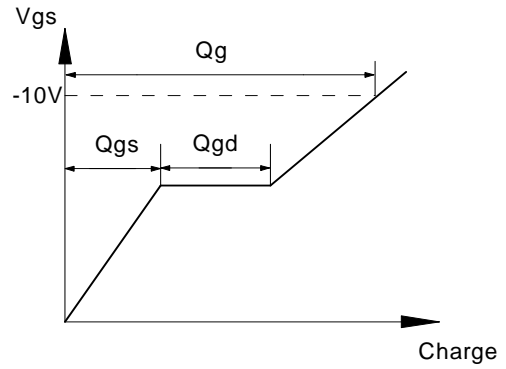
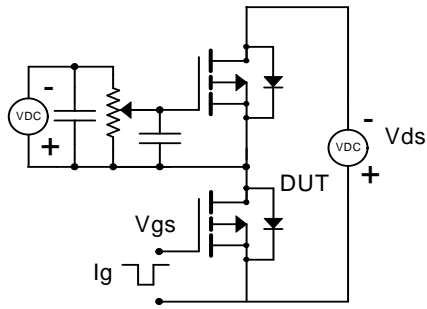


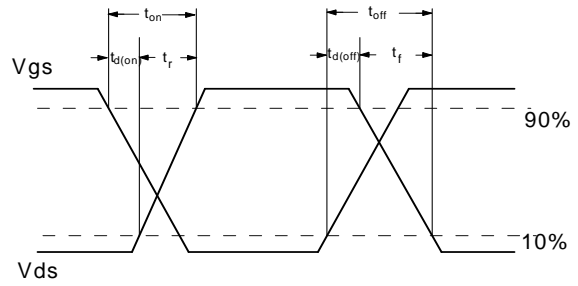
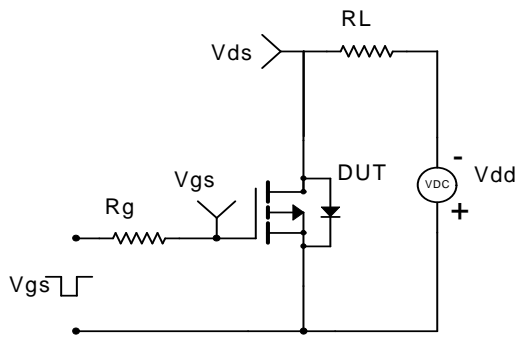
Figure 11: Normalized Maximum Transient Thermal Impedance



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

