SX8652

15kV ESD Low Power 4-Wire / 5-Wire Resistive Touchscreen Controller with SPI Interface

ADVANCED COMMUNICATIONS & SENSING DATASHEET

GENERAL DESCRIPTION

The SX8652 is a very low power, high reliability controller for 4-wire and 5-wire resistive touch screens used in PDAs, portable instruments and point-of-sales terminal applications. It features a wide input supply range from 1.65V to 3.7V and low power modes to preserve current when the screen is unintentionally touched.

To compute touch screen X-Y coordinates and touch pressure with precision, a low power 12-bit analog-digital converter is activated with the possibility to enable on-chip data averaging processing algorithms to reduce host activity and suppress system noise.

The touch screen controller inputs have been specially designed to provide robust on-chip ESD protection of up to ±15kV in both HBM and Contact Discharge, and eliminates the need for external protection devices. The SX8652 is controlled by a high speed SPI™ serial interface.

The SX8652 is available in a 4.0 mm x 3.0 mm 14-DFN package and a 1.5 mm x 2.0 mm wafer level chip scale package (WLCSP) for space conscience applications.

APPLICATIONS

- DSC, DVR, Cell Phones
- PDA, Pagers
- Point-of-Sales Terminals
- Touch-Screen Monitors

ORDERING INFORMATION

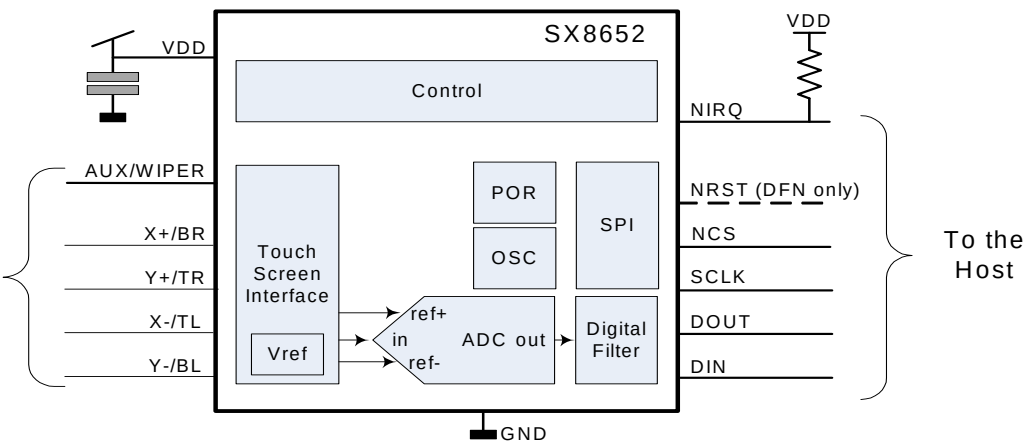
Part Number	Package (Dimension in mm)	Marking
SX8652ICSTRT[1]	12 - Ball WLCSP (1.5x2.0)	FG97
SX8652IWLTRT[1]	14 - Lead DFN (4.0x 3.0)	FG97

1. 3000 Units / reel

KEY PRODUCT FEATURES

- Extremely Low Power Consumption: 23uA@1.8V 8kSPS
- Superior On-chip ESD Protection
  - ➪±15kV HBM (X+,X-,Y+,Y-)
  - ➪±2kV CDM
  - ➪±25kV Air Gap Discharge
  - ➪±15kV Contact Discharge
  - ➪±300V MM
- Single 1.65V to 3.7V Supply/Reference
- 4-Wire or 5-Wire Resistive Touch Screen Interface
- Integrated Preprocessing Block to Reduce Host Loading and Bus Activity
- Four User Programmable Operation Modes provides Flexibility to address Different Application Needs
  - ➪Manual, Automatic, Pen Detect, Pen Trigger
- Low Noise Ratiometric Conversion
- Precision, High Speed 12-bit SAR ADC Operating At 74k SPS
- Throughput: 5000 (X-Y) coordinates/second (c/s) with 7-Sample Averaging
- Low Power Shut-Down Mode < 1uA
- SPI™ Serial Interface
- Touch Pressure Measurement (4-Wire)
- Auxiliary Input (4-Wire) For Alternate ADC Input or Start of Conversion Trigger
- Hardware & Software reset
- -40℃ to +85℃ operation
- Pb-Free, Halogen Free, RoHS/WEEE compliant product
- Windows CE 6.0, Linux Driver Support Available
- Packages: 14-LD (4.0 mm x 3.0 mm) DFN
  12-Ball (1.5 mm x 2.0 mm) WLCSP

To the touch screen



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1.1. DFN Pinout Diagram and Marking Information (Top View)

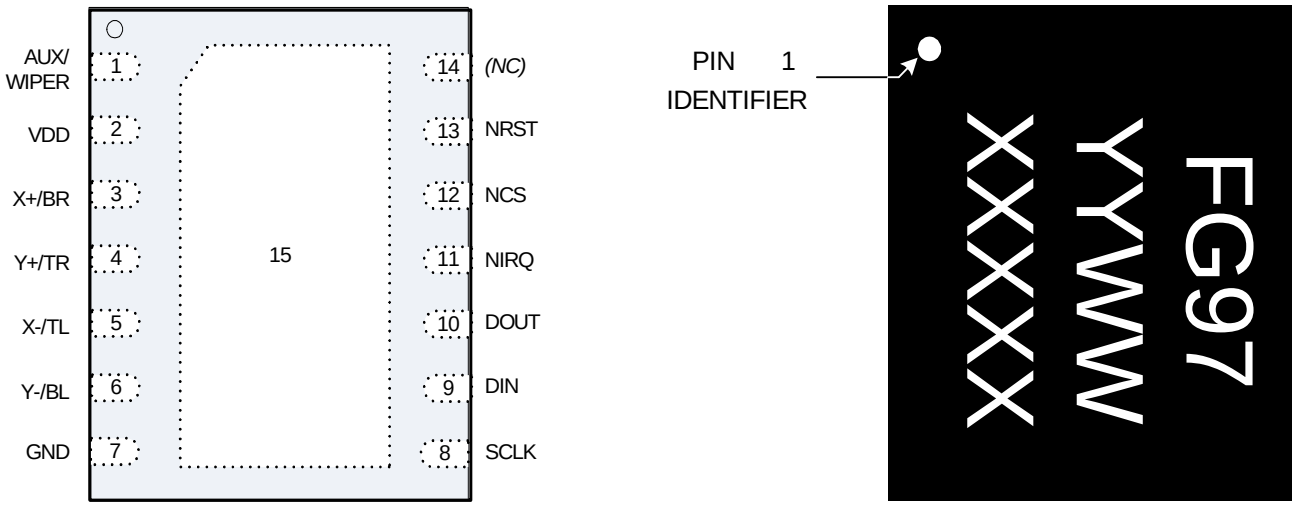


Figure 1. SX8652 DFN Top View, Pad on Bottom Side

YYWW: date code

XXXXX: Lot Number

1.2. WLCSP Pinout Diagram and Marking Information (Top View)

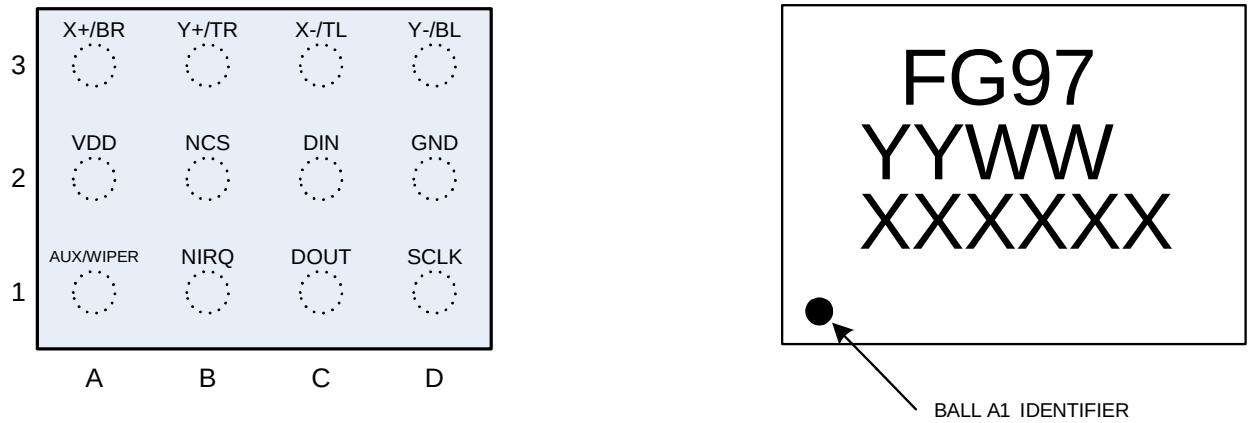


Figure 2. SX8652 WLCSP Top View, Solder Bumps on Bottom Side

YYWW: date code

XXXXX: Lot Number

1.3. Pin Description

Pin Number #		Name	Type	Description
DFN	WLCSP			
1	A1	AUX/WIPER	Digital Input / Analog Input	Conversion Synchronization (4-wire) or Analog Auxiliary Input (4-wire) / Wiper Input (5-wire)
2	A2	VDD	Power Input	Input power supply, connect to a 0.1uF capacitor to GND
3	A3	X+/BR	Analog IO	X+ Right electrode (4-wire) / Bottom Right (5-wire) channel
4	B3	Y+/TR	Analog IO	Y+ Top electrode (4-wire) /Top Right (5-wire) channel
5	C3	X-/TL	Analog IO	X- Left electrode (4-wire) /Top Left (5-wire) channel
6	D3	Y-/BL	Analog IO	Y- Bottom electrode (4-wire) /Bottom Left (5-wire) channel
7	D2	GND	Ground	Ground
8	D1	SCLK	Digital Input	SPI Serial Clock Input
9	C2	DIN	Digital Output	SPI Serial Data Input
10	C1	DOUT	Digital Output	SPI Serial Data Output
11	B1	NIRQ	Digital Output, open drain	Interrupt Request Output, Active low, Need external pull-up
12	B2	NCS	Digital Input	SPI Chip Select Input, Active low
13	-	NRST	Digital Input	DFN package only, Reset Input, Active low, Internal pull-up resistor
14	-	(NC)		Not Connected
15	-	GND	Power input	Backside Ground

Table 1. Pin description

1.4. Simplified Block Diagram

The SX8652 simplified block diagram is shown in Figure 3.

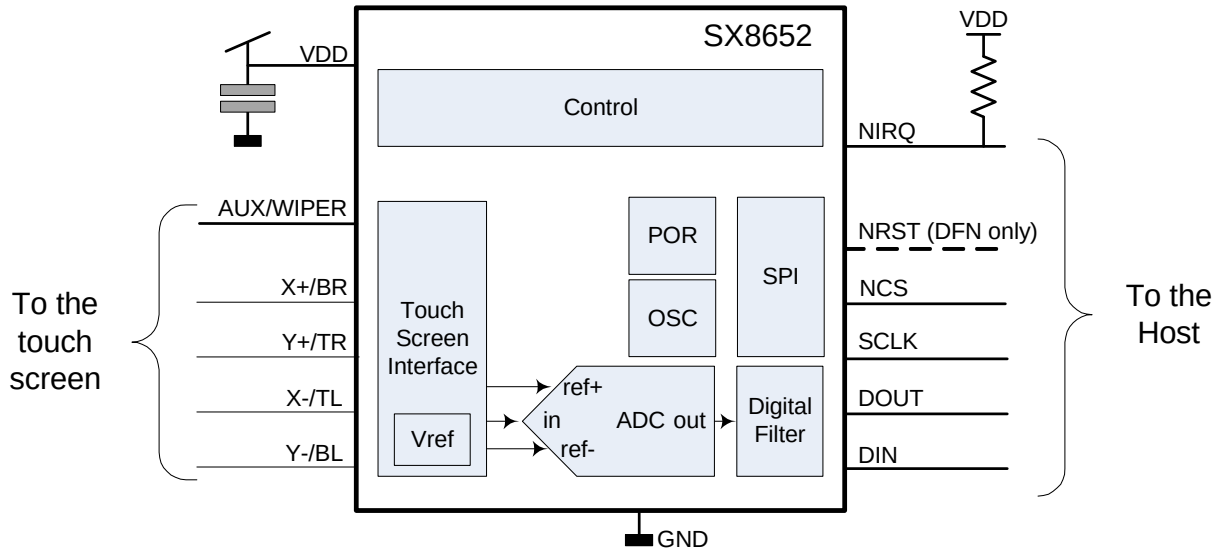


Figure 3. Simplified block diagram of the SX8652

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Stresses above the values listed in “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these, or any other conditions beyond the “Recommended Operating Conditions”, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage		V_{DDABS}	-0.5	3.9	V
Input voltage (non-supply pins)		V_{IN}	-0.5	3.9	V
Input current (non-supply pins)		I_{IN}		10	mA
Operating Junction Temperature		T_{JCT}		125	℃
Reflow temperature		T_{RE}		260	℃
Storage temperature		T_{STOR}	-50	150	℃
ESD HBM (Human Body Model)	High ESD pins: X+/BR, X-/TL, Y+/TR, Y-/BL, Aux/Wiper	ESD_{HBM1}	± 15(i)		kV
			± 8(ii)		kV
	All pins except high ESD pins	ESD_{HBM2}	± 2		kV
ESD (Contact Discharge)	High ESD pins: X+/BR, X-/TL, Y+/TR, Y-/BL, Aux/Wiper	ESD_{CD}	± 15		kV
Latchup(iii)		I_{LU}	± 100		mA

Table 2. Absolute Maximum Ratings

(i) Tested to TLP (10A)

(ii) Tested to JEDEC standard JESD22-A114

(iii) Tested to JEDEC standard JESD78

2.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max	Unit
Supply Voltage	V_{DD}	1.65V	3.7	V
Ambient Temperature Range	T_A	-40	85	℃

Table 3. Recommended Operating Conditions

2.3. Thermal Characteristics

Parameter	Symbol	Min.	Max	Unit
Thermal Resistance with DFN package - Junction to Ambient (iii)	θ_{JA}		39	℃/W
Thermal Resistance with WLCSP package - Junction to Ambient (iii)	θ_{JA}		65	℃/W

Table 4. Thermal Characteristics

(iii) θ_{JA} is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

2.4. Electrical Specifications

All values are valid within the recommended operating conditions unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Current consumption						
Mode = MANUAL	I_{pwd}	Converter stopped, pen detection off, SPI listening, OSC stopped		0.4	1	uA
Mode = PENDET	I_{pndt}	Converter stopped, pen detection activated, device generates interrupt upon detection, SPI listening, OSC stopped		0.4	1	uA
Mode =PENTRIG	I_{pntr}	Converter stopped, pen detection activated, device starts conversion upon pen detection. SPI listening, OSC stopped		0.4	1	uA
Mode=AUTO	I_{auto}	Converter stopped, pen detection off, SPI listening, OSC on, timer on		1.5		uA
Operation @8kSPS, VDD=1.8V	I_{opl}			23	50	uA
Operation @42kSPS, VDD=3.3V	I_{oph}			105	140	uA
Digital I/O						
High-level input voltage	V_{IH}		$0.8V_{DD}$		V_{DD}+0.2	V
Low-level input voltage	V_{IL}		V_{SS}-0.3		$0.2V_{DD}$	V
Hysteresis	V_{HysLow}	VDD > 2V		0.05 V_{DD}		V
	$V_{HysHigh}$	VDD < 2V		0.1 V_{DD}		V
Output Logic High	V_{OH}	I_{OH}>-2mA	$0.8V_{DD}$			
Output Logic Low	V_{OL}	I_{OL}<2mA	0		0.4	V
Input leakage current	L_I	CMOS input			±1	uA
High ESD Input - Output capacitance	$C_{X+/BR}$,$C_{X-/TL}$,$C_{Y+/TR}$, $C_{Y-/BL}$, C_{AUX}			50		pF
Input - Output capacitance	C_{NRST} , C_{NIRQ} ,C_{NCS} ,C_{DIN} , C_{DOUT}, C_{SCLK}			5		pF

Table 5. Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ	Max	Unit
Startup						
Power-up time	t_{por}	Time between rising edge VDD and rising NIRQ			1	ms
ADC						
Resolution	A_{res}		12			bits
Offset	A_{off}			±1		LSB
Gain error	A_{ge}	At full scale		0.5		LSB
Differential Non Linearity	A_{dnl}			±1		LSB
Integral Non Linearity	A_{inl}			±1.5		LSB
Resistors						
X+, X-, Y+, Y- resistance	R_{chn}	Touch Pad Biasing Resistance		5		Ohm
Pen detect resistance	R_{PNDT_00}	R_{PNDT} = 0		100		kOhm
	R_{PNDT_01}	R_{PNDT} = 1		200		kOhm
	R_{PNDT_10}	R_{PNDT} = 2		50		kOhm
	R_{PNDT_11}	R_{PNDT} = 3		25		kOhm
External components		**recommendations**				
Capacitor between VDD, GND	C_{vdd}	Type 0402, tolerance +/-50%		0.1		uF

Table 5. Electrical Specifications

2.5. Host Interface Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI TIMING SPECIFICATIONS (i)						
SCLK Clock Frequency Duty Cycle	 f_{SCLK} duty		 40		5000 60	 kHz %
NCS edge to first SCLK "↑"	T_{CSS}		50			
NCS edge to DOUT Low	T_{DCD}				100	
SCLK High Pulse Width	T_{CKH}		80			
SCLK Low Pulse Width	T_{CKL}		80			
Data Setup Time	T_{DS}		40			
Data Valid to SCLK Hold Time	T_{DH}		70			ns
Data Output Delay after SCLK "↓"	T_{DOD}				70	
NCS "↑" to SCLK Ignored	T_{CSI}		50			
NCS "↑" to DOUT Hi-Z state	T_{CCZ}				90	
NCS Hold Time	T_{CSW}		150			

(i) All timing specifications refer to voltage levels (50% VDD, V_{OH}, V_{OL}) defined in Table 6 unless otherwise mentioned.

Table 6. Host Interface Specifications

2.6. Host Interface Timing Waveforms

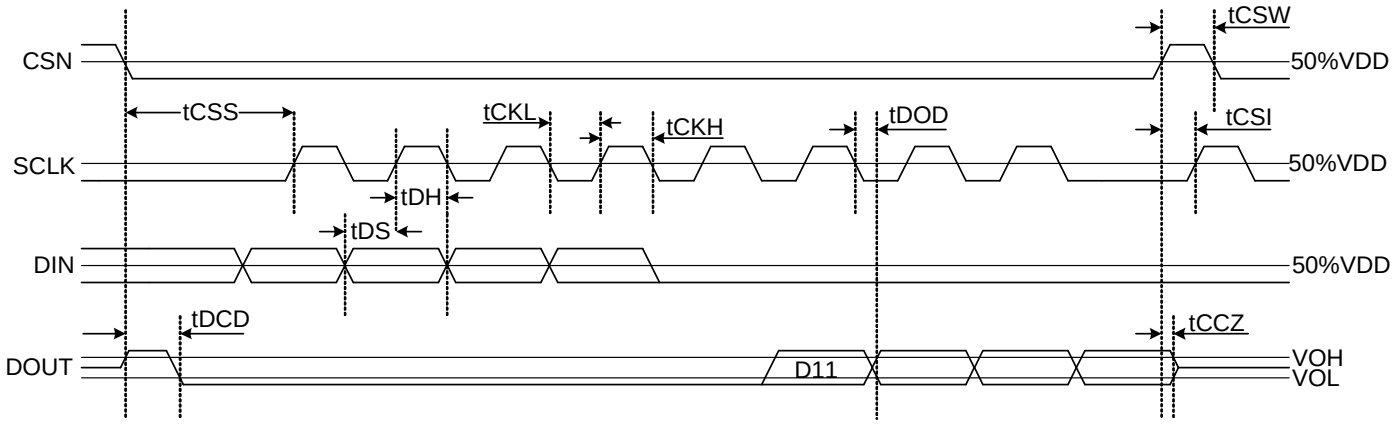


Figure 4. SPI Timing Waveform

3. Functional Description

3.1. General Introduction

This section provides an overview of the SX8652 architecture, device pinout and a typical application.

The SX8652 is designed for 4-wire and 5-wire resistive touch screen applications. The touch screen or touch panel is the resistive sensor and can be activated by either a finger or stylus. When the top layer is pressed, it makes contact with the bottom sheet and the touch location can be measured.

As shown in Figure 5 with a 4-wire panel, the touch screen coordinates and touch pressure are converted into SPI format by the SX8652 for transfer to the host. The auxiliary input can be used to convert with 12-bit resolution any analog input in the supply range. It can also serves as an external synchronisation input to trig the touchscreen acquisition as described in the Application Information section.

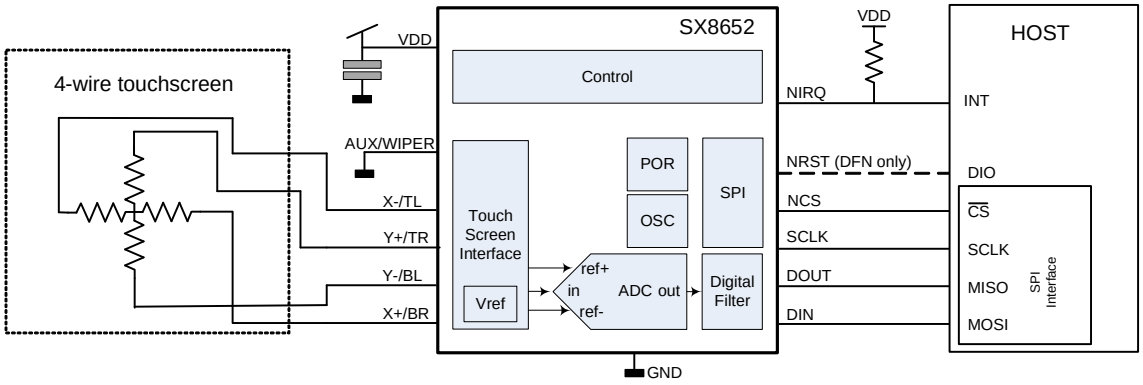


Figure 5. SX8652 with a 4-wire touch screen

A 5-wire touchscreen application is shown in Figure 6. The 5-wire top sheet acts as a voltage measuring probe. The measurement accuracy is not affected by damage on this sheet and consequently the reliability is improved but the touch pressure can not be calculated.

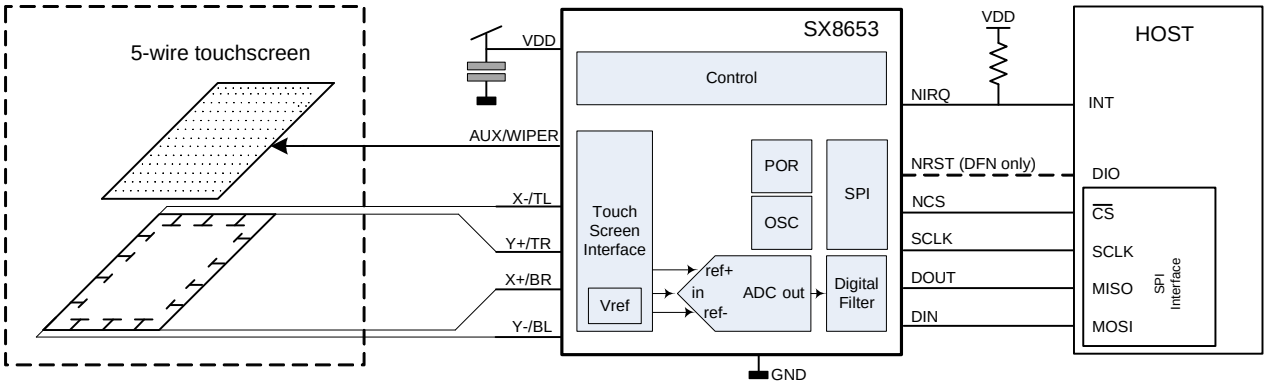


Figure 6. SX8652 with a 5-wire touch screen

3.2. Device Interface and ESD protection

The touch screen controller inputs have been specially designed to provide robust on-chip ESD protection of up to ±15kV in both HBM and Contact Discharge.

3.2.1. Touchscreen interface

The X+/BR, X-/TL, Y+/TR,Y-/BL, AUX/WIPER are the pins dedicated for the touchscreen interface. It provides the voltage sequence in order to obtain the coordinates and pressure measurement.

The five pins are connected to BR, TL, TR, BL, WIPER on a 5-wire touchscreen. They are the electrodes on the 4 corners of the bottom layer of the touchscreen plus the electrode on the top layer.

On a 4-wire touchscreen, only 4 electrodes are used: X+,X-,Y+,Y-. The AUX pin is not needed and therefore can be used to convert an analog signal (range GND - VDD) into 12-bit digital value. The touchscreen interface pins are the most exposed pins for an ESD event.

As shown in Figure 7, theses pins have internal ESD protection to GROUND and VDD.

3.2.2. Host Interface and Control Pins

The SX8652 is a slave device configured via the SPI interface.

NIRQ provides an interrupt to the host processor when a pen is detected or when channel data is available. The NIRQ pin is an active low, open drain output to facilitate interfacing to different supply voltages and thus requires an external pull-up resistor (1-10 kOhm).

The host can reset the chip via the SPI interface or with the dedicated pin NRST. The NRST pin is an active low input that provides a hardware reset. An internal pull-up enables the interfacing with devices at different supply voltage.

NRST and NIRQ pins are protected to GROUND.

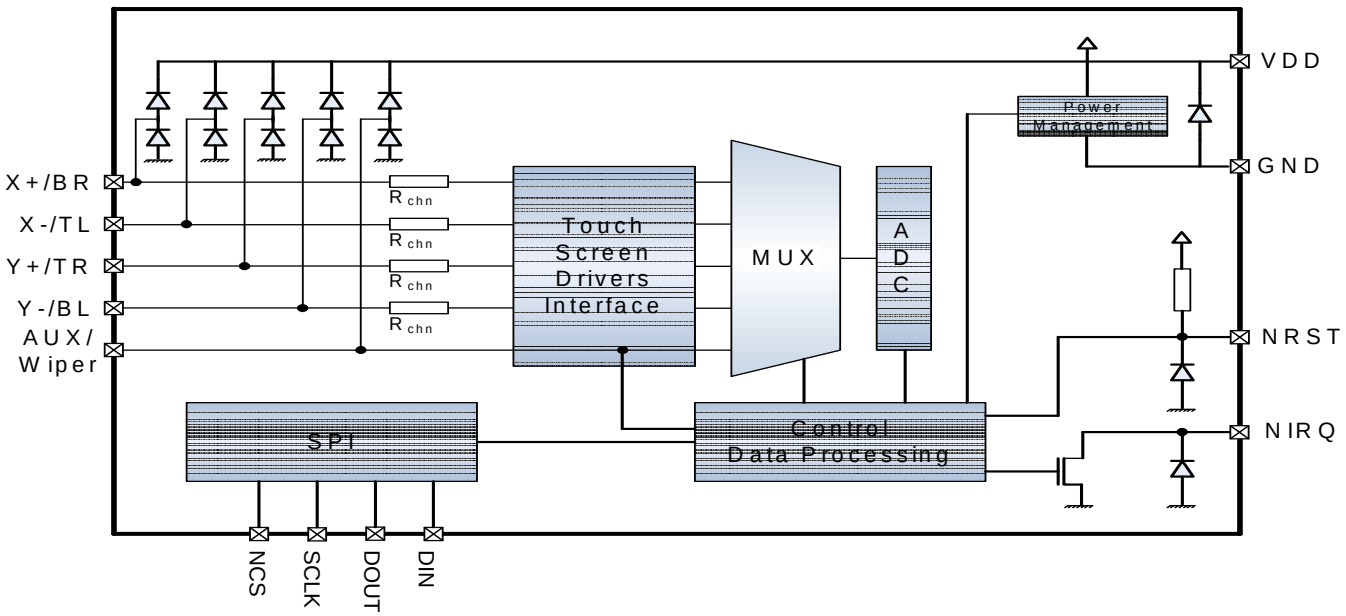


Figure 7. ESD protection

4. 4-wire Touch Screen Detailed Description

4.1. Touch Screen Operation

A 4-wire resistive touch screen consists of two resistive sheets separated by an insulator (Figure 4.2).

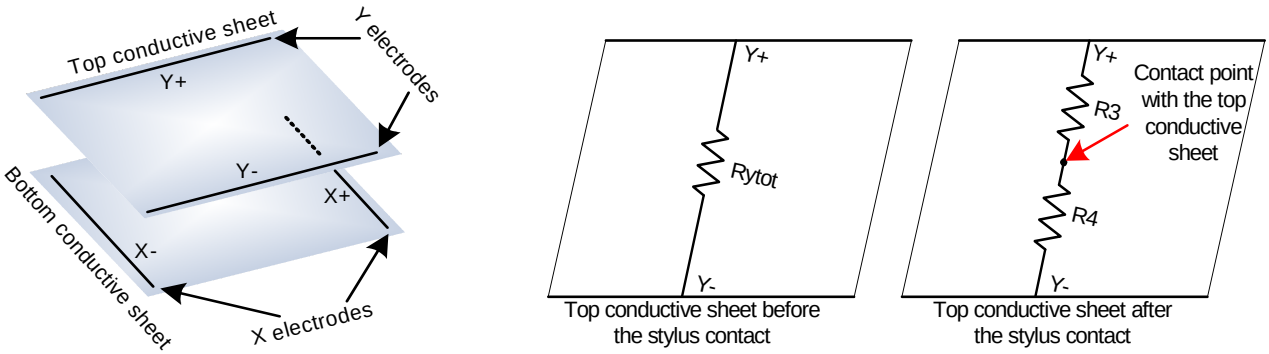


Figure 8. 4-wire Touch Screen

When a pressure is applied on the top sheet with a stylus for example, a connection with the lower sheet is made.

The contact point split the *Rxtot* bottom resistance in the vertical axis into two resistances *R1* and *R2*. In the same way, the Rytot resistance in the horizontal axis of the top sheet is divided into two resistances *R3* and *R4*.

$$Rxtot = R1 + R2$$
$$Rytot = R3 + R4$$

The touchscreen controller imposes a voltage level on X or Y electrodes allowing the detection of the contact position.

4.2. Coordinates Measurement

During the touch, the top and bottom touchscreen layers are connected. The resistance between the two sheets is R_T. A current coming from the reference voltage goes from X+ to X- to perform the X coordinate measurement. Figure 9 shows the measurement schematics.

Since the ADC had a high input impedance, no current flows through R_T and R3. The positive ADC input is biased with a voltage created by the R1, R2 voltage divider.

The conversion with the 12 bit ADC gives the X location.

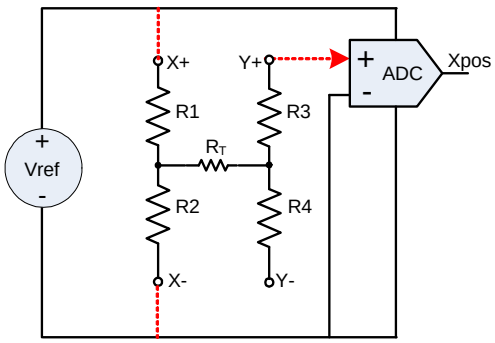


Figure 9. Abscissa (X) coordinates measurement

$$Xpos = 4095 \cdot \frac{R2}{R1 + R2}$$

The Y coordinate is measured in a similar fashion with the measurement setup given in Table 7.

$$Ypos = 4095 \cdot \frac{R4}{R3 + R4}$$

4.3. Pressure Measurement

The 4-wire touchscreen allows pressure measurement. The contact resistance between the two sheets are a function of the pressure applied on the top sheet. Indeed, the a low pressure applied with the finger will create a small contact area. With a greater pressure, the contact area will be bigger and the R_T resistance smaller.

The R_T contact resistance is therefore an indication of the applied pressure. R_T is deducted from Z1 and Z2 measurement. The measurement setup given in Table 7 allows to find Z1 and Z2.

$$z1 = 4095 \cdot \frac{R4}{R1 + R4 + R_T} \qquad z2 = 4095 \cdot \frac{R4 + Rt}{R1 + R4 + R_T}$$

Arranging Z1 and Z2 with Rxtot and Rytot allows the computation of R_T.

$$R_T = Rytot \cdot \frac{Ypos}{4095} \cdot \left[\frac{z2}{z1} - 1\right]$$

An alternative calculation method is using Xpos and Ypos.

$$R_T = \frac{Rytot \cdot Ypos}{4095} \cdot \left[\frac{4095}{z1} - 1\right] - Rxtot \cdot \left[1 - \frac{Xpos}{4095}\right]$$

Measurement	Vref +	Vref-	ADC +
X	X+	X-	Y+
Y	Y+	Y-	X+
Z1	X+	Y-	Y+
Z2	X+	Y-	X-

Table 7. Measurement setup

4.4. Pen Detection

The pen detection circuitry is used to detect a user action on the touchscreen. The contact between the two layers generates an interrupt or starts an acquisition sequence.

Doing a pen detection prior to conversion avoids feeding the host with dummy data and saves power.

If the touchscreen is powered between X+ and Y- through a resistor R_{PNDT}, no current will flow so long as pressure is not applied to the surface (see Figure 10).

When a pressure is applied, a current path is created and brings X+ to the level defined by the resistive divider determined by R_{PNDT} and the sum of R1, R_T and R4.

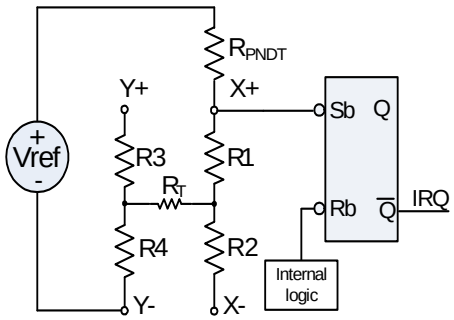


Figure 10. 4-wire pen detection circuitry

R_{PNDT} should be set to the greatest value of 200 kOhm for optimal detection (see Table 15). Increasing PowDly settings can also improve the detection on panel with high resistance.

The pen detection will set the PENIRQ bit of the RegStat register. The PENIRQ bit will be cleared and the NIRQ will be de-asserted as soon as the host reads the status register.

In PENDET mode, the pen detection will set NIRQ low.

5. 5-wire Touch Screen Detailed Description

5.1. Touch Screen Operation

As the 4-wire, the 5-wire resistive touch screen consists of two resistive sheets separated by an insulator (Figure 11). The main difference is that the 4 wires are connected on the 4 corners of the bottom conductive sheet. They are referred as Top Left, Top Right, Bottom Left, Bottom Right.

The fifth wire is embedded in the top sheet and is used for sensing the electrode voltage and is referred as the wiper.

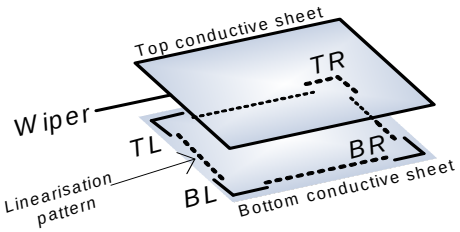


Figure 11. 5-wire touchscreen

5.2. Coordinates Measurement

When the electrodes TL is connected with BL and TR with BR, they form with the linearization pattern 2 electrodes bars which are very similar to the X electrodes in a 4-wire touchscreen. In the same way, the association of TL with TR and BL with BR create Y electrodes.

The four corners are therefore able to produce voltage gradients in the horizontal and vertical axis. The wiper is connected to the high input impedance of the ADC. When a pressure is applied on the top sheet, the contact point split the bottom sheet resistance into R1 and R2 on the X axis and R3 and R4 on the Y axis.

The X and Y position converted by the 12-bit ADC gives the following result.

$$Xpos = 4095 \cdot \frac{R2}{R1 + R2} \qquad Ypos = 4095 \cdot \frac{R4}{R3 + R4}$$

5.3. Pen Detection

The BR pin is connected to the positive pin of the reference voltage through R_{PNDT}. The wiper panel is grounded at the AUX/WIPER pin to provide the grounding path for a screen touch event.

The BR pin is monitored to detect voltage drop. When a pressure is applied on the top surface, a current path is created between the two layers and the PENIRQ bit of the RegStat register will be set. R_{PNDT} should be set to the greatest value of 200 kOhm for optimal detection (see Table 15). Increasing PowDly settings can also improve the detection on panel with high resistance.

In PENDET mode, the pen detection will set NIRQ low.

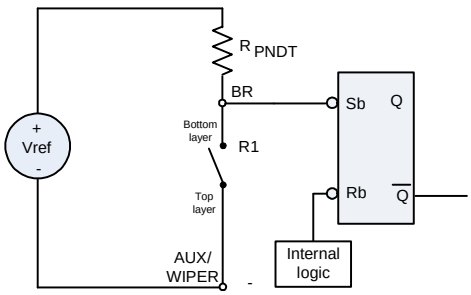


Figure 12. 5-wire pen detection circuitry

6. Data Processing

The SX8652 offers 4 types of data processing which allows the user to make trade-offs between data throughput, power consumption and noise rejection. The parameter FILT is used to select the filter order N_{filt} as seen in Table 8.

The *sn* samples from the ADC can be averaged. The processed *cn* 12-bit value is then send through the SPI bus.

The noise rejection will be improved with a high order to the detriment of the power consumption.

The K coefficient in Table 8 is a filter constant. Its value is K=4079/4095.

FILT	N_{filt}	Explanation	Processing
0	1	No average	$s_n = c_n$
1	3	3 ADC samples are averaged	$s_n = \frac{1}{3}K(c_n + c_{n-1} + c_{n-2})$
2	5	5 ADC samples are averaged	$s_n = \frac{1}{5}K(c_n + c_{n-1} + c_{n-2} + c_{n-3} + c_{n-4})$
3	7	7 ADC samples are sorted and the 3 center samples are averaged	$c_{max1} \geq c_{max2} \geq c_a \geq c_b \geq c_c \geq c_{min1} \geq c_{min2}$ $s_n = \frac{1}{3}K(c_a + c_b + c_c)$

Table 8. Filter order

7. Power-Up, Reset

During power-up, NIRQ pin is kept low, the POR reset all registers and states of the SX8652. The SX8652 is not accessible and SPI communications are ignored.

As soon as NIRQ rises, the SX8652 is in manual mode with only the SPI peripheral enabled to minimize power consumption.

The host can reset the SX8652 by setting the NRST pin low or via the SPI bus. Writing the code 0xDE to the register RegSoftReset reset the circuit.

When NRST is driven LOW by the host, NIRQ will be driven low by the SX8652. After the reset NIRQ will be released by the SX8652.

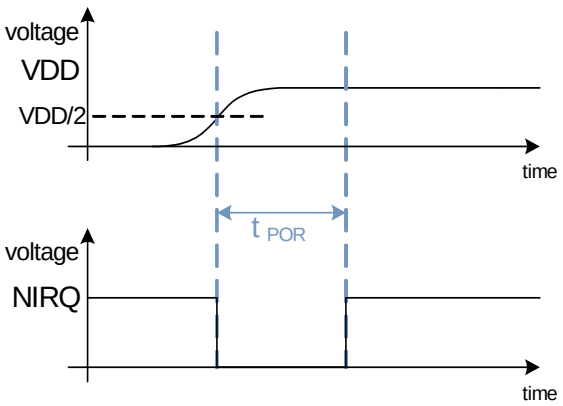


Figure 13. Power-up, NIRQ

8. Modes of Operation

The SX8652 has four operation modes that are configured using the SPI commands as defined in Table 13 and Table 15.

These 4 modes are:

- manual (command ‘MANAUTO’ and RATE=0),
- automatic (command ‘MANAUTO’ and RATE>0),
- pen detect (command ‘PENDET’),
- pen trigger mode (command ‘PENTRG’).

In the PENDET mode the pen detection is activated. The SX8652 will generate an interrupt (NIRQ) upon pen detection and set the PENIRQ bit in the SPI status register. To quit the PENDET mode the host needs to configure the manual mode.

In the PENTRG mode the pen detection is activated and a channel conversion will start after the detection of a pen. The SX8652 will generate an interrupt (NIRQ) upon pen detection and set the CONVIRQ bit in the SPI status register. To quit the PENTRIG mode the host needs to configure the manual mode. The PENTRG mode offers the best compromise between power consumption and coordinate throughput.

8.1. MANual Mode

In manual mode (RATE=0), the host sequences all the actions by the SPI commands described in Table 9.

When a command is received, the SX8652 executes the associated task and waits for the next command.

Command	Action
CONVERT(CHAN)	Select and bias a channel Wait for the programmed settling time (POWDLY) Start conversion
SELECT(CHAN)	Select and bias a channel

Table 9. CONVERT and SELECT command

The channel can be biased for an arbitrary amount of time by first sending a SELECT command and then a CONVERT command once the settling time requirement is met.

The SELECT command can be omitted if the large range of POWDLY settings cover the requirements. In the latter case, the CONVERT command alone is enough to perform an acquisition.

With CHAN=SEQ, multiple channels are sampled. This requires programming the POWDLY field in register RegCTRL0. The selected channel will be powered during POWDLY before a conversion is started. The channel bias is automatically removed after the conversion has completed.

8.2. AUTOmatic mode

In automatic mode (RATE > 0), SX8652 start the acquisition when a touch is detected. It converts all the channels selected with RegChnMsk and set NIRQ low when it is finished.

After the host has read the channels, if CONDIRQ=1 and the touch is detected again, the SX8652 starts a new conversion cycle.

To not loose data, the SX8652 does not begin conversion before the host read all the channels.

We can define the time *ts* between the start of the conversion and the end of the channels reading by the host.

The rate programmed is achieved if *ts*<1/RATE otherwise the new rate is 1/*ts*.

When the control CONDIRQ bit (see register RegStat Table 15) is set to ‘1’ then the interrupts will only be generated if the pen detect occurred. This result in a regular interrupt stream, as long as the host performs the read channel commands, and the screen is touched. When the screen is not touched, interrupts does not occur.

If the control CONDIRQ bit is cleared to ‘0’, the interrupts will be always generated. In case there is no pen detected on the screen then the coordinate data will be qualified as invalid, see section [9.5]. This result in a regular interrupt stream as long as the host performs the read channel commands,

This working is illustrated in Figure 16.

Figure 14 shows the SPI working in automatic mode with CONDIRQ=1. After the first sentence send through the SPI to make the initialization, traffic is reduced as only reads are required.

The processing time is the necessary time for the SX8652 to makes the pen detection, the settling time (POWDLY) and the conversion of the selected channels. This time increases with the number of channel selected and the filter used. NIRQ interrupt signal notifies the host when the conversions are done.

The host just need to read the channels data to release the interrupt.

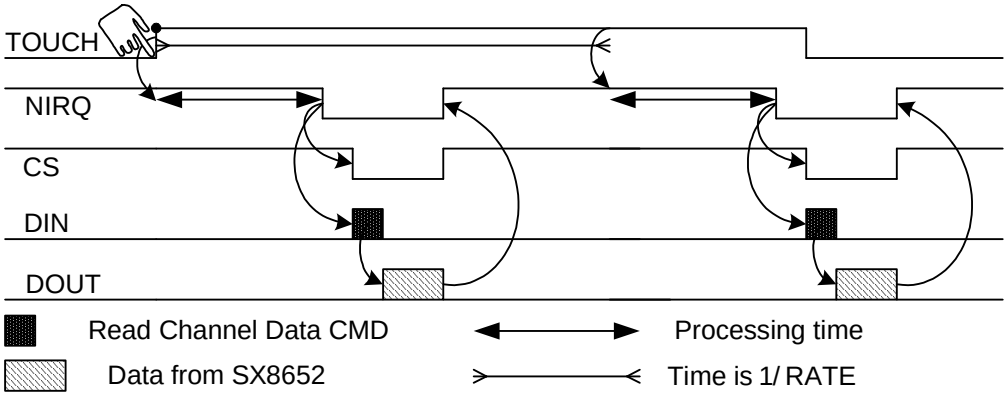


Figure 14. SPI working in AUTO mode

8.3. PENDET Mode

The PENDET mode can be used if the host only needs to know if the screen has been touched or not and take from that information further actions. When pen detect circuitry is triggered the interrupt signal NIRQ will be generated and the status register bit 'PENIRQ' will be set. The bit is cleared by reading the status register RegStat. The PENDET working is illustrated in Figure 16.

8.4. PENTRIG Mode

The PENTRIG mode offers the best compromise between power consumption and coordinate throughput.

In this mode the SX8652 will wait until a pen is detected on the screen and then starts the coordinate conversions. The host will be signaled only when the screen is touched and coordinates are available. The flowchart is describes in Figure 16.

The coordinate rate in pen trigger mode is determined by the speed of the host reading the channels and the conversion times of the channels. The host performs the minimum number of SPI commands in this mode.

The host has to wait for the NIRQ interrupt to make the acquisition of the data.

The SPI working is illustrated in Figure 15.

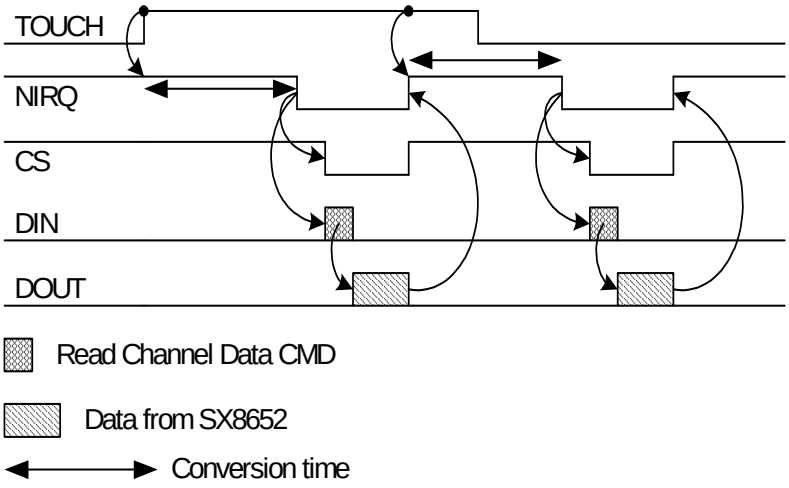


Figure 15. SPI working in PENTRIG mode

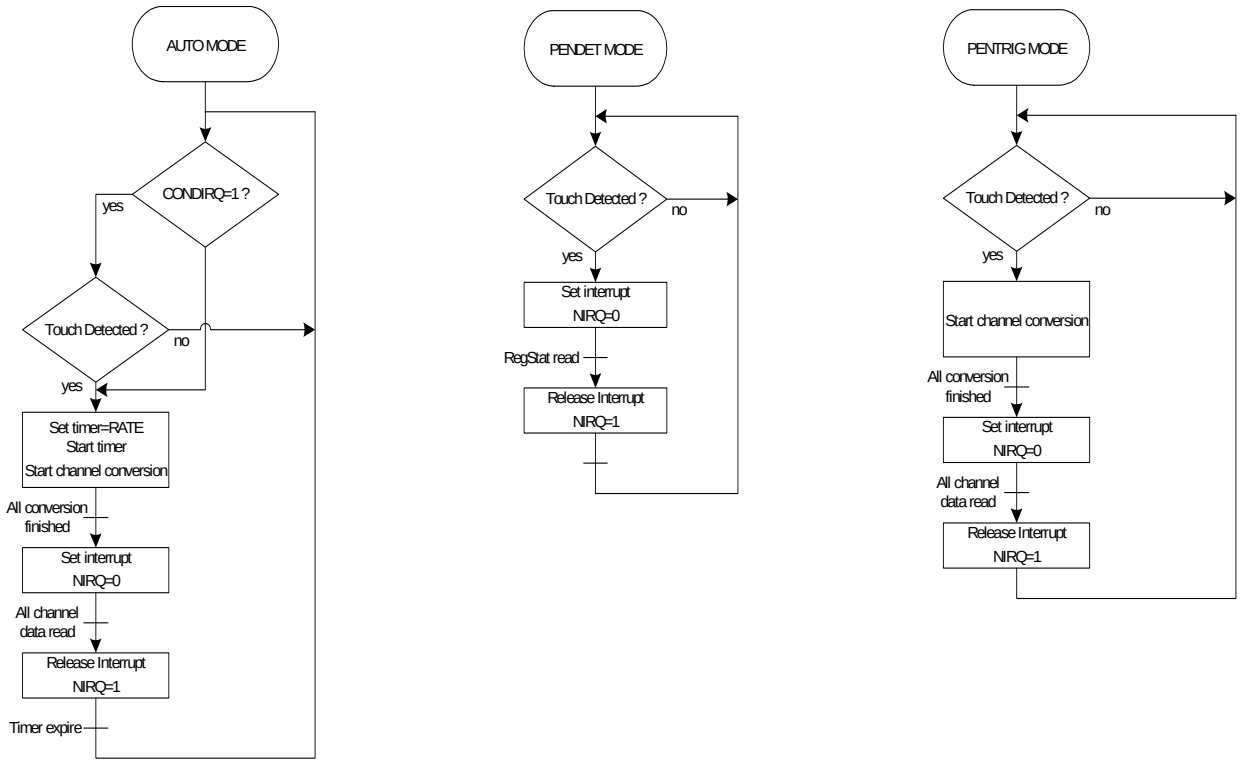


Figure 16. AUTO, PENDET and PENTRIG Mode Flowchart

9. Host Interface

The host interfaced is composed of a SPI bus. It performs the read/ write operations on the registers and channels data.

9.1. SPI Read/Write Registers

The WRITE command allows the host to write a single or multiple registers in the SX8652. The host can read single or multiple registers from the SX8652 by the READ command. This is defined in Table 10.

W/R command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
WRITE(RA)	0	0	0	RA(4:0)					Write register (see Table 14 for RA)
READ(RA)	0	1	0	RA(4:0)					Read register (see Table 14 for RA)

Table 10. W/R commands

9.2. SPI Reading Channel Data

Five channels can be sampled by the SX8652: X, Y, Z1, Z2 and AUX. They are defined in Table 12. They can be converted in sequence with the RegChanMsk register.

The READCHAN command allows the host to read the data obtained after the channels conversion and processing.

W/R command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
READCHAN	0	0	1	x	x	x	x	x	Read data from channel

Table 11. Read Channels Data

Channel	CHAN(2:0)			Function
	2	1	0	
X	0	0	0	X channel
Y	0	0	1	Y channel
Z1	0	1	0	First channel for pressure measurement
Z2	0	1	1	Second channel for pressure measurement
AUX	1	0	0	Auxiliary channel
reserved	1	0	1	
reserved	1	1	0	
SEQ	1	1	1	Channel sequentially selected from RegChanMsk register, (see Table 15)

Table 12. Channel definition

The channel data are 12-bit of unsigned format which corresponds to integers between 0 and 4095. This is send on two bytes, MSB first then LSB. A mask with the value 0x0FFF (4095) must be done to filter the four first unknown bit.

When a channel data has been transmitted, the next one is sent in the successive order: X,Y, Z1, Z2 and AUX. If a channel has not been converted, the data is not transmitted.

When the channel data buffer gets empty, the data will carry an invalid data as explained in the channel data format.

Remark: After a conversion sequence, it is possible to read only one time the same channel.

Example: the SX8652 is set to convert X and Y. The value 0xC0 is set in RegChanMsk. The first byte read after the READCHAN command will be X(MSB), then X(LSB), Y(MSB) and at the end Y(LSB). If the host carry on the reading, it will get invalid data.

9.3. SPI Host Commands

.The host can issue commands to change the operation mode or perform manual actions as defined in Table 13.

command name	CR(7:0)								Function
	7	6	5	4	3	2	1	0	
SELECT(CHAN)	1	0	0	0	x	CHAN(2:0)			Bias channel (see Table 12 for CHAN)
CONVERT(CHAN)	1	0	0	1	x	CHAN(2:0)			Bias channel (see Table 12 for CHAN)
MANAUTO	1	0	1	1	x	x	x	x	Enter manual or automatic mode.
PENDET	1	1	0	0	x	x	x	x	Enter pen detect mode.
PENTRG	1	1	1	0	x	x	x	x	Enter pen trigger mode.

Table 13. Host Commands

9.4. SPI implementation and multiple Read/Write

The SPI implemented on the SX8652 is set to the common setting CPOL=0 and CPHA=0 which means data are sampled on the rising edge of the clock, and shifted on the falling one.

The default state of the clock when NCS gets asserted is low. If a host send a command while the system is busy, the command is discarded.

The SPI protocol is designed to be able to do multiple read/write during a transaction. During one single operation, as long as NCS stay asserted, the register address is automatically increased to allow sequential read/write (or sequential retrieval of data). Between each different operation though (READ/WRITE/READCHAN), the communication should be restarted.

This is described in Figure 17.

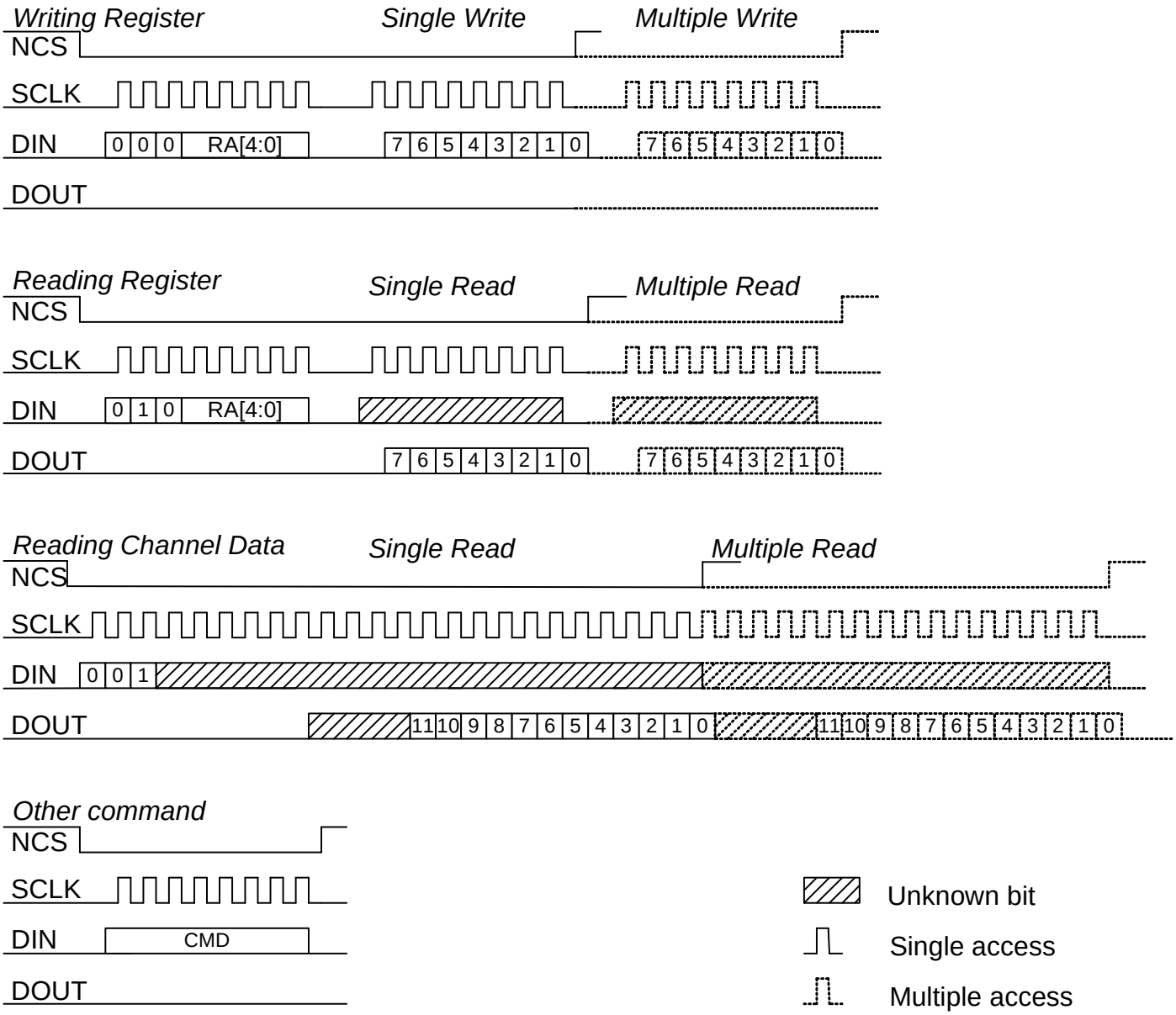


Figure 17. Data channel format

9.5. Invalid Qualified Data

The SX8652 returns 0xFFFF data in case of invalid qualified data.

This occurs:

- When the SX8652 has read all the channel data in the FIFO
- When a conversion is done without a pen being detected.

9.6. Register Map

Register Address RA(4:0)	Register	Description
0 0000	RegCtrl0	Write, Read
0 0001	RegCtrl1	Write, Read
0 0010	RegCtrl2	Write, Read
0 0100	RegChanMsk	Write, Read
0 0101	RegStat	Read
1 1111	RegSoftReset	Write

Table 14. Register address

The details of the registers are described in the next sections.

9.7. SX8652 register

Register	Bit	Default	Description		
RegCtrl0	7:4	0000	RATE	Set rate in coordinates per sec (cps) (± 20%) If RATE =0: Manual mode. if RATE >0: Automatic mode	
				0000: Timer disabled -Manual mode 0001: 10 cps 0010: 20 cps 0011: 40 cps 0100: 60 cps 0101: 80 cps 0110: 100 cps 0111: 200 cps	1000: 300 cps 1001: 400 cps 1010: 500 cps 1011: 1k cps 1100: 2k cps 1101: 3k cps 1110: 4k cps 1111: 5k cps
	3:0	0000	POWDLY	Conversion (or first conversion when filtering is enabled) settling time (± 10%)	
				0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms
RegCtrl1	7:6	00	AUXAQC	00: AUX is used as an analog input (4-wire only) 01: On rising AUX edge, wait POWDLY and start acquisition	10: On falling AUX edge, wait POWDLY and start acquisition 11: On rising and falling AUX edges, wait POWDLY and start acquisition
				The AUX trigger works only in manual mode with 4-wire touchscreen	
	5	1	CONDIRQ	Enable conditional interrupts 0: interrupt always generated at end of conversion cycle. If no pen is detected the data is set to 'invalid qualified'.	1: interrupt generated when pen detect is successful
	4	0	SCREEN	Select the type of screen: 0: 4-wire	1: 5 -wire
	3:2	00	RPDNT	Select the Pen Detect Resistor 00: 100 kOhm 01: 200 kOhm	10: 50 kOhm 11: 25 kOhm
	1:0	00	FILT	Digital filter control 00: Disable 01: 3 sample averaging	10: 5 sample averaging 11: 7 sample acquisition, sort, average 3 middle samples
RegCtrl2	7:4	0	reserved		
	3:0	0000	SETDLY	Settling time while filtering (± 10%) 0000: Immediate (0.5 us) 0001: 1.1 us 0010: 2.2 us 0011: 4.4 us 0100: 8.9 us 0101: 17.8 us 0110: 35.5 us 0111: 71.0 us	1000: 0.14 ms 1001: 0.28 ms 1010: 0.57 ms 1011: 1.14 ms 1100: 2.27 ms 1101: 4.55 ms 1110: 9.09 ms 1111: 18.19 ms

Table 15. SX8652 Register

Register	Bit	Default	Description		
RegChanMsk	7	1	XCONV	0: no sample	1: Sample X channel
	6	1	YCONV	0: no sample	1: Sample Y channel
	5	0	Z1CONV	0: no sample	1: Sample Z1 channel
	4	0	Z2CONV	0: no sample	1: Sample Z2 channel
	3	0	AUXCONV	0: no sample	1: Sample AUX channel
	0	0	reserved		
	0	0	reserved		
	0	0	reserved		
RegStat	Host writing to this register is ignored.				
	7	0	CONVIRQ	0: no IRQ pending 1: Conversion sequence finished IRQ is cleared by the channel data read command	
	6	0	PENIRQ	Operational in pen detect mode 0: no IRQ pending 1: Pen detected IRQ pending IRQ is cleared by the RegStat reading	
	5	1	RSTEVENT	A reset event has occurred	
	4:0	00000	reserved		
RegSoftReset	7:0	0x00	Writing 0xDE to this register reset the SX8652 Any other data will not affect the SX8652		

Table 15. SX8652 Register

10. Application Information

This section describes in more detail application oriented data.

10.1. Acquisition Setup

Prior to an acquisition, the SX8652 can be setup by writing the control registers. Registers are written by issuing the register write command. They can be read by issuing the read command. Please refer to the section [9.7].

10.2. Channel Selection

The SX8652 can be setup to start a single channel conversion or to convert several channels in sequence. For a single conversion, the channel to be converted is determined from the CHAN(2:0) field in the command word (defined in Table 12).

Several channels defined in RegChanMsk can be acquired sequentially by setting the CHAN(2:0) field to SEQ. The channels will be sampled in the order X, Y, Z1, Z2, AUX.

10.3. Noise Reduction

A noisy environment can decrease the performance of the controller. For example, an LCD display located just under the touch screen can adds a lot of noise on the high impedance A/D converter inputs.

10.3.1. POWDLY

In order to perform correct coordinates acquisition properly, some time must be given for the touch screen to reach a proper level. It is a function of the PCB trace resistance connecting the SX8652 to the touchscreen and also the

capacitance of the touchscreen. We can define tau as the RC time constant. POWDLY duration should be programmed to 10 tau to reach 12 bit accuracy.

Adding a capacitor from the touch screen drivers to ground is a solution to minimize external noise but it increases settling time and consequently the power consumption.

10.3.2. SETDLY

A best method to filter noise is described in section [6] (Data processing). When filtering is enabled, the channel will be biased initially during a time of POWDLY for the first conversion. The parameter SETDLY sets the settling time between the subsequent conversions in a filter set. In most applications, SETDLY can be set to 0. In applications with a high tau and where accuracy of 1LSB is required SETDLY should be increased.

10.4. AUX Input - 4-wire touchscreen only

The AUX input can be used to sample an analog signal in the range 0-VDD. For system supply by battery, the battery voltage can be monitored for example. The conversion is done in sequence with the touchscreen acquisition therefore the sample rate is defined with RegCtrl0 in AUTO mode.

The AUX pin can also triggered conversions. A rising edge, a falling edge or both applied on the AUX pin can trigger the conversion. This is defined by AUXACQ in RegCtrl1.

This method can be used to sample touchscreen when there is noise-free periods.

10.5. Interrupt Generation

An interrupt (NIRQ=0) will be generated:

- During the power-up phase or after a reset
- After completion of a conversion in MANUAL, PENTRIG or AUTO mode. CONVIRQ (bit [7] of RegStat) will be set at the same time.
- After a touch on the panel being detected in PENDET mode. PENIRQ (bit [6] of RegStat) will be set at the same time.

The NIRQ will be released and pulled high(NIRQ=1) by the external pull-up resistor:

- When the power-up phase is finished
- When the host read all channels data that were previously converted by the SX8652 in MANUAL, PENTRIG or AUTO mode. CONVIRQ will be cleared at the same time.
- When the host read the status register in PENDET mode. PENIRQ, will be cleared at the same time.

An active NIRQ (low) needs to be cleared before any new conversions will occur.

10.6. Coordinate Throughput Rate

The coordinate throughput rate depends on the following factors:

- The SPI communication time: T_{com}
- The conversion time: T_{conv}

The coordinate rate is the frequency to get the X, Y, Z1 and Z2 coordinate: $CoordRate = \frac{1}{T_{com} + T_{conv}}$

10.6.1. SPI Communication Time

The minimum time to read the channel data in PENTRIG mode is: $T_{com} = (8 + 16 \times N_{chan}) \times T_{SPI}$

The highest throughput will be obtained with a SPI frequency of 5MHz when the host read the channel data as quickly as possible after the NIRQ falling edge.

10.6.2. Conversion Time

The maximum possible throughput can be estimated with the following equation

$$T_{conv} = 47 \cdot T_{osc} + N_{chan}[POWDLY + SETDLY(N_{filt} - 1) + T_{osc}(21N_{filt} + 1)]$$

with:

- N_{filt} = {1,3,5,7} based on the order defined for the filter FILT (see Figure 8).
- N_{chan} = {1,2,3,4,5} based on the number of channels defined in RegChanMsk
- POWDLY = 0.5us to 18.19ms, settling time as defined in RegCtrl0
- SETDLY = 0.5us to 18.19ms, settling time when filtering as defined in RegCtrl2
- Tosc is the oscillator period (555ns +/- 15%)

Table 16 gives some examples of Coordinate Rate and Sample Rate for various setting in PENTRIG mode.

Nch [1..5]	Nfilt [1 3 5 7]	PowDly [uS]	SetDly [uS]	Tconv [uS]	Tcomm [uS]	CoordRate [kSPS]
2	1	0.5	-	51	8	16.7
2	3	71	0.5	190	8	5.0
4	3	140	0.5	740	14	1.3

Table 16. Coordinate throughput examples

10.7. ESD event

In case of ESD event, the chip may reset to protect its internal circuitry. The bit *RSTEVENT* indicates that a reset event has occurs.

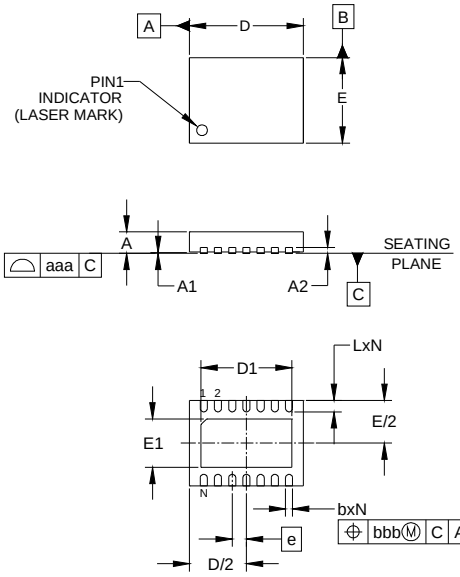
ESD event may trig the pen detection circuitry. In this case wrong data will be send to the host. To detect this false coordinates on 4-wire touchscreen, Z1 and Z2 can be read. The conditions Z1<LowThreshold and Z2>HighThreshold indicate an ESD event. The values LowThreshold and HighThreshold are given for indication only on the table below and should be fine tune according to the system.

LowThreshold	HighThreshold
10	4070

Table 17. Threshold to detect false coordinates

11. Packaging Information

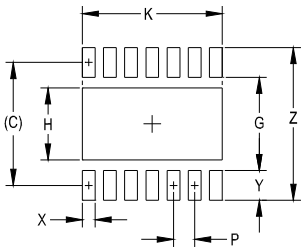
11.1. DFN Package



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	-	0.80
A1	0.00	0.02	0.05
A2	-	(0.20)	-
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D1	3.05	3.20	3.30
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e	0.50 BSC		
L	0.30	0.40	0.50
N	14		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 18. DFN Package Outline Drawing

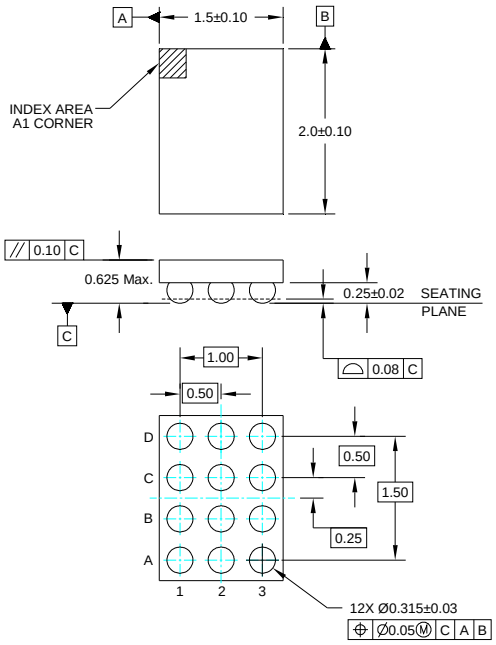


DIMENSIONS	
DIM	MILLIMETERS
C	(2.90)
G	2.20
H	1.70
K	3.30
P	0.50
X	0.30
Y	0.70
Z	3.60

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

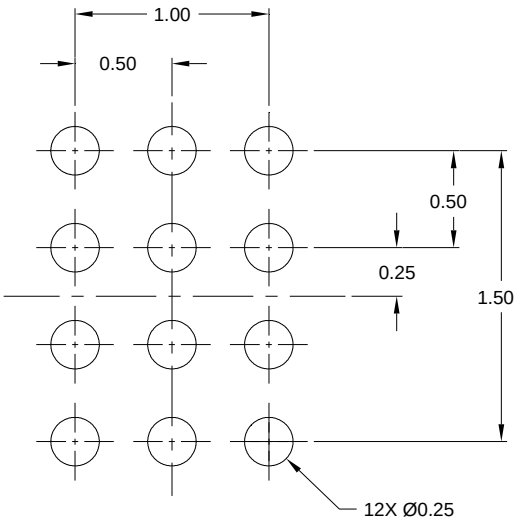
Figure 19. DFN Package Land Pattern

11.2. WLCSP Package



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

Figure 20. WLCSP Package Outline Drawing



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Figure 21. WLCSP Land Pattern of WLCSP

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