Document Number SAC57D54H
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SAC57D54H

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Features

- ARM™ Cortex-A5, 32-bit CPU
  - Supports ARMv7- ISA
  - 32 KB Instruction cache, 32 KB Data cache
  - NEON SIMD Media Processing Engine
  - FPU supporting double precision floating point operations
  - Memory Management Unit
  - GIC Interrupt Controller
  - Up to 320 MHz
- ARM™ Cortex-M4, 32-bit CPU
  - Supports ARMv7 - ISA
  - 16 KB Instruction cache, 16 KB Data cache
  - 64 KB Tightly-Coupled Memory (TCM)
  - Single Precision FPU
  - NVIC Interrupts Controller
  - 1.25 DMIPS per MHz integer performance
  - Up to 160 MHz
- I/O Processor
  - ARM™ Cortex-M0+, 32-bit CPU
  - Intelligent Stepper Motor Drive
- Memory subsystem
  - System Memory Protection Unit
  - 4 MB on-chip flash supported with the flash controller
  - 1 MB on-chip SRAM with ECC
  - 1.3 MB on-chip Graphics SRAM with FlexECC
- Supports wake-up from low power modes via the WKPU controller
- On-chip voltage regulator
  - External 3.3 V input supply
  - Option for direct, external supply of core voltage
  - Low Voltage Detect (LVD) and High Voltage Detect (HVD) on various supplies and regulators
- Debug functionality
  - Run-time debug control of cores and visibility of system resources using the Debug Access Port (DAP)
  - IEEE 1149.1/ IEEE 1149.7 System JTAG Controller (SJTAG)
  - Program and Data Trace support (16-bit data width) implemented by the ARM Trace Port Interface Unit (TPIU) Trace capture
- Timer
  - Four 8-channel Flextimer modules (FTM)
  - Two 4 channel System Timer Module (STM)
  - Three Software WatchDog Timers (SWT)
  - One 8 channel Periodic Interrupt Timer (PIT)
  - Autonomous Real Time Counter (RTC)
- Analog
  - 1 x 24 channel, 12-bit analog-to-digital converter (ADC)
  - 2 analog comparators (CMP)
- Security
  - Cryptographic Services Engine (CSE)
- Safety
  - ISO26262 ASIL-B compliance
  - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Multiple operating modes
  - Includes enhanced low power operation
- Memory interfaces
  - 2 x Dual QuadSPI Serial flash controllers
  - Supports SDR and DDR serial flash
  - Support for 3.3 V Hyperflash (Spansion)
  - DRAM controller supporting SDR and DDR2
- Clock interfaces
  - 8-40 MHz external crystal (FXOSC)
  - 16 MHz IRC (FIRC)
  - 128 kHz IRC (SIRC)
  - 32 kHz external crystal (SXOSC)
  - Clock Monitor Unit (CMU)
  - Frequency modulated phase-locked loop (FMPLL)
  - Real Time Counter (RTC)

- Graphics interfaces
  - Vivante GC355 GPU supporting OpenVG 1.1
  - 2 x 2D-ACE Display Controllers (with inline Head-Up-Display warping)
  - Digital RGB, TCON_0 (RSDS), TCON_1 and OpenLDI/LVDS output options
  - Digital Video Input (VIU4)
  - RLE Decoder for memory-memory decompression
  - 40x4 segment LCD driver, reconfigurable as 38x6 or 36x8
- Cluster peripherals
  - Sound Generator Module (SGM)
  - 6 Stepper Motor Drivers with Stepper Stall Detect
- Communication
  - Ethernet 10/100 + AVB (ENET)
  - MLB50
  - FlexCAN x 3
  - DSPI x 5
  - LINFlexD x 3 (1 x Master/Slave, 2 x Master only)
  - I2C x 2
- eDMA controller with multiple transfer request sources using DMAMUX
- Boot Assist Flash (BAF) supports internal flash programming

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1 Block diagram

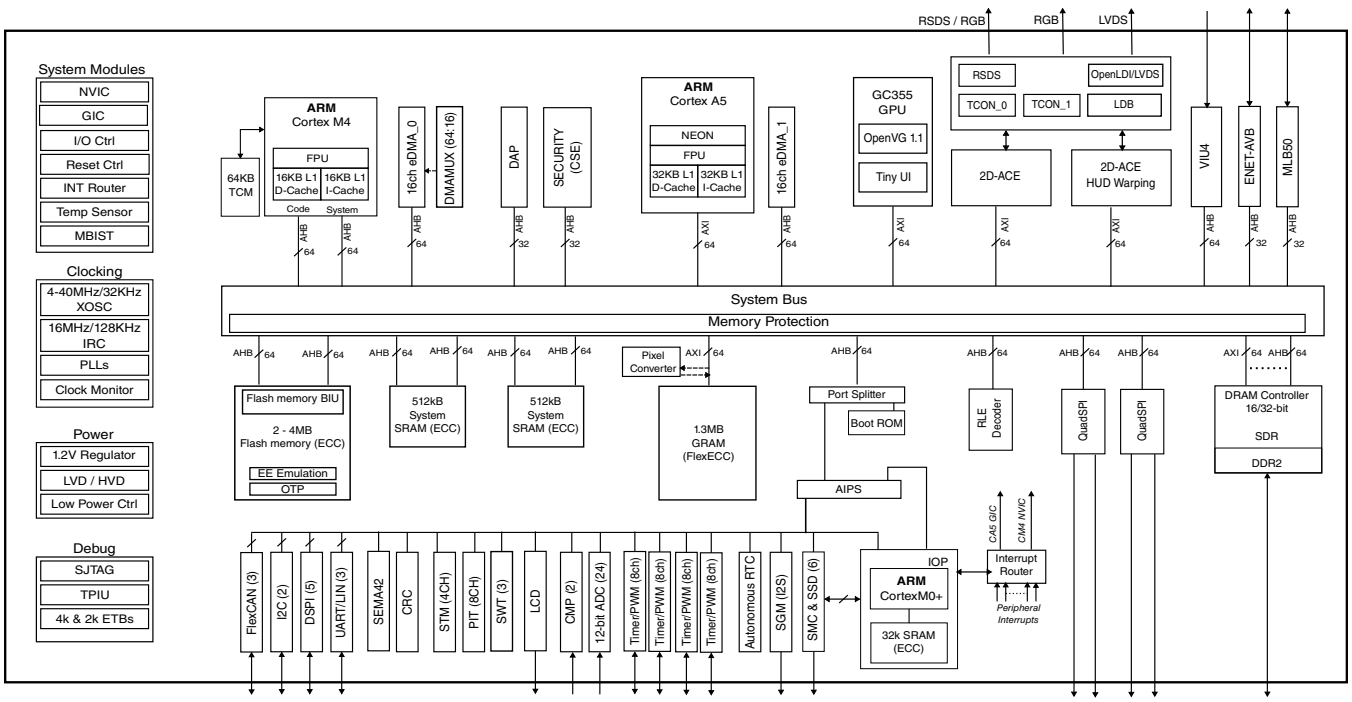


Figure 1. High level block diagram

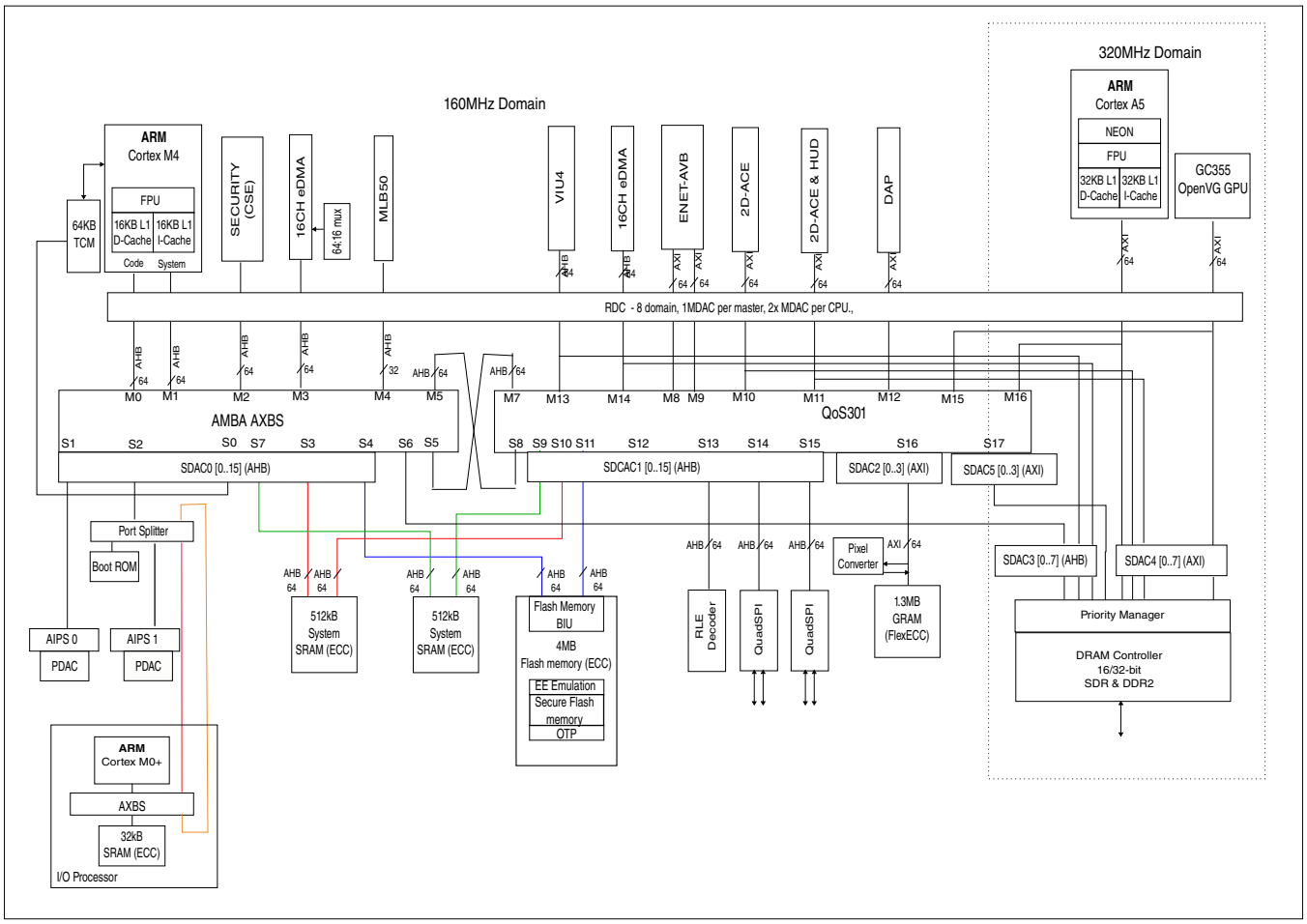


Figure 2. Detailed block diagram

2 Family comparison

The table below provides a summary of the different members of the SAC57D5xx Low/ Mid-Line Instrument Cluster family and their features. Note that not all features are available simultaneously on all packages.

Table 1. Feature sets

Product Features		SAC57D54H	SAC57D53M	SAC57D52L
Cores	Cortex-A5 (320 MHz, 32 KB/32 KB L1 Caches, FPU, MMU, NEON)	Yes	Yes	Yes
	Cortex-M4 (160 MHz, 16 KB/16 KB L1 Caches, FPU)	Yes	Yes	Yes

Table continues on the next page...

Table 1. Feature sets (continued)

Product Features		SAC57D54H	SAC57D53M	SAC57D52L
	Cortex - M0+ I/O Processor (IOP) (80 MHz)	Yes	Yes	Yes
Internal Memory	ECC Flash Memory	4 MB	3 MB	2 MB
	Graphics SRAM[1]	1.3 MB	1.3 MB	1.3 MB
	System SRAM (ECC)	2 x 512 KB	2 x 512 KB	2 x 512 KB
	IOP local SRAM (ECC)	32 KB	32 KB	32 KB
External Memory Interfaces	Dual DDR QuadSPI	2 x Dual DDR QuadSPI	2 x Dual DDR QuadSPI	2 x Dual DDR QuadSPI
	16 bit SDR DRAM (160MHz)	Yes	Yes	Yes
	32-Bit DDR2 DRAM (320MHz)[2]	Yes	Yes	-
System and General Purpose	Memory / Peripheral Protection (xDRC - Extended Resource Domain Controller)	Yes	Yes	Yes
	Security (CSE)	Yes	Yes	Yes
	eDMA	16ch x 2	16ch x 2	16ch x 2
Graphics/Video/Display/ Audio	2D-ACE	x2	x2	x2
	HUD Warping Engine	Yes	Yes	Yes
	TCON_0/RSDS	Yes	Yes	Yes
	TCON_1	Yes	Yes	Yes
	OpenLDI/LVDS	Yes	Yes	-
	GPU	GC355 : OpenVG 1.1 / TinyUI	GC355 : OpenVG 1.1 / TinyUI	GC355 : OpenVG 1.1 / TinyUI
	Video Input Unit	Yes	Yes	Yes
	Sound Generator	Yes	Yes	Yes
	Segment LCD	Yes	Yes	Yes
System Connectivity	FlexCAN	x3	x3	x3
	I2C	x2	x2	x2
	LINFlexD	x3	x3	x3
	SPI	x5	x5	x5
	MLB50	Yes	Yes	Yes
	10/100 Ethernet + AVB	Yes	Yes	Yes
Analog Connectivity	SMC/SSD	x6	x6	x6
	12 Bit ADC	Yes	Yes	Yes
	Analog Comparator	2 x 8ch	2 x 8ch	2 x 8ch
Timer/PWM	PIT	8ch	8ch	8ch
	SWT	3	3	3
	ARTC	Yes	Yes	Yes
	FlexTimer	4 x 8ch	4 x 8ch	4 x 8ch
Package Options	LQFP	208 LQFP	208 LQFP	208 LQFP

Table continues on the next page...

Table 1. Feature sets (continued)

Product Features		SAC57D54H	SAC57D53M	SAC57D52L
	BGA	516 MAPBGA	516 MAPBGA	-

1. GRAM can be reconfigured as ECC RAM
2. DDR2 interface only available in BGA package option

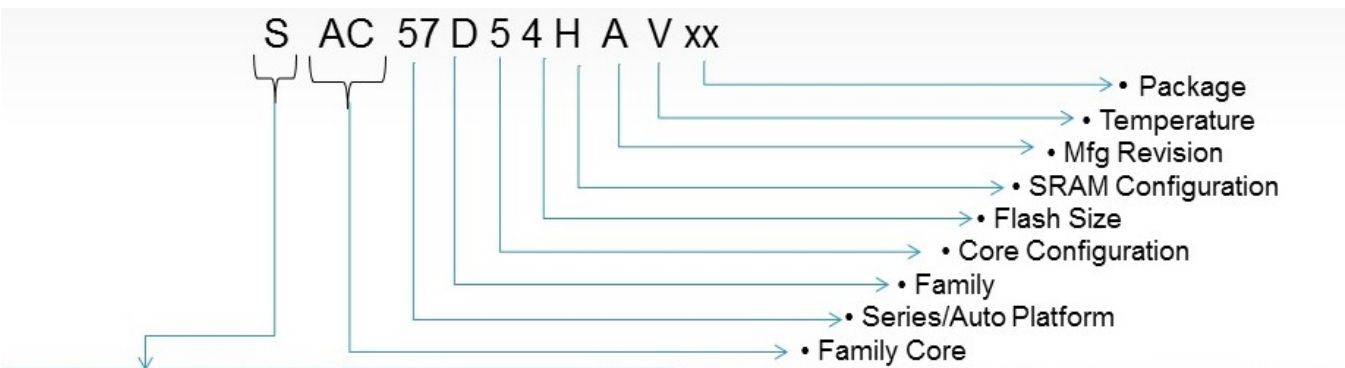
3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: SAC57D5xx.

3.2 Ordering information



Qualification Level	M
Prototype	P
Qualified	M
Auto Qualified	S
Family Core	**AC**
ARM Core	AC
Auto Platform	**57**
55nm FG	57

Family	D
Driver Information	D
Core Configuration	**5**
A5, M4, M0+	5
M4, M0+	4
Feature: Flash Size	**4**
4M Flash	4
3M Flash	3
2M Flash	2
1M Flash	1

Feature: SRAM Config	H
High	H
Mid	M
Low	L
Mfg Revision	**A**
TSMC14/Rev0	A
Temperature	**V**
Auto -40°C to 105°C	V

Package	xx
516MAPBGA Pb-free	MO
208LQFP Pb-free	LT

Packaging	
Tray	
T&R	R

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 2. Absolute maximum ratings

Symbol [1]	Parameter	Conditions	Min	Max	Unit
V_{DDE_A}, V_{DDE_B}, V_{DDE_SDR}	Input/output supply voltage[2]	—	–0.3	3.6	V
$V_{DD\_LP\_DEC}$	Decoupling pin for low power regulators[3]	—	–0.32	1.32	V
V_{DDA}	ADC supply voltage	—	–0.3	6.0	V
V_{DDEH_ADC}	ADC I/O supply voltage	—	–0.3	6.0	V
V_{SSA}	ADC supply ground	—	–0.3	0.3	V
V_{DDA_REF}[4]	ADC supply voltage	—	–0.3	6.0	V
V_{DDM_SMD}	SMD supply voltage	—	–0.3	6.0	V
V_{SSM_SMD}	SMD supply ground	—	–0.3	0.3	V
V_{DDE_DDR}[5]	DDR2 DRAM supply voltage	—	–0.3	2.3	V
DDR_VREF	DDR I/O Reference Voltage	—	–0.3	1.15	V
V_{DD12}	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on ADC analog pin with respect to V_{SSA}	Relative to V_{DDE_A}, V_{DDE_B}, V_{DDE_SDR}	–0.3	V_{DDE_ADC} + 0.3	V
	Voltage on Analog comparator pin (CMP) with respect to V_{SS}		–0.3	V_{DDE_A} + 0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS})	Relative to V_{DDE_A}, V_{DDE_B}, V_{DDE_SDR}	–0.3	V_{DDE_x} + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100 V/ms	—
Ta [6]	Ambient temperature	—	–40	105	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All parameters are with reference to V_{ss} unless otherwise specified.
2. A crossover current of up to 2 mA may be experienced if V_{DD12} is ramped up before V_{DDE_A} supply. This current is only an electrical crossover but has no functional implications, and should be removed when V_{DDE_A} ramps up to its functional operating range.
3. Not available for input voltage, only for decoupling internal regulators.
4. V_{DDA_REF} is only available on the 516 BGA package.
5. DDR_VREF is expected to be equal to 0.5 × V_{DDE_DDR} and to track V_{DDE_DDR} DC variations as measured at the device pins. Ensure V_{DD_LV} supply ramps up before V_{DDE_DDR}. In Standby mode, it should be ensured that V_{DDE_DDR} supply should be cut off.
6. Tj=125°C. Assumes Ta=105°C. Assumes maximum θJA of 2s2p board. See Thermal attributes section for details.

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

For normal device operations, V_{DDE_A}, V_{DDA}, V_{DDA_REF}, V_{DDEH_ADC} and V_{DD12} supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used. If using the ADC to convert SSD channels then V_{DDA} should always be >= V_{DDM_SMC}.

V_{DD12} should be supplied externally. V_{DDA_REF}, the supply port to 516 BGA is shorted to V_{DDA} inside lower pin packages. Stepper Stall Detect module (SSD) should only be operated in the 4.5 V to 5.5 V range and so cannot be used if V_{DDM_SMD} is in 3.3 V range.

Table 3. Recommended operating conditions

Symbol [1]	Parameter	Conditions	Min[2]	Max	Unit
V_{DDE_A} V_{DDE_B}[3] V_{DDE_SDR}[3]	Input/output supply voltage	—	3.15	3.6	V
V_{SSA}	ADC supply ground, relative to VSS	—	-0.1	0.1	V
V_{DDA}	ADC supply voltage	V_{DDA},V_{DDA_REF} and V_{DDEH_ADC} should be within +/-25 mV of each other	3.15	5.5	V
V_{DDEH_ADC}	ADC I/O supply voltage		3.15	5.5	V
V_{DDA_REF}	ADC reference voltage		3.15	5.5	V
V_{DDM_SMD}	SMD supply voltage	—	3.15	5.5	V
V_{DDE_DDR}	DDR2 supply voltage	—	1.7	1.9	V
DDR_VREF	DDR I/O Reference Voltage	—	V_{DDE_DDR} (min)/2	V_{DDE_DDR} (max)/2	V
V_{DD12}[4]	Core logic supply voltage	—	1.20	1.32	V

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Symbol [1]	Parameter	Conditions	Min[2]	Max	Unit
V_{SSEH_ADC}	ADC supply ground, relative to VSS	—	-0.3	0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_a[5]	Ambient temperature under bias		–40	105	°C

1. All parameters are with reference to Vss, unless otherwise specified.
2. Device will be functional (and electrical specifications as per various datasheet parameters will be guaranteed) until one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. V_{DDE_A}, V_{DDE_B} and V_{DDE_SDR} are all independent supplies and can each be set to 3.3 V. However, care must be taken over LCD inputs that operate across the IO segments.
4. Only applicable when supplying from external source. V_{DD12} supply pins should never be grounded (through a small impedance). If not driven, these should only be left floating.
5. Tj=125°C. Assumes Ta=105°C. Assumes maximum θJA of 2s2p board. See Thermal attributes section for details.

4.3 Voltage regulator electrical specifications

The voltage regulator is composed of the following blocks:

- Connect an external 1.25 V nominal directly
- Low voltage detector - low threshold (LVD_HV_A) for V_{DDE_A} supply
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply
- Various low voltage detectors (LVD_LV_x) for digital core supply (VDD12)
- High voltage detector (HVD_LV) for digital core supply (V_{DD12})
- Power on Reset (POR_LV) for 1.25 V digital core supply (V_{DD12})
- Power on Reset (POR_HV) for V_{DDE_A}

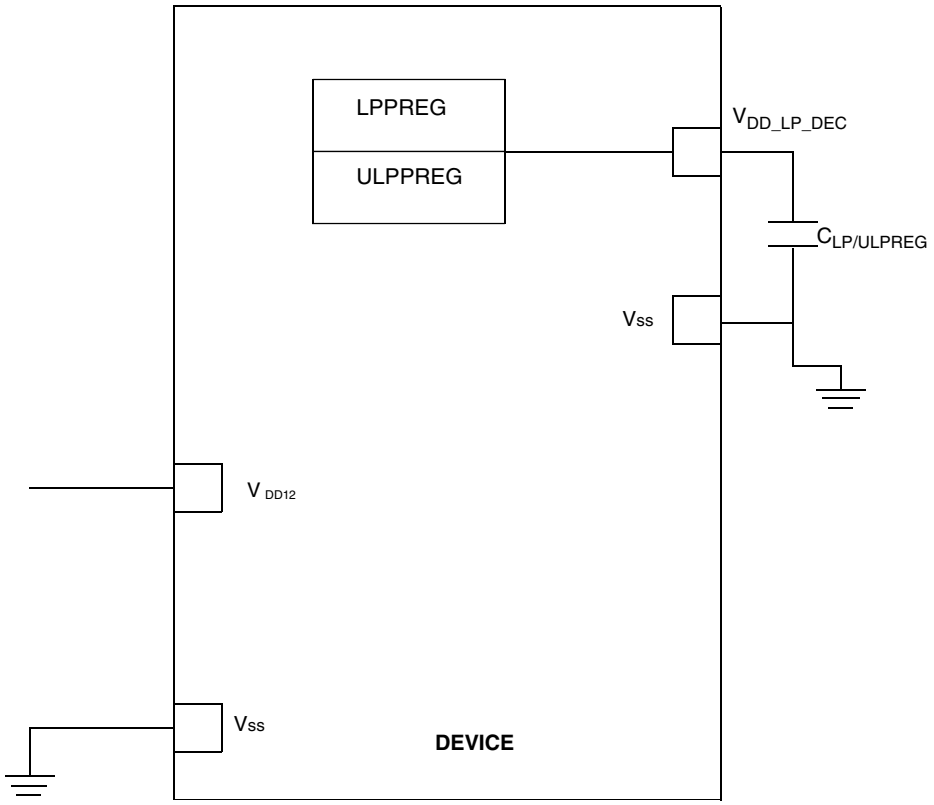


Figure 3. Voltage regulator capacitance connection

Table 4. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations	0.8	1	1.4	µF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm

1. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.

4.3.1 Recommended decoupling capacitor values

Following are the recommendations for supply decoupling on various power domains:

- For V_{DDE_A}, V_{DDE_B}, V_{DDE_SDR}, V_{DDM_SMD}, V_{DDE_DDR}, V_{DDA}, V_{DDEH_ADC},V_{DDA_REF}, DDR_VREF supplies:
  - 0.1 µF close to each VDD/VSS pin pair.
  - 1 µF on each side of the chip for each supply domain.
  - 10 µF near for each power supply source (except for V_{DDM_SMD} pins where a higher capacitance value may be needed depending upon motor characteristics).

- For V_{DD12}, 0.1 µF close to each V_{DD}/V_{SS} pin pair is required.

4.4 Voltage monitor electrical specifications

Table 5. Voltage monitor electrical specifications

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt	Reset Type	Min	Typ	Max	
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	0.9300	0.9790	1.0280	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				0.9800	1.0290	1.0780	V
			Trimmed				-	-	-	V
$V_{HVD\_LV\_cold}$	LV supply high voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.3250	1.3450	1.3750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.3450	1.3650	1.3950	V
$V_{LVD\_LV\_PD2\_hot}$	LV supply low voltage monitoring, detecting in the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1250	1.1425	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1450	1.1625	1.1800	V
$V_{LVD\_LV\_PD1\_hot}$	LV supply low voltage monitoring, detecting in the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
$V_{LVD\_LV\_PD0\_hot}$	LV supply low voltage monitoring, detecting in the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Destructive	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Destructive	2.7000	2.8500	3.0000	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				2.7500	2.9000	3.0500	V
			Trimmed				-	-	-	V
$V_{LVD\_IO\_A\_LO}$	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Destructive	2.7500	2.9230	3.0950	V
			Trimmed				2.9780	3.0260	3.0750	V
		Rise	Untrimmed				2.7800	2.9530	3.1250	V
			Trimmed				3.0080	3.0690	3.1300	V
$V_{LVD\_LV\_PD2\_COLD}$	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.

4.5 Power consumption

The following table shows the power consumption for the device in the various modes of operation.

Table 6. Power consumption

Mode	Configuration	Typ	Max	Unit
Run Mode	CA5 320 MHz, CM4 160 MHz, DDR2 320 MHz, Dual Display (516 BGA)	800	1500	mA
Run Mode	CA5 320 MHz, CM4 160 MHz, SDR 160 MHz, Single Display (208 QFP)	600	1200	mA
IOP Run Mode	CM0+ 16 MHz, PD1/0 domains powered, remainder of device power gated off.	3[1]	35	mA
IOP Stop Mode	CM0+ halted, PD1/0 domains powered, all module enabled and LCD running in IOP domain, remainder of device power gated off.	0.25[2]	20	mA
Stop Mode	Cores halted, Device fully powered.	240	700 [3]	mA
Standby Mode[4, 5]	ARTC/32 KHz + 32 KB SRAM powered	50 (25 °C)	70 (25 °C)	µA
		500 (55 °C)	900 (55 °C)	
		1500 (85 °C)	2500 (85 °C)	
		2000 (105 °C)	4000 (105 °C)	
	ARTC/32 KHz + 8 KB SRAM powered	45 (25 °C)	65 (25 °C)	µA
		500 (55 °C)	900 (55 °C)	
		1500 (85 °C)	2500 (85 °C)	
		2000 (105 °C)	4000 (105 °C)	

1. IOP_Run typical is measured at 25ºC.
2. IOP_Stop typical is measured at 25ºC.
3. There could be 10% variation based on the characterization.
4. Weak pull functionality provided in I/O pads must be used to configure I/Os in a known state (that does not cause contention with external connection on the pin) to avoid floating input to cause crow-bar currents and hence increased leakage during low power modes.
5. During STANDBY/IOP modes, it is recommended to keep V_{DDE_A}, V_{DDEH_ADC}, $V_{DDA}$and V_{DDA_REF} powered to their respective functional levels to obtain best power performance of the device. All other supplies are recommended be kept unpowered in these low power modes.

The following diagrams show the supply configuration of the device.

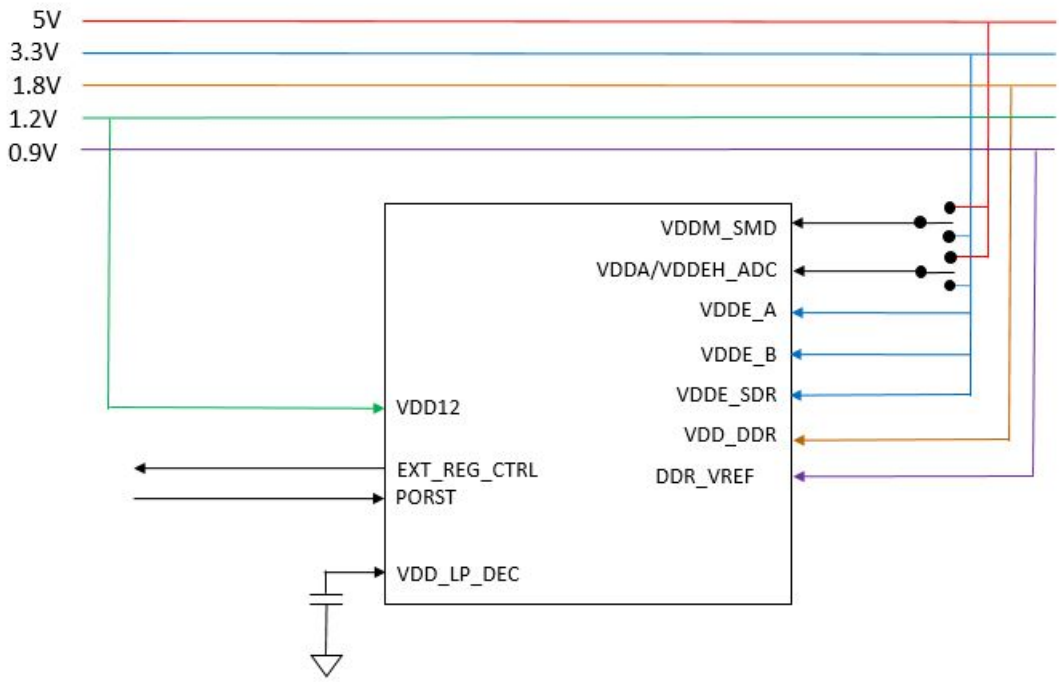


Figure 4. Supply configuration

4.6 Electrostatic discharge (ESD) specifications

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD ratings

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C	H1C	2000	V

Table continues on the next page...

Table 7. ESD ratings (continued)

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
		conforming to AEC-Q100-002			
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V range

Table 8. Functional Pad AC Specifications @ 3.3 V range

Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
	Min	Max		MSB, LSB
pad_sr_hv (output)		1.75/1.5	25	11 (Recommended setting)
	0.8/0.8	3.25/3	50	
	3.5/2.5	12/12	200	
	0.6/0.8	3.75/3.5	25	10
	1/1	7/6.5	50	
	7.7/5	25/21	200	
	4/3.5	25/25	50	01
	6.3/6.2	30/30	200	
	6.8/6	40/40	50	00[1]
	11/11	51/51	200	
pad_i_hv/pad_sr_hv (input)[2]		0.5/0.5	0.5	NA
pad_fc_hv (output)	0.6/0.6	1.5/1.5	30	11
		2.4/2.4	50	
	0.6/0.6	1.5/1.5	20	10
	0.6/0.6	1.85/1.85	10	01
	12/11	36/45	50	00

1. Slew rate control modes
2. Input slope = 2 ns

5.2 DC electrical specifications @ 3.3 V range

Table 9. DC electrical specifications @ 3.3 V range

Symbol	Parameter	Value		Unit
		Min	Max	
Vdde	I/O Supply Voltage	3.15	3.63	V
V_{ih}	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 x Vdde	Vdde + 0.3	V
V_{il}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	Vss – 0.3	0.40 x Vdde	V
V_{ih_hys}	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65 x Vdde	Vdde + 0.3	V
V_{il_hys}	CMOS Input Buffer Low Voltage (with hysteresis enabled)	Vss – 0.3	0.35 x Vdde	V
V_{hys}	CMOS Input Buffer Hysteresis	0.1 x Vdde		V
Pull_Ioh_vil_hys	Weak Pullup Current measured when pad = 0.35 x Vdde	25	80	µA
Pull_Ioh_vih_hys	Weak Pulldown Current measured when pad = 0.65 x Vdde	25	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	–2.5	2.5	µA
V_{oh}	Output High Voltage[1]	0.8 x Vdde	—	V
V_{ol}	Output Low Voltage[2]	—	0.2 x Vdde	V
V_{ih_ttl}	TTL High Level Input Voltage	1.8		V
V_{il_ttl}	TTL Low Level Input Voltage		0.6	V
V_{hyst_ttl}	TTL Input Hysteresis Voltage	0.25		V
V_{ih_auto}	Automotive High Level Input Voltage	0.75 x Vdde	Vdde + 0.3	V
V_{il_auto}[3]	Automotive Low Level Input Voltage	–0.3	0.35 × Vdde	V
V_{hyst_auto}	Automotive Input Hysteresis Voltage	0.11 x Vdde		V

1. Measured when pad is sourcing 2 mA.
2. Measured when pad is sinking 2 mA.
3. Auto levels are applicable to the ‘input only' channels (CH0-7) of the ADC pins

5.3 AC specifications @ 5 V range

Table 10. Functional pad AC specifications @ 5 V range

Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
	Min	Max		MSB, LSB
pad_sr_hv (output)		1.2/1.2	25	11 (Recommended setting)
		2.5/2	50	
		8/8	200	
		3/2	25	10
		5/4	50	
		18/16	200	
		13/13	50	01
		24/24	200	
		24/24	50	00[1]
		50/50	200	
pad_fc_hv (output)		1.8/1.7	50	11
		6.6/6.1	200	
		2.7/2.5	50	10
		10.3/9.3	200	
		5.6/4.8	50	01
		21/19	200	
		41/41	50	00
		151/151	200	

1. Slew rate control modes

5.4 DC electrical specifications @ 5 V range

Table 11. DC electrical specifications @ 5 V range

Symbol	Parameter	Value		Unit
		Min	Max	
V_{dde}	I/O Supply Voltage	4.5	5.5	V
V_{ih}	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 × Vdde	Vdde + 0.3	V
V_{il}	CMOS Input Buffer Low Voltage (with hysteresis disabled)	Vss – 0.3	0.40 × Vdde	V
V_{ih_hys}	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65 × Vdde	Vdde + 0.3	V
V_{il_hys}	CMOS Input Buffer Low Voltage (with hysteresis enabled)	Vss – 0.3	0.35 × Vdde	V

Table continues on the next page...

Table 11. DC electrical specifications @ 5 V range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
V_{hys}	CMOS Input Buffer Hysteresis	0.1 × Vdde		V
Pull_Ioh_vil_h ys	Weak Pullup Current measured when pad = 0.35 x Vdde (Vil_hys)	40	120	µA
Pull_Ioh_vih_hys	Weak Pulldown Current measured when pad = 0.65 x Vdde (Vih_hys)	40	120	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	–2.5	2.5	µA
V_{oh}	Output High Voltage[1]	0.8 x Vdde	—	V
V_{ol}	Output Low Voltage[2]	—	0.2 x Vdde	V
V_{ih_ttl}	TTL High Level Input Voltage	2.0		V
V_{il_ttl}	TTL Low Level Input Voltage		0.8	V
V_{hyst_ttl}	TTL Input Hysteresis Voltage	0.3		V
V_{ih_auto}	Automotive High Level Input Voltage	3.8	Vdde + 0.3	V
V_{il_auto}[3]	Automotive Low Level Input Voltage	–0.3	2.2	V
V_{hyst_auto}[3]	Automotive Input Hysteresis Voltage	0.5		V
Automotive Levels with Expanded VDDE Range: 4 V - 5.5 V				
Vi_{h_auto}[3]	Automotive High Level Input Voltage	0.7 × Vdde	Vdde + 0.3	V
V_{il_auto}[3]	Automotive Low Level Input Voltage	–0.3	0.47 × Vdde	V
V_{hyst_auto}[3]	Automotive Input Hysteresis Voltage	0.11 × Vdde		V

1. Measured when pad is sourcing 2 mA.
2. Measured when pad is sinking 2 mA.
3. Auto levels are applicable to the ‘input only' channels (CH0-7) of the ADC pins

5.5 DDR2 pads IO specifications

5.5.1 DDR2 pads AC specifications @ 1.8V V_{DDE_DDR}

Table 12. DDR2 pads AC electrical specifications at 1.8 V V_{DDE_DDR}

Name	Rise/Fall Edge (V/ns)		Drive Load (pF)	Drive Strength Select (Refer SIUL_MSCR[SRE] description in the device reference manual)
	Min	Max		Half/Full
pad_dq_18	1	—	5	Half
	1	—	20	Half
	1	—	5	Full

Table continues on the next page...

Table 12. DDR2 pads AC electrical specifications at 1.8 V V_{DDE_DDR} (continued)

Name	Rise/Fall Edge (V/ns)		Drive Load (pF)	Drive Strength Select (Refer SIUL_MSCR[SRE] description in the device reference manual)
	Min	Max		Half/Full
	1	—	20	Full
pad_acc_18	1	—	5	Half
	1	—	20	Half
	1	—	5	Full
	1	—	20	Full
pad_clk_18	1	—	5	Half
	1	—	20	Half
	1	—	5	Full
	1	—	20	Full

5.5.2 SSTL_18 Class II 1.8 V DDR2 DC specifications

Table 13. SSTL_18 Class II 1.8 V DDR2 DC specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes	SpecID
V_{DDE_DDR}	DDR 1.8 V I/O Supply voltage	—	1.7	1.8	1.9	V	JESD8-15A	A5.14
V_{DD12}	Core Supply Voltage	—	1.20	1.26	1.32	V		A5.15
DDR_REF	I/O Reference Voltage	—	0.49 x V_{DDE_DDR}	0.50 x V_{DDE_DDR}	0.51 x V_{DDE_DDR}	V		A5.16
$V_{ih(dc)}$	DC Input Logic High	—	DDR_VREF + 0.125	—		V	JESD8-15A	A5.18
$V_{il(dc)}$	DC Input Logic Low	—		—	DDR_VREF – 0.125	V	JESD8-15A	A5.19
$V_{ih(ac)}$	AC Input Logic High	—	DDR_VREF + 0.25	—	—	V	JESD8-15A	A5.20
$V_{il(ac)}$	AC Input Logic Low	—	—	—	DDR_VREF – 0.25	V	JESD8-15A	A5.21
I_{in}	Pad input Leakage Current	—	-50	—	50	µA	—	A5.22
V_{oh}	Output High Voltage Level	—	V_{DDE_DDR} − 0.28	—	—	V	—	A5.23
V_{ol}	Output Low Voltage Level	—	—	—	0.28	V	—	A5.24

Table continues on the next page...

Table 13. SSTL_18 Class II 1.8 V DDR2 DC specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes	SpecID
$I_{oh(dc)}$	Output min source dc current	$V_{out} = V_{oh}$	–12.86	—	—	mA	JESD8-15 A V_{DDE_DDR} = 1.7V Voh = 1.42V	A5.25
$I_{ol(dc)}$	Output min sink dc current	$V_{out}= V_{ol}$	12.86	—	—	mA	JESD8-15 A V_{DDE_DDR} = 1.7 V Vol = 0.28 V	A5.26

Table 14. Current-draw Characteristics for DDR_VREF

Symbol	Parameter	Min	Max	Unit
DDR_VREF	Current-draw characteristics for DDR_VREF	-	5	mA

5.6 SMC pads IO specifications

5.6.1 SMC 5V pads IO specifications

NOTE

In Table 15, Table 16, "V_{DDE}" is the V_{DDM_SMD} supply

5.6.1.1 SMC 5V pads IO DC specifications

Table 15. SMC 5V IO DC specifications(4.5V<vdde<5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{il}	Low level input voltage	–0.3		0.35 × vdde	V
V_{ih}	High level input voltage	0.65 × vdde		vdde + 0.3	V
V_{hyst}	Schmitt trigger hysteresis	0.1 × vdde			V
I_{pu}	Internal pull up device current ($V_{in}=V_{il}$)	–130			µA
I_{pu}	Internal pull up device current ($V_{in}=V_{ih}$)			–10	µA
I_{pd}	Internal pull down device current ($V_{in}=V_{il}$)	10			µA
I_{pd}	Internal pull down device current ($V_{in}=V_{ih}$)			130	µA
I_{in}	Input leakage current (ipp_pue=0)	–2.5		2.5	µA
V_{ol}	Low level output voltage (I_{ol}=+20 mA)			0.32	V

Table continues on the next page...

Table 15. SMC 5V IO DC specifications(4.5V<vdde<5.5V) (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{oh}	High level output voltage (I_{oh}=-20 mA)	vdde – 0.32			V
V_{sum}	Vsum (| Vol | + | Voh |) (I_{ol}=+40 mA and I_{oh}=-40 mA)			1.0	V
V_{oh} delta / V_{ol} delta	Delta V_{oh} across one motor segment and Delta V_{ol} across one motor segment	–50		50	mV
R_{dsonh}	Pad drive active high impedance (test load I_{oh} = 30 mA)	4		13	Ω
R_{dsonl}	Pad drive active low impedance (test load I_{ol} = 30 mA)	2.75		9	Ω

5.6.1.2 SMC 5V pads IO AC specifications

Table 16. SMC 5V IO functional pad AC specifications (4.5V<vdde<5.5V)

Name	Symbol	Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
			Min	Max		ipp_sre_lv
CMOS input				0.5/0.5	0.5	NA

5.6.2 SMC 3.3 V pads IO specifications

NOTE

In Table 17, Table 18, the "V_{DDE}" refers to the V_{DDM_SMD} supply.

5.6.2.1 SMC 3.3 V pads IO DC specifications

Table 17. SMC 3.3 V pads IO DC specifications (3.0V<vdde<3.6V)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{il}	Low level input voltage	-0.3		0.35 × vdde	V
V_{ih}	High level input voltage	0.65 × vdde		vdde + 0.3	V
V_{hyst}	Schmitt trigger hysteresis	0.1 × vdde			V
I_{pu}	Internal pull up device current (V_{in}=V_{il})	-130			µA
I_{pu}	Internal pull up device current (V_{in}=V_{ih})			-10	µA
I_{pd}	Internal pull down device current (V_{in}=V_{il})	10			µA

Table continues on the next page...

Table 17. SMC 3.3 V pads IO DC specifications (3.0V<vdde<3.6V) (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{pd}	Internal pull down device current (V_{in}=V_{ih})			130	µA
I_{in}	Input leakage current (ipp_pue=0)	-2.5		+2.5	µA
V_{ol}	Low level output voltage (I_{ol}=+10 mA)			0.32	V
V_{oh}	High level output voltage (I_{oh}=-10 mA)	vdde – 0.32			V

5.6.2.2 SMC 3.3 V pads IO AC specifications

Table 18. SMC 3.3 V functional pads IO DC specifications (3.0V<vdde<3.6V)

Name	Symbol	Symbol	Rise/Fall Edge (ns)		Drive Load (pF)	Drive/Slew Rate Select
			Min	Max		ipp_sre_lv
CMOS input				0.5/0.5	0.5	NA

5.7 RSDS pads electrical specifications

Table 19. RSDS pads electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Supply Voltages					
	V_{dde}[1]	3	3.3	-	V
RSDS_Tx					
	Normal mode (V_{dde})	-	3	-	mA
	Power down mode	-	1	-	µA
RSDS reference					
	Normal mode	-	400	-	µA
	Power down mode	-	0.1	-	µA
Data rate					
	Data Frequency		50	50	MHz
Driver specs					
V_{od}	Differential o/p voltage	100	200	400	mV
V_{os}	Common mode voltage (VOS)	-	1.2	-	V
t_R/t_F	Rise/Fall time	-	500	-	ps
	Startup Time (RSDS_ref)	-	6	-	µs
	Startup time (RSDSTx)	-	6	-	µs
Termination					

Table continues on the next page...

Table 19. RSDS pads electrical specifications (continued)

	Termination Resistance	-	100	-	ohm
	Trans. Line (differential Zo)	95	100	105	ohm
Skew					
t_{skew}[2]	Skew between different RSDS lines	-	382	-	ps

1. vdde is the V_{DDE_B} supply
2. This value is derived from simulation assuming default register setting of all 1's for skew. There are 8 programmable bits to provide 256 different skew numbers with various combinations of these bits. See the TCON chapter of the device Reference Manual for details. All "0" combination of 8 bits is not valid.

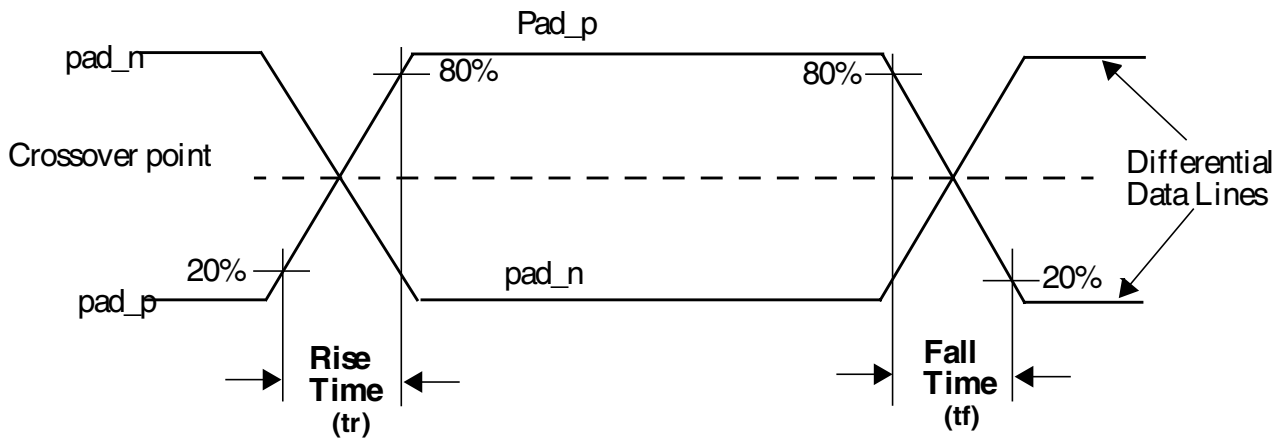


Figure 5. Rise/Fall transition

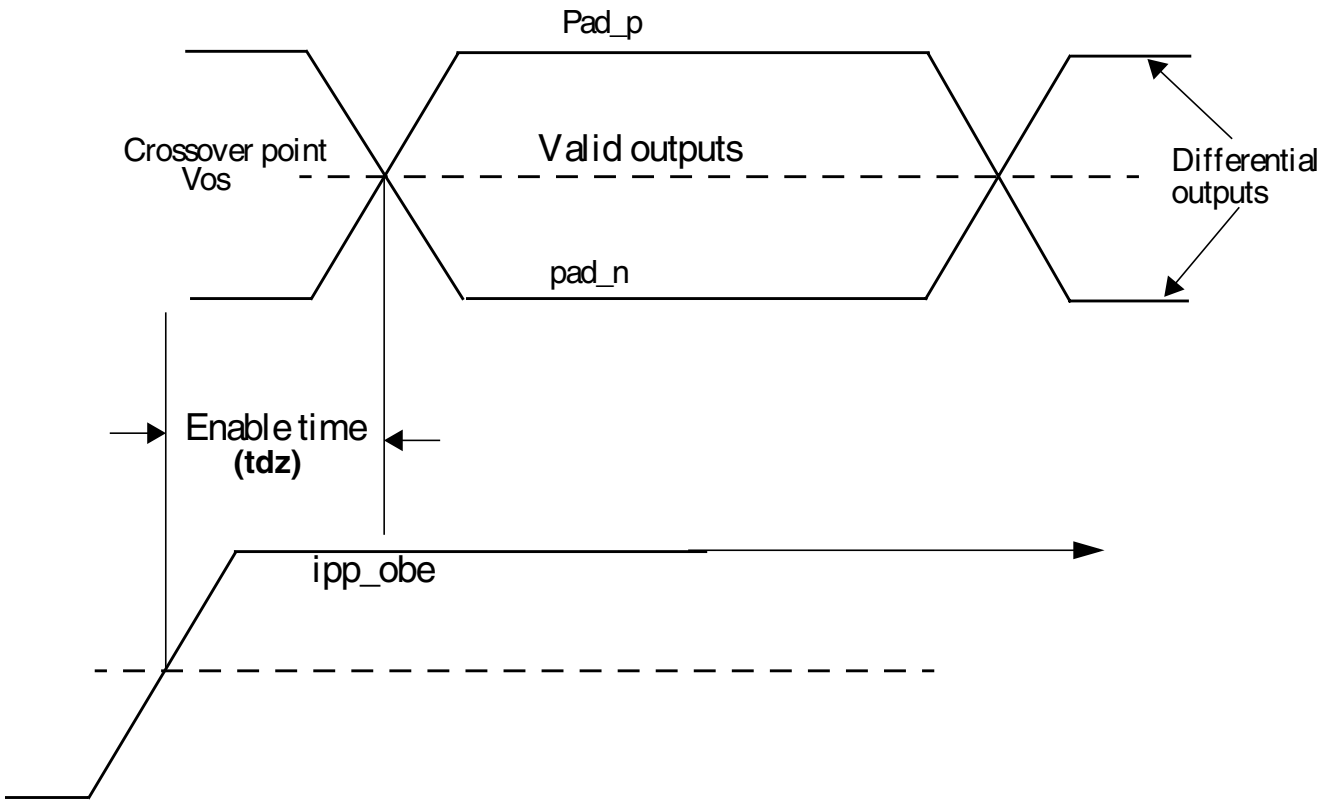


Figure 6. Enable time

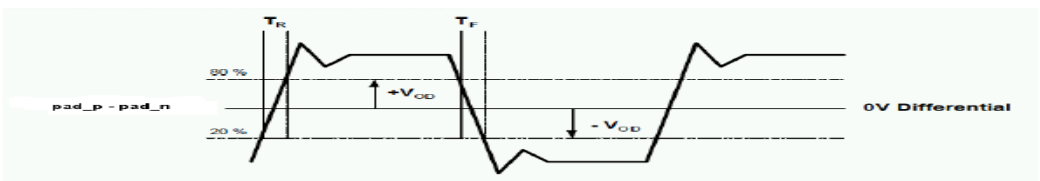


Figure 7. Rise/Fall transition of differential output

5.8 LVDS pads electrical specifications

Table 20. LVDS pads electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Supply Voltages					

Table continues on the next page...

Table 20. LVDS pads electrical specifications (continued)

	V_{DDE} [1]	3	3.3	-	V
Current consumption					
LVDS Tx					
	Normal mode (V_{DDE} [1])	—	5	—	mA
	Switching currents	—	±1.5 (during output transition)	—	mA
	Power down mode	—	1	—	µA
LVDS Reference					
	Normal mode	—	400	—	µA
	Power down mode	—	0.1	—	µA
Data Rate					
	Data Frequency	—	—	560	Mbps
Driver specs					
V_{od}	Differential o/p voltage [2]	247	—	454	mV
V_{os}	Common mode voltage (V_{OS})	1.125	—	1.375	V
t_r/t_f	Rise/Fall time [3]	—	—	800	ps
	Startup Time (lvds_ref)	—	5	—	µs
	Startup time (lvds_Tx)	—	5	—	µs
Termination					
	Termination Resistance	—	100±1%	—	Ω
	Trans. Line (differential Zo)	95	100	105	Ω

1. V_{DDE} is the V_{DDE_B} supply.
2. The limit applies to the default drive current.
3. Rise/fall time is assumed to be measured with 20%-80% levels.

5.9 Functional reset pad electrical specifications

The device implements a dedicated bidirectional RESET pin.

Table 21. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	V_{DDE_A}+0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.65	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV

Table continues on the next page...

Table 21. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DDE\_A}=V_{DD\_POR}$ V_{OL} = 0.35 x V_{DDE_A}	0.2	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\lvert I_{WPU} \rvert$	Weak pull-up current absolute value	RESET pin $V_{IN} = V_{DD}$	23	—	82	µA

5.10 PORST electrical specifications

Table 22. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x V_{DDE_A}	—	V
V_{IL}	Input low level	—	0.35 x V_{DDE_A}	—	V

6 Peripheral operating requirements and behaviors

6.1 Analog modules

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

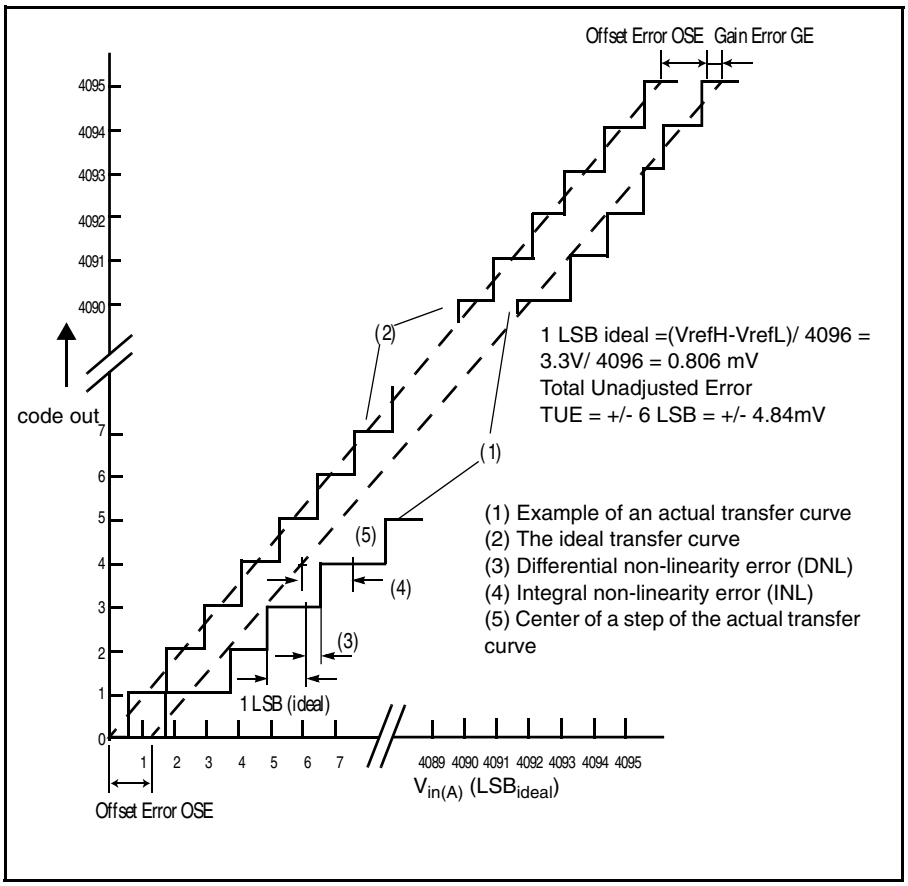


Figure 8. ADC characteristics and error definitions

6.1.1.1 Input impedance and ADC accuracy

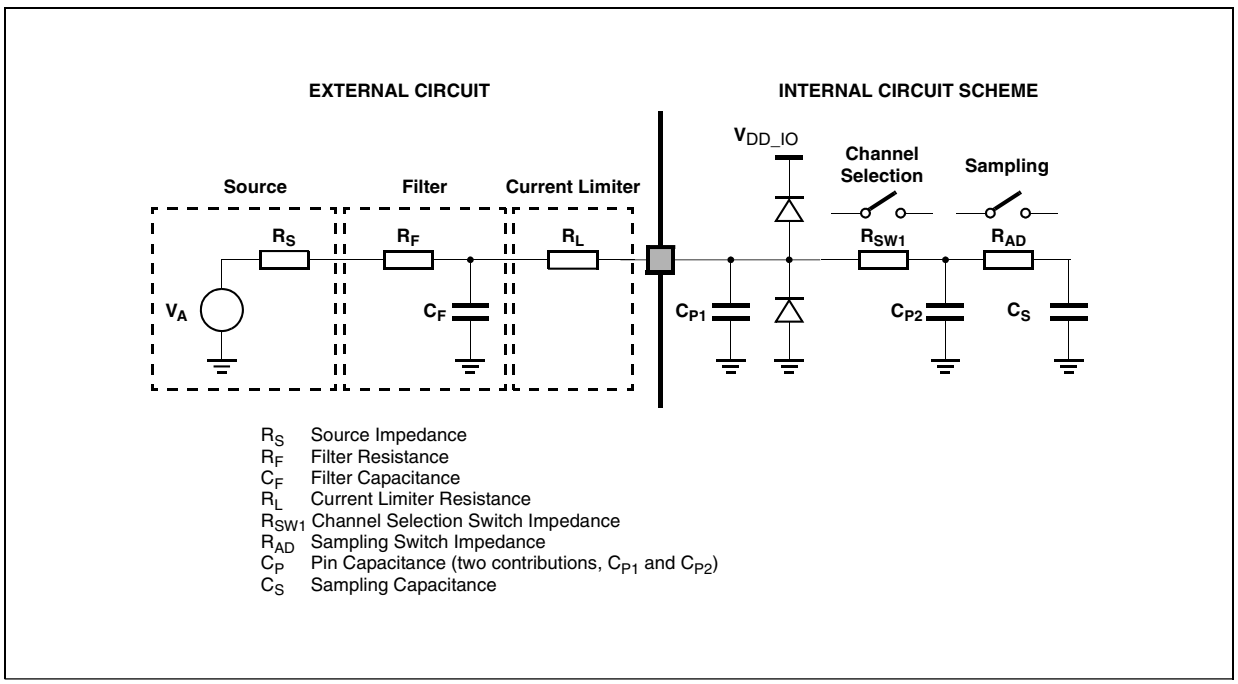


Figure 9. Input equivalent circuit

Table 23. ADC conversion characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[1] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1	MHz
t_{sample}	Sample time[2]	80 MHz@ 100 ohm source impedance	250	800	—	ns
t_{conv}	Conversion time[3]	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[4]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
ADC Analog Pad (pad going to one ADC)	Max leakage	125°C	—	—	250	nA
	Max positive/negative injection		–5	—	5	mA

Table continues on the next page...

Table 23. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC (12-bit mode)						
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/- 4	6	LSB
		With current injection	—	+/- 5	—	LSB
$T_{recovery}$	Differential non-linearity	—	—	—	<1	µs
ADC (10-bit mode)[6]						
INL	Integral non-linearity	—	–1	—	1	LSB
DNL	Differential non-linearity	—	–0.7	—	0.7	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–5	+/- 3	5	LSB
		With current injection	—	+/- 4	—	LSB
$T_{recovery}$	Differential non-linearity	—	—	—	<1	µs

1. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
2. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
3. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
4. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
5. See Figure 2.
6. Measurements taken with same ADC accuracy settings as for 12bit. ADC data is read from CDR with last 2-LSBs ignored.

6.1.2 Analog Comparator (CMP) electrical specifications

Table 24. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DDE_A}	V
V_{AIO}	Analog input offset voltage [1]	-42	—	42	mV
V_H	Analog comparator hysteresis [2]	—	1	25	mV
	• CR0[HYSTCTR] = 00	—	20	50	mV
	• CR0[HYSTCTR] = 01	—	40	70	mV

Table continues on the next page...

Table 24. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	• CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	—	60	105	mV
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	14	µs
	Analog comparator initialization delay, High speed mode[4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
INL	6-bit DAC integral non-linearity	–1	—	1	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}$/64

6.2 Clocks and PLL interfaces modules

6.2.1 Fast Oscillator (FXOSC) electrical specifications

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

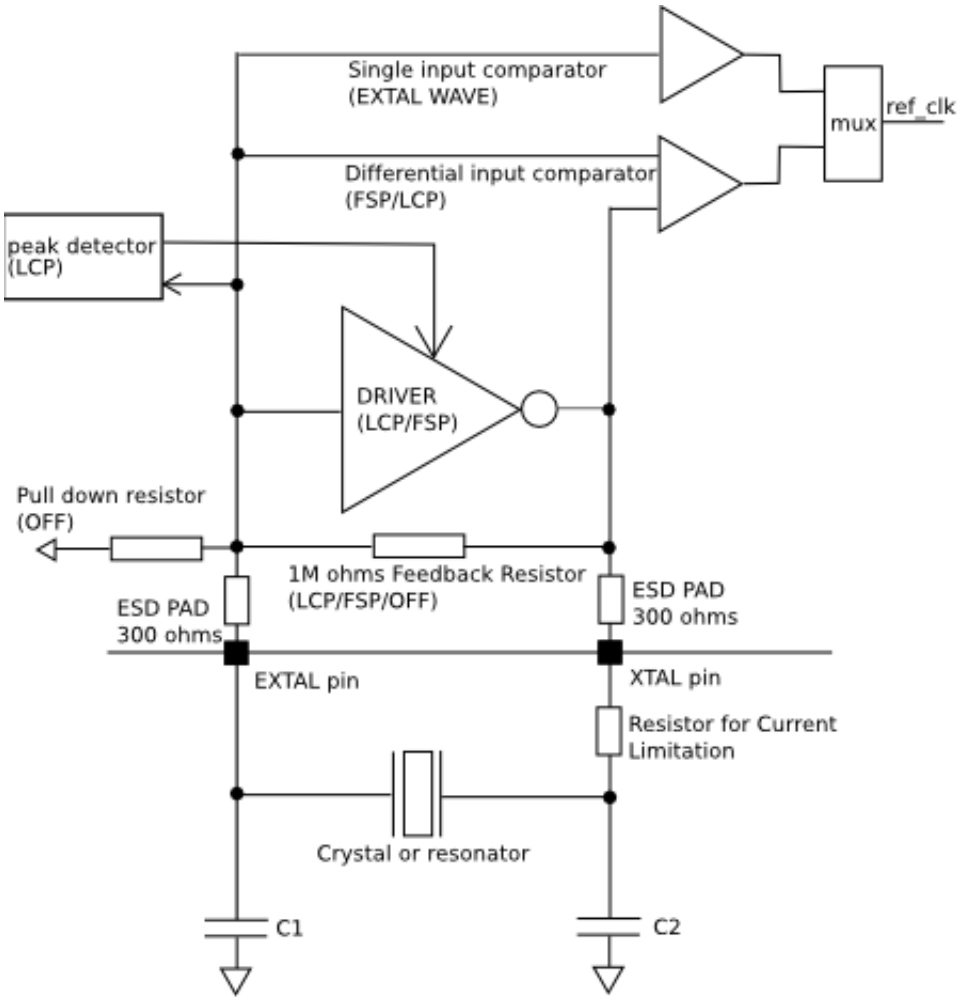


Figure 10. Oscillator connections scheme

Table 25. Fast Oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$T_{XOSCHSSU}$	Startup time	FSP/LCP	8-40 MHz		1		ms
	Supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		µA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3		1.84		V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3		1.48		V

6.2.2 Slow Oscillator (SXOSC) electrical specifications

Table 26. Slow Oscillator (SXOSC) electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	kHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s
V_{pp}	Peak-to-Peak XTAL Amplitude			0.5[3]		V

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.
3. RF is integrated and may not be attached externally.

6.2.3 Fast internal RC Oscillator (FIRC) electrical specifications

Table 27. Fast internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz
$T_{startup}$	Startup time	—		—	1.5[1]	µs
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.2	%
I_{VDDHV}	Current consumption on 3.3 V power supply	After $T_{startup}$	—	—	75	µA
I_{VDDLV}	Current consumption on 1.2 V power supply	After $T_{startup}$	—	—	25	µA

1. The start-up time is generally 16 clock cycles of FIRC untrimmed clock.

6.2.4 Slow internal RC oscillator (SIRC) electrical specifications

Table 28. Slow internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{osc}	Oscillator frequency	Calibrated	119	128	136.5	kHz
	Temperature dependence				600	ppm/C

Table continues on the next page...

Table 28. Slow internal RC oscillator electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

6.2.5 PLL electrical specifications

Table 29. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 30	ps	NON SSCG mode
TIE			See Table 30		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	µs	Calibration mode

Table 30. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN} [1]	Jitter due to Fractional Mode (ps) J_{SDM} [2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1, 2	$+/-(J_{SN}+J_{SDM}+J_{SSCG}+N^{[4]} \times J_{RJ})$
Long Term Jitter (Integer Mode)				40	$+/-(N \times J_{RJ})$
Long Term jitter (Fractional Mode)				100	$+/-(N \times J_{RJ})$

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on avdd, avss, dvdd, dvss.
2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See Percentage of sample exceeding specified value of jitter table

Table 31. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory specifications

NOTE

Flash specs defined in this section at 150°C are also valid for the maximum temperature specifications of the device.

6.3.1.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 32 shows the estimated Program/Erase times.

Table 32. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs

Table continues on the next page...

Table 32. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.1.2 Flash memory Array Integrity and Margin Read specifications

Table 33. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs

Table continues on the next page...

Table 33. Flash memory Array Integrity and Margin Read specifications (continued)

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.1.3 Flash memory module life specifications

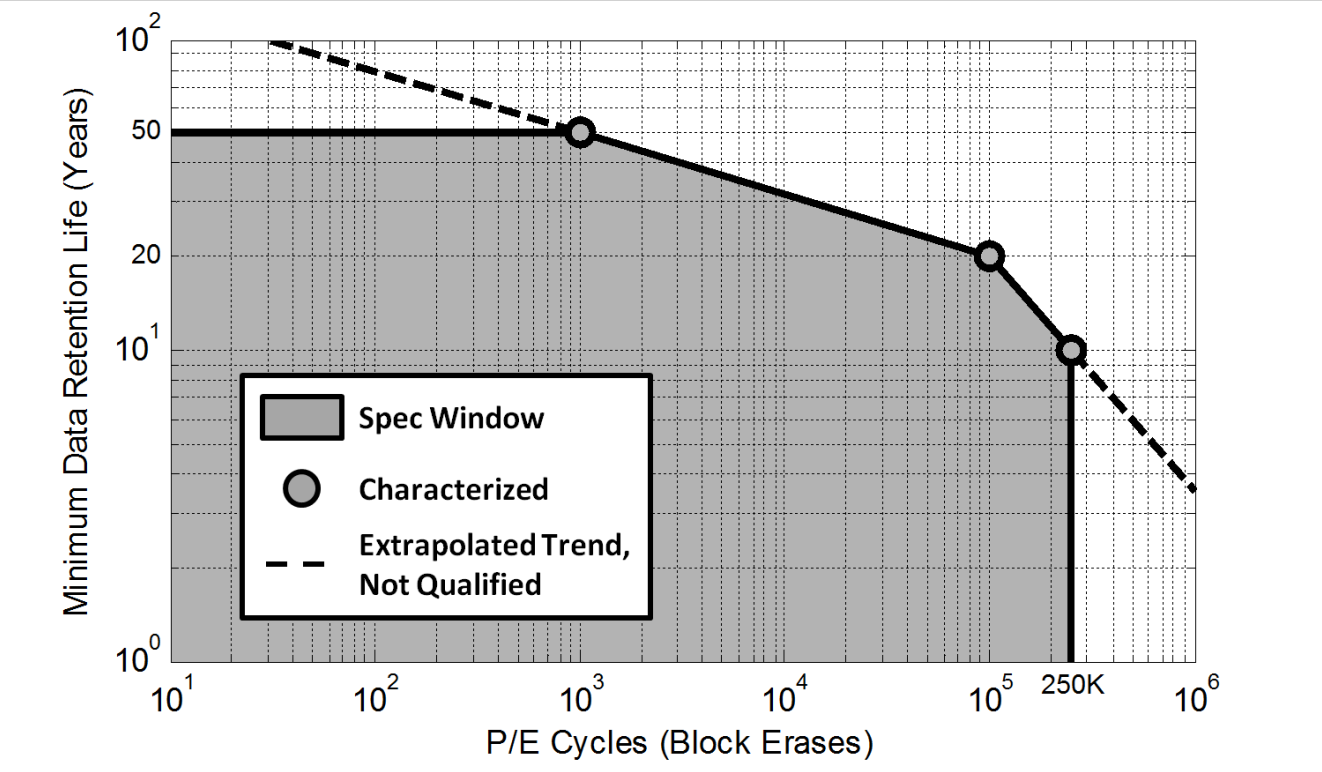
Table 34. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

6.3.1.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.3.1.5 Flash memory AC timing specifications

Table 35. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16	—	45	µs

Table continues on the next page...

Table 35. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
		plus seven system clock periods.		plus seven system clock periods	
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

6.3.1.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 150 °C.

Table 36. Flash read wait state and address pipeline control guidelines

Flash Frequency	RWSC setting	APC setting
0 MHz < fFLASH ≤ 33 MHz	0	0
33 MHz < fFLASH ≤ 100 MHz	2	1
100 MHz < fFLASH ≤ 133 MHz	3	1
133 MHz < fFLASH ≤ 167 MHz	4	1
167 MHz < fFLASH ≤ 200 MHz	5	2

6.3.2 QuadSPI AC specifications

- Measurements are with a load of 35 pF on output pins. Input slew: 1ns, DSE[1:0]=11
- QuadSPI input timing is with 15pF load on flash output

The following table lists various QuadSPI modes and their corresponding configurations. These DDR configurations are applicable when used without learning. Please see the device reference manual for register and bit descriptions.

Table 37. QuadSPI read/write settings

QuadSPI Modes		QuadSPI_MCR[DDR_EN]	QuadSPI_MCR[DQS_EN]	QuadSPI_MCR [SCLKCFG]	QuadSPI_SOCCR [SOCCFG]	QuadSPI_FLSHCR[TDH]
SDR mode	Internal DQS mode	0	1	07h	002F_002Fh	00
DDR mode (without learning)	4x Sampling mode	1	0	Don't care	Don't care	10
	Internal DQS mode	1	1	03h	002F_002Fh	10
	HyperFlash mode	1	1	02h	0000_0000h	10

6.3.2.1 SDR mode

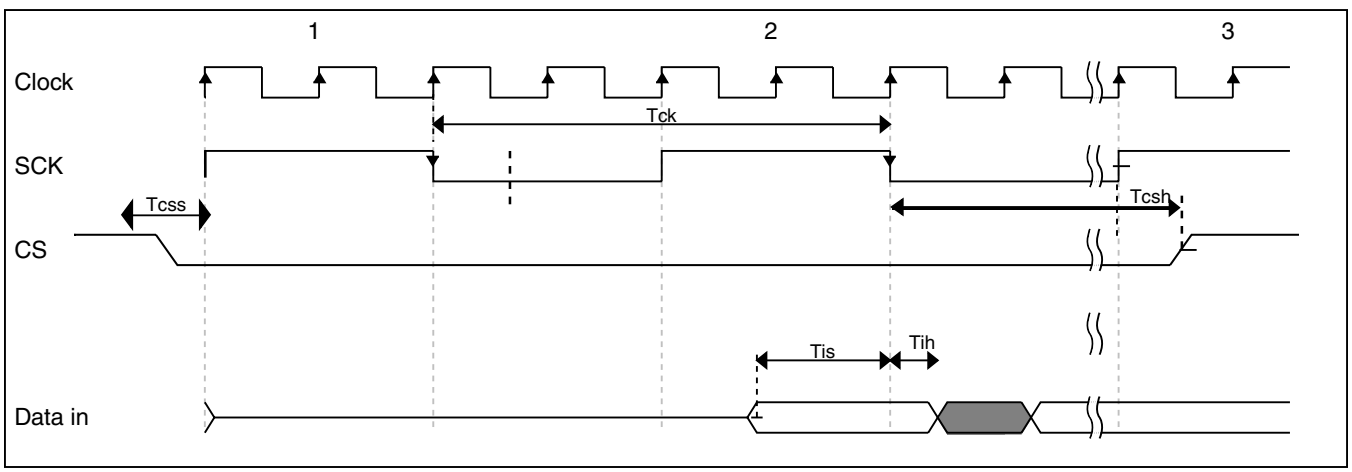


Figure 11. QuadSPI input timing (SDR mode) diagram

NOTE

- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- All board delays need to be added appropriately
- Input hold time being negative does not have any implication or max achievable frequency

Table 38. QuadSPI input timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	5.5	-	ns
T_{ih}	Hold time for incoming data	1.5	-	ns
F_{SCK}	SCK clock frequency	-	80	MHz

NOTE

For SDR mode, QuadSPI_MCR[DQS_EN] must be set as '1'.
The delay chain settings for this mode is mentioned Table 37.

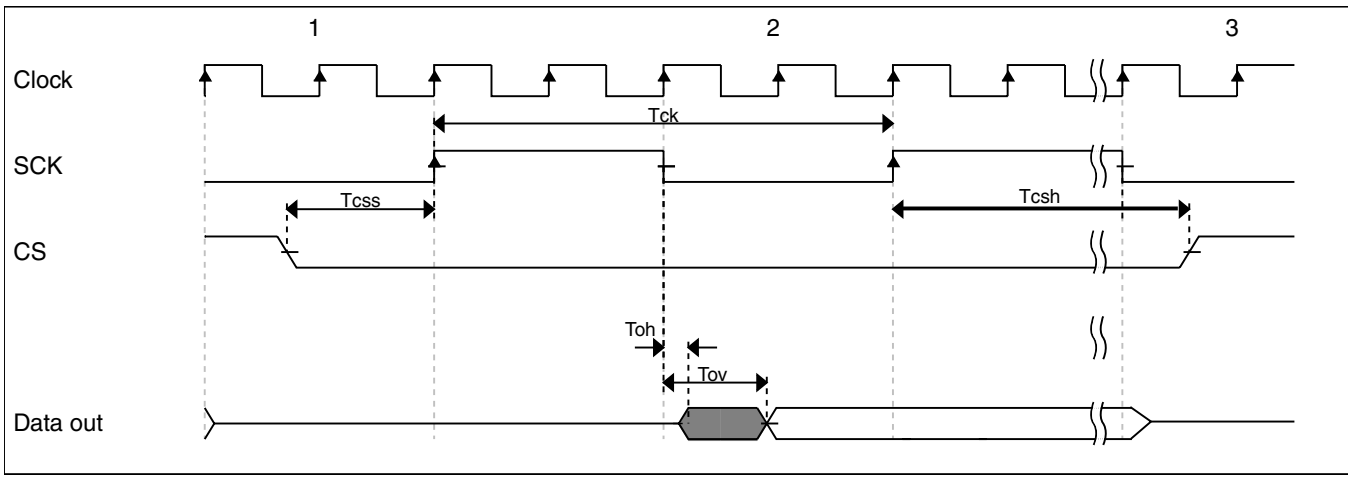


Figure 12. QuadSPI output timing (SDR mode) diagram

Table 39. QuadSPI output timing (SDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	2.8	ns
T_{oh}	Output Data Hold	-1.5	-	ns
T_{ck}	SCK clock period	-	80	MHz
T_{css}	Chip select output setup time	1	-	ns
T_{csh}	Chip select output hold time	-1	-	ns

6.3.2.2 DDR mode

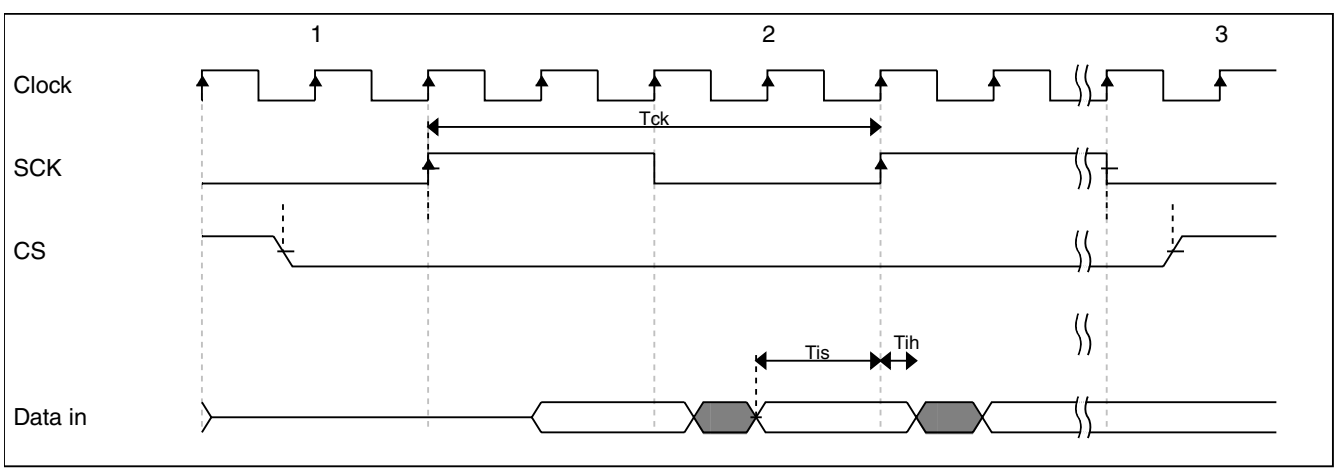


Figure 13. QuadSPI input timing (DDR mode) diagram

Table 40. QuadSPI input timing (DDR mode) specifications without learning (valid across PVT)

Symbol	Parameter	Value		Unit	Configuration
		Min	Max		
T_{is}	Setup time for incoming data	5.5	—	ns	
T_{ih}	Hold time for incoming data	1.5	—	ns	
F_{SCK}	SCK Clock Frequency	—	45 (Internal DQS)	MHz	Refer Table 37
		—	35 (4x sampling)		QSPI_SMPR[DDRSMP]=1

Table 41. QuadSPI input timing (DDR mode) specifications with learning

Symbol	Parameter	Value		Unit	Note
		Min	Max		
F_{SCK}	SCK Clock Frequency	—	80 (Internal DQS) [1]	MHz	Flash data valid window must be > 3.5 ns
		—	66 (4x sampling)		Flash data valid window must be > 3.5 ns, Flash max access time must be < = 6.5 ns

1. Multiple (dynamic) calibration across voltage/temperature on board required.

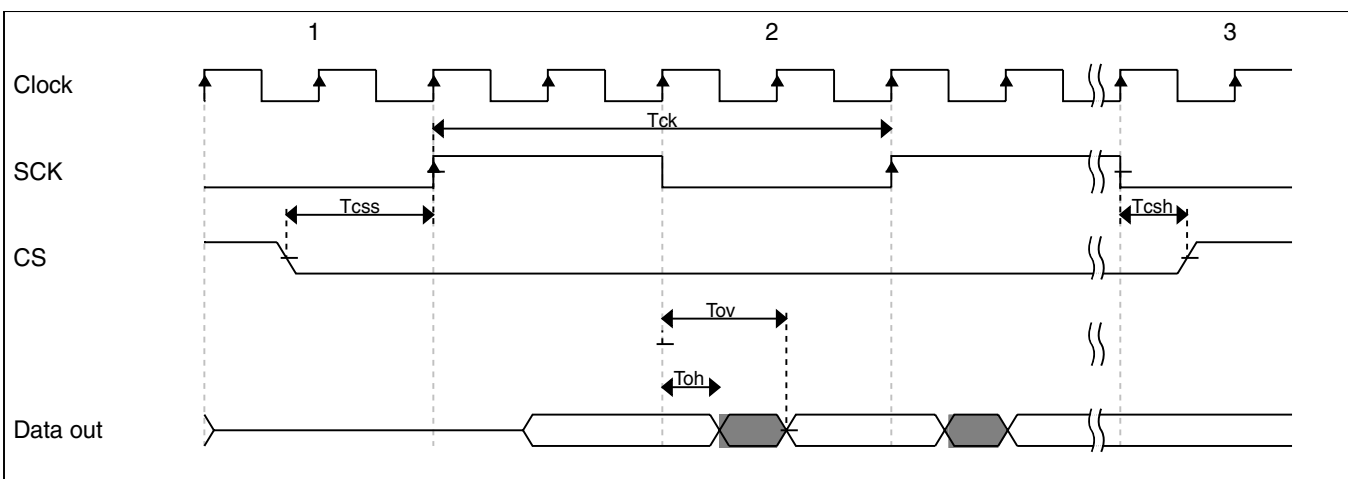


Figure 14. QuadSPI output timing (DDR mode) diagram

Table 42. QuadSPI output timing (DDR mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	4.5	ns
T_{oh}	Output Data Hold	1.5	-	ns
T_{css}	Chip select output setup time	1	-	ns

Table continues on the next page...

Table 42. QuadSPI output timing (DDR mode) specifications (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{csh}	Chip select output hold time	-1	-	ns

6.3.2.3 HyperFlash mode

NOTE

In HyperFlash mode, the read/write maximum frequency is 90 MHz.

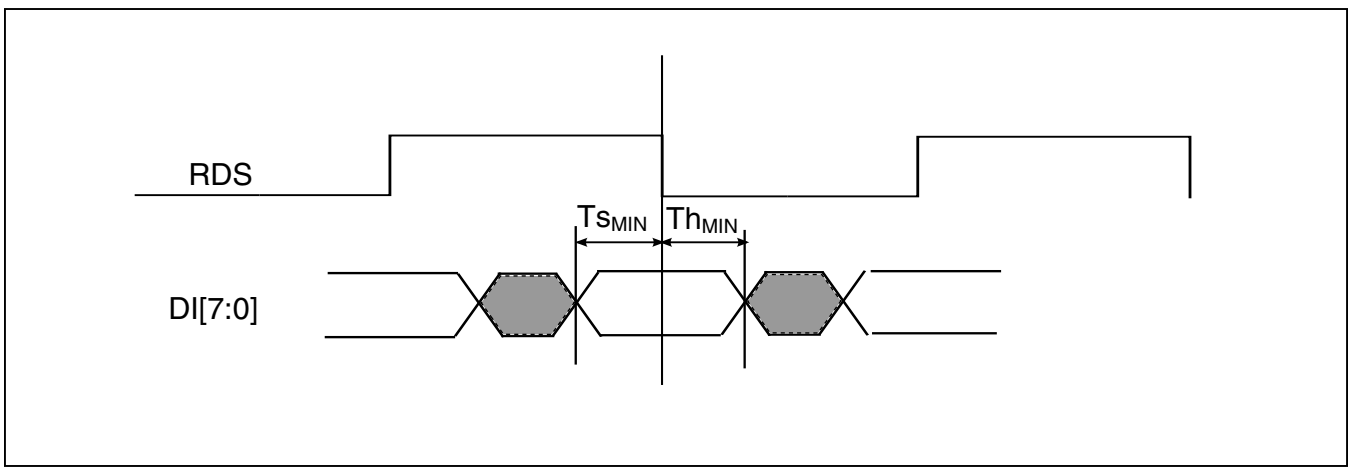


Figure 15. QuadSPI input timing (Hyperflash mode) diagram

Table 43. QuadSPI input timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit	Configurations
		Min	Max		
Tis	Setup time for incoming data	2	-	ns	Refer Table 37
Tih	Hold time for incoming data	2	-	ns	

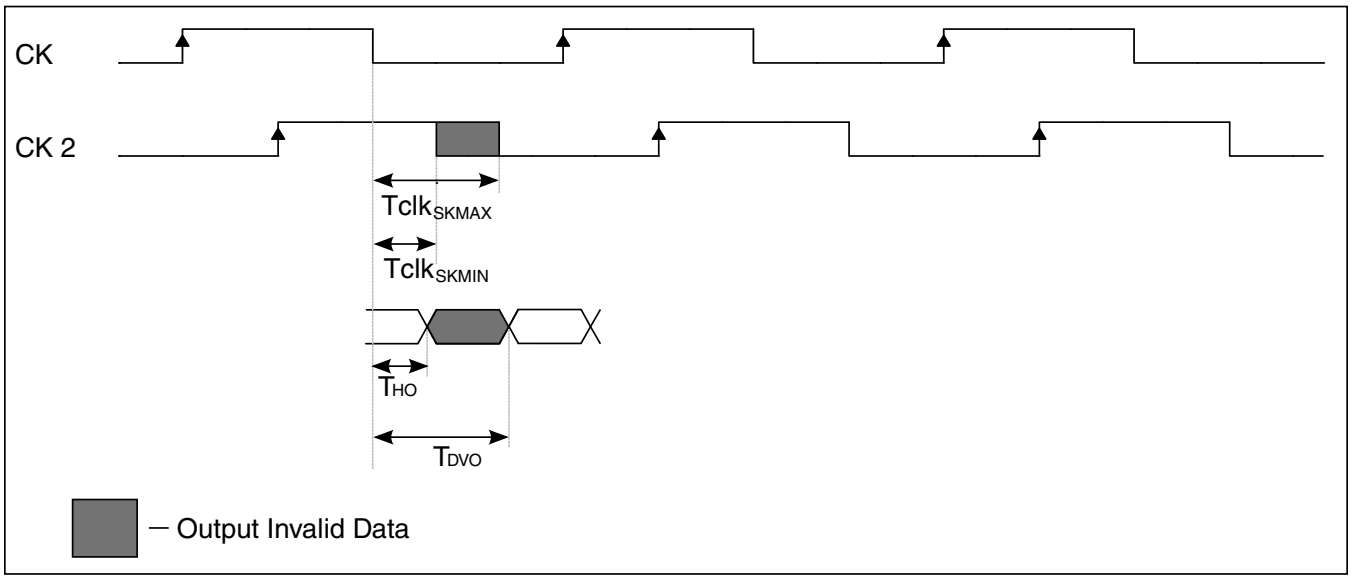


Figure 16. QuadSPI output timing (Hyperflash mode) diagram

Table 44. QuadSPI output timing (Hyperflash mode) specifications

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output Data Valid	-	3	ns
T_{HO}	Output Data Hold	1.3	-	ns
$Tclk_{SKMAX}$	CK to CK2 skew max	-	T/4 + 0.5	ns
$Tclk_{SKMIN}$	CK to CK2 skew min	T/4 - 0.5	-	ns

6.3.3 SDR AC specifications

For details on read timings with and without the external capacitor and capacitance value, refer the "Chip-specific MDDRC information" section of the device Reference Manual.

For SDRAM operating frequencies above 80 MHz the SDR_A12 pin cannot be used for the SDRAM address. At higher operating frequencies this pin requires an external capacitor connected with V_{SS} to adjust the read timing.

Round trip delay (consisting of board trace delay of SDCK and DQ(READ)) should not be more than 450 ps.

NOTE

1. All transitions measured at mid-supply (V_{DDE_SDR}/2).
2. Data signal which are driven from ATE are given a swing of 20%/80% of full signal swing.

3. The DQS Config Offset Count register (MDDRC_DQS_CFG) would need to be programmed with value 0x0000_16h in the initialization code when operating SDR at 160 MHz.
4. The SRE settings for SDR_CLK pad going to the external memory should be 2'b11 (as noted in the "Section 15.3.2.1 Recommended settings for SRE pads" in the Reference Manual). SRE settings for loopback clock A12 has been reduced to 2'b01 in CZ to help with EMC improvement.

Table 45. SDR @ 160 MHz AC timing specification

ID	Symbol	Parameter	Min	Typ	Max	Unit
—	t_{SDCK}	Clock Period	—	6.25	—	ns
DD1	t_{QVS}	Data output Valid (Write transaction)	—	—	$(0.5 \times t_{SDCK}) + 1.125$	ns
DD2[1]	t_{QH}	Data output Hold (Write transaction)	1.5	—	—	ns
DD3	t_{IS}	Data Input Setup (Read transaction)	-0.4	—		ns
DD4	t_{IH}	Data input Hold (Read transaction)	3.7	—	—	ns
—	t_{CH}	CK HIGH pulse width	0.43	—	0.57	t_{CK}
—	t_{CL}	CK LOW pulse width	0.43	—	0.57	t_{CK}
—	—	Series termination (Data/CLK/ Address/Command)	—	50	—	ohms
—	—	Trans. line impedance (Zo)	—	50	—	ohms

1. Applies to command and address buses also.

Table 46. SDR @ 80 MHz AC timing specification

ID	Symbol	Parameter	Min	Typ	Max	Unit
—	t_{SDCK}	Clock Period	—	12.5	—	ns
DD1	t_{QVS}	Data output Valid (Write transaction)	—	—	$(0.5 \times t_{SDCK}) + 1.25$	ns
DD2[1]	t_{QH}	Data output Hold (Write transaction)	3.0	—	—	ns
DD3	t_{IS}	Data Input Setup (Read transaction)	2.2	—		ns
DD4	t_{IH}	Data input Hold (Read transaction)	2.0	—	—	ns
—	t_{CH}	CK HIGH pulse width	0.43	—	0.57	t_{CK}
—	t_{CL}	CK LOW pulse width	0.43	—	0.57	t_{CK}
—	—	Series termination (Data/CLK/ Address/Command)	—	50	—	ohms
—	—	Trans. line impedance (Zo)	—	50	—	ohms

1. Applies to command and address buses also.

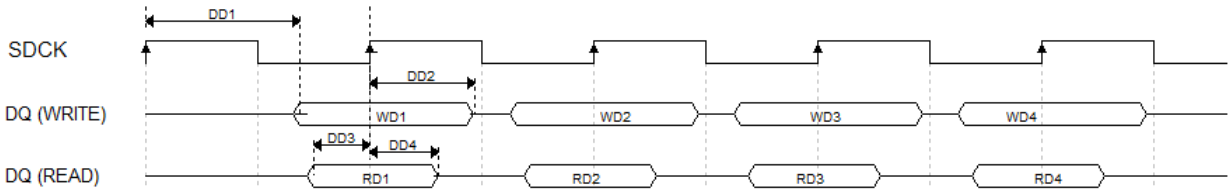


Figure 17. SDR (@ 160 MHz and @ 80 MHz) AC read and write timings

6.3.3.1 SDR DC specifications

The SDR DC specifications are same as pad_fc_hv specs described in this document.

6.3.4 DDR2 SDRAM AC specifications

NOTE

DDR2-800 (-25E speed grade) is the lowest speed grade supported. If self-refresh mechanism needs to be supported, an external pull-down resistance needs to be connected to the DDR CKE pin.

NOTE

Specified values in the table are at recommended operating conditions with V_{DDE_DDR} of 1.8±5.5%

Table 47. DDR2 SDRAM timing specifications[1, 2, 3, 4, 5]

ID	Symbol	Parameter	Min	Typ	Max	Unit
—	F	Frequency of operation (Clock Period)	—	—	320	MHz
—	V_{IX-AC}	MCK AC differential crosspoint voltage	0.5 × V_{DDE_DDR} — 0.175	—	0.5 × V_{DDE_DDR} + 0.175	V
DD1	t_{DDR_CLK}	Clock period	3.125	—	—	ns
DD2	t_{DDR_CLKH}	High pulse width[6]	0.47	—	0.53	tCK
DD3	t_{DDR_CLKL}	Low pulse width	0.47	—	0.53	tCK
DD4	t_{CMS}	Address/Command Output Setup	0.5 × t_{DDR_CLK}–0.75	—	—	ns
DD5	t_{CMH}	Address/Command Output Hold	0.5 × t_{DDR_CLK}–0.75	—	—	ns
DD6	t_{DQSS}	First DQS latching transition to associated clock edge	-0.18 × t_{DDR_CLK}	—	0.18 × t_{DDR_CLK}	ns

Table continues on the next page...

Table 47. DDR2 SDRAM timing specifications[1, 2, 3, 4, 5] (continued)

ID	Symbol	Parameter	Min	Typ	Max	Unit
DD7	t_{OS}	Data and Data Mask Output Setup relative to DQS (DDR Write Mode) [8, 9]	$t_{DDR\_CLK}/4 - 0.4$	—	—	ns
DD8	t_{OH}	Data and Data Mask Output Hold relative to DQS (DDR Write Mode) [7, 10]	$t_{DDR\_CLK}/4 - 0.4$	—	—	ns
DD9	t_{IS}	Input Data Skew relative to DQS[11]		—	0.24	ns
—	—	Parallel termination address lines	—	50	—	Ohms
—	—	Differential clock lines	—	100	—	Ohms
—	—	Trans. Line (differential Zo)	—	50	—	Ohms

1. V_{DDE_DDR} value is 1.8 V for DDR2 mode
2. C_Z at -40 to 125 °C.
3. Measured with clock pin loaded with differential 100 ohm termination resistor.
4. All transitions measured at mid-supply ($V_{DDE\_DDR}/2$).
5. Measured with all outputs except the clock loaded with 50 ohm termination resistor to $V_{DDE\_DDR}/2$.
6. Pulse width high + pulse width low cannot exceed minimum and maximum clock period.
7. The losses for IO and package are 190 ps and are already included in the 400 ps budget taken by the device.
8. This specification relates to the required input setup time of DDR memories. The chip output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory is in violation. DDR_DQ[31:24] is relative to DDR_DQS[3]; DDR_DQ[23:16] is relative to DDR_DQS[2], DDR_DQ[15:8] is relative to DDR_DQS[1] and DDR_DQ[7:0] is relative to DDR_DQS[0].
9. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.
10. This specification relates to the required hold time of DDR memories. DDR_DQ[31:24] is relative to DDR_DQS[3]; DDR_DQ[23:16] is relative to DDR_DQS[2], DDR_DQ[15:8] is relative to DDR_DQS[1] and DDR_DQ[7:0] is relative to DDR_DQS[0].
11. Data input skew is derived from each DDR_DQS clock edge. It begins with a DDR_DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

Figure 18 shows the DDR2 SDRAM write timing.

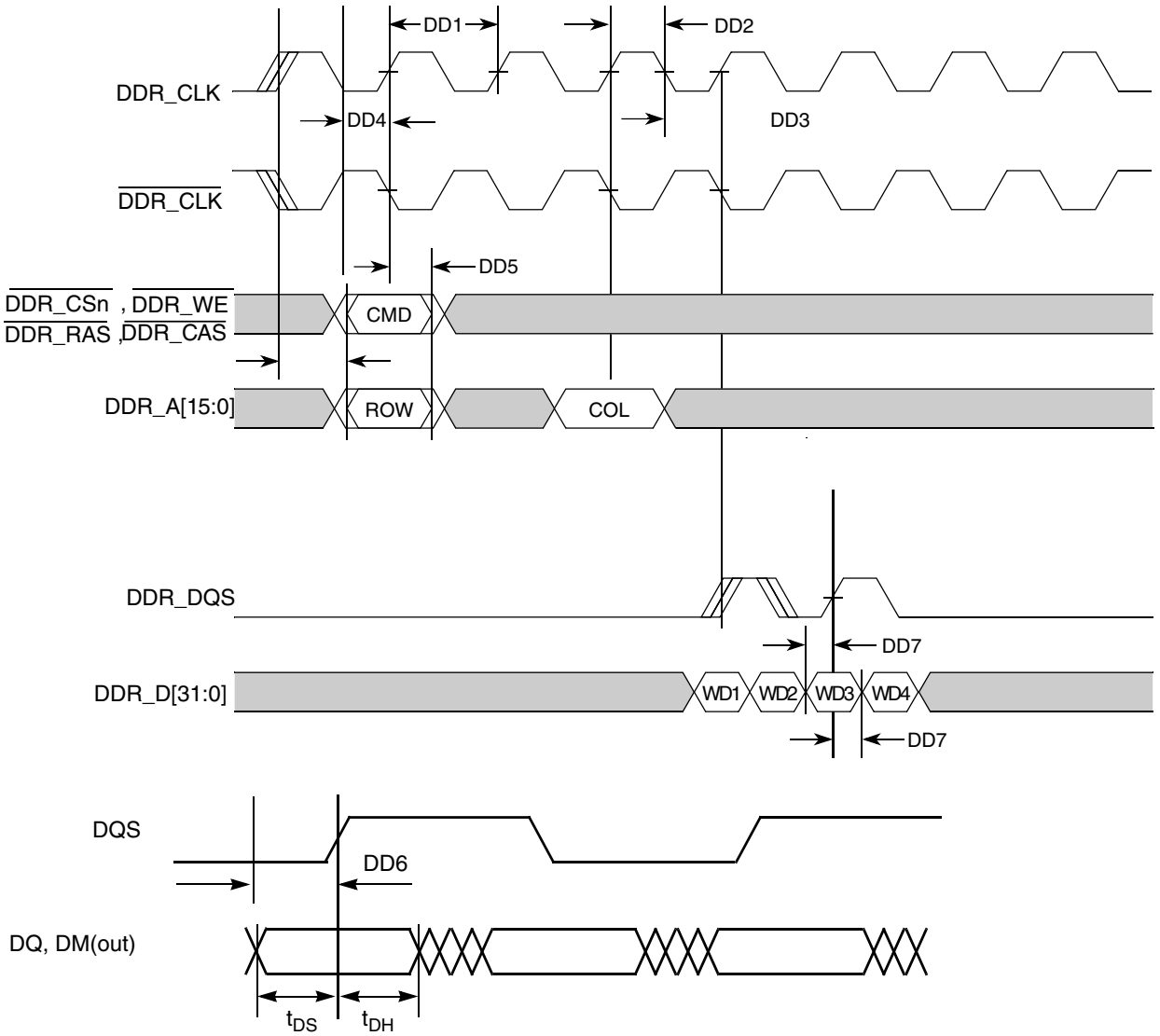


Figure 18. DDR2 write timing

Figure 19 shows the DDR2 SDRAM read timing.

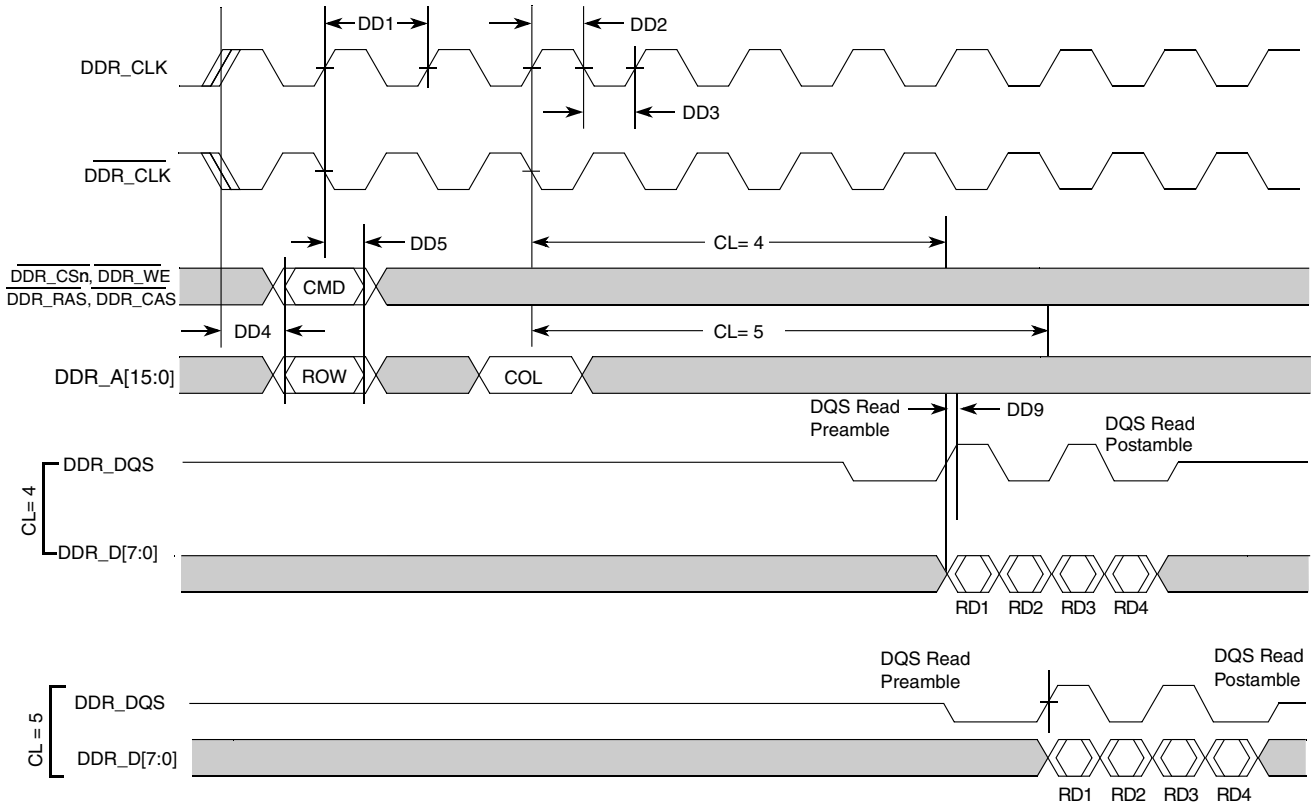


Figure 19. DDR2 read timing

6.4 Communication modules

6.4.1 SPI electrical specifications

Table 48. SPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	SPI cycle time	Master (MTFE = 0)	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2 - 1$	$t_{SCK}/2 + 1$	—	—	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	$_{SS}$ inactive to SOUT High-Z or invalid	—	25	—	—	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	—	—	ns

Table continues on the next page...

Table 48. SPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	—	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8	—	
			Master (MTFE = 1, CPHA = 1)	15	—	20	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	NA	—	–2	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	0	—	11[1]	—	
			Master (MTFE = 1, CPHA = 1)	0	—	-2	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	NA	—	7	ns
			Slave	—	15	—	23	
			Master (MTFE = 1, CPHA = 0)	—	7	—	19.5[1]	
			Master (MTFE = 1, CPHA = 1)	—	7	—	7	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	–2	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10[1]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	–2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction for high speed modes:

- Maximum of one SPI will support 40 MHz Master mode SCK
- 4 SPIs will support 20 MHz master SCK frequency.
- Maximum of one SPI will support 25 MHz Slave SCK frequency.
- **SIN**(GPIO_20, PB[4]), **DATAOUT**(GPIO_19, PB[3]), **SCK**(GPIO_27, PB[11]) groups support high frequency mode.

NOTE

For numbers shown in the following figures, see Table 48

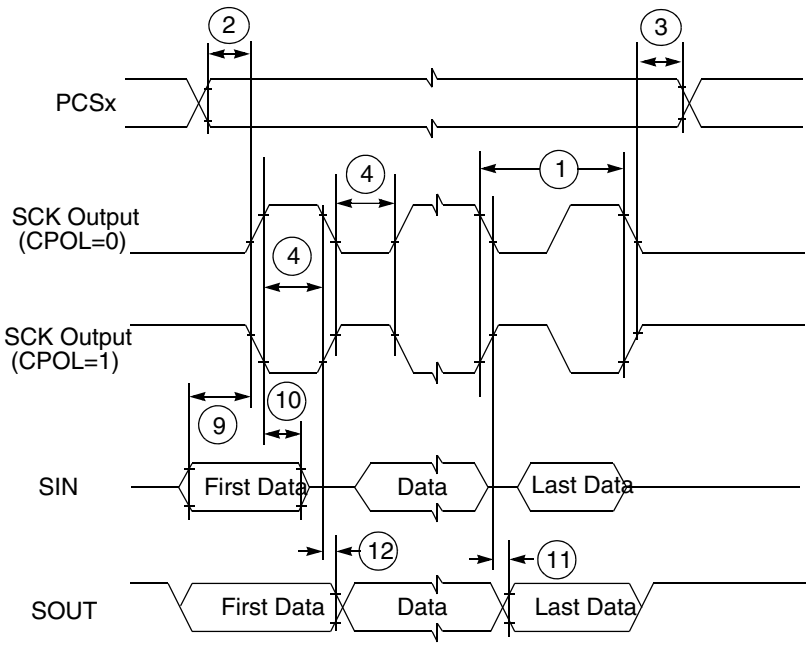


Figure 20. SPI classic SPI timing — master, CPHA = 0

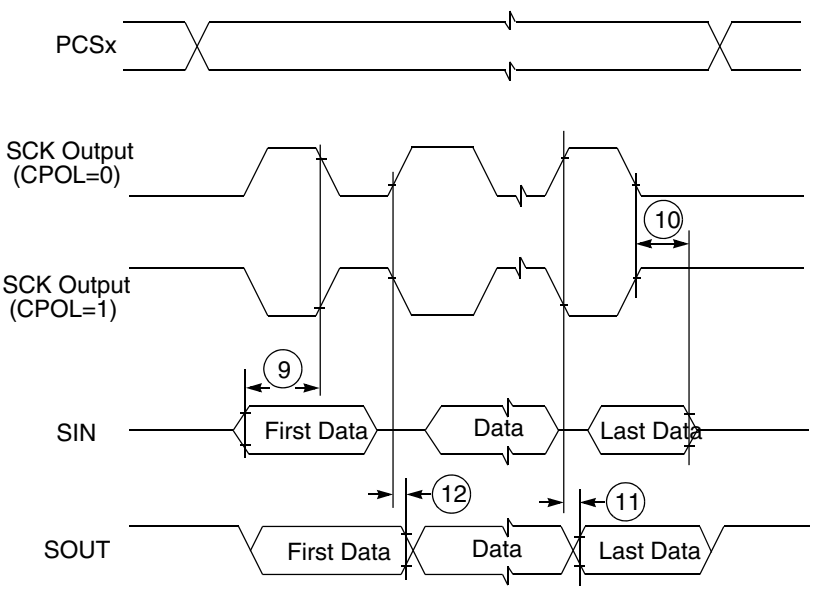


Figure 21. SPI classic SPI timing — master, CPHA = 1

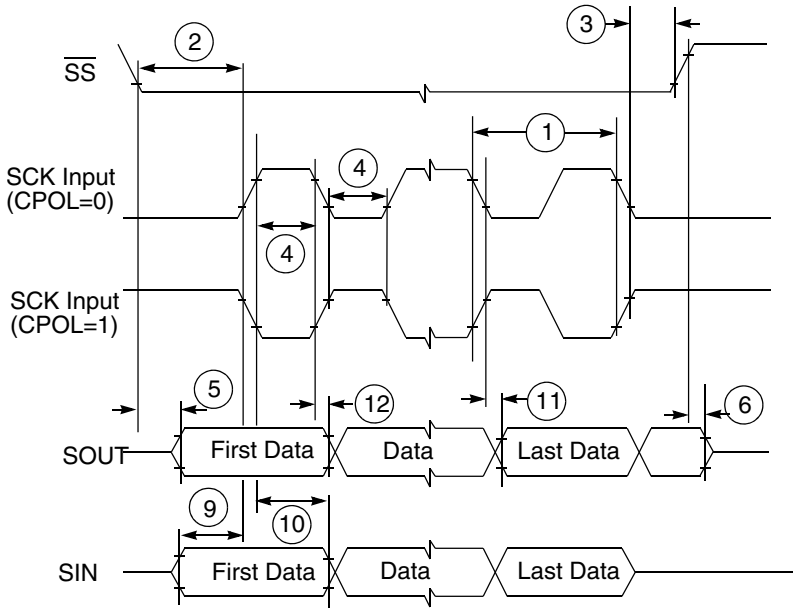


Figure 22. SPI classic SPI timing — slave, CPHA = 0

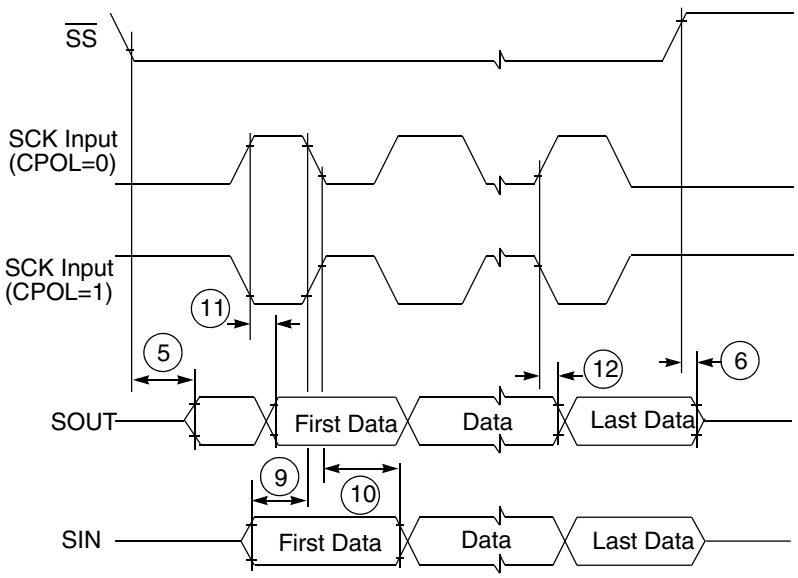


Figure 23. SPI classic SPI timing — slave, CPHA = 1

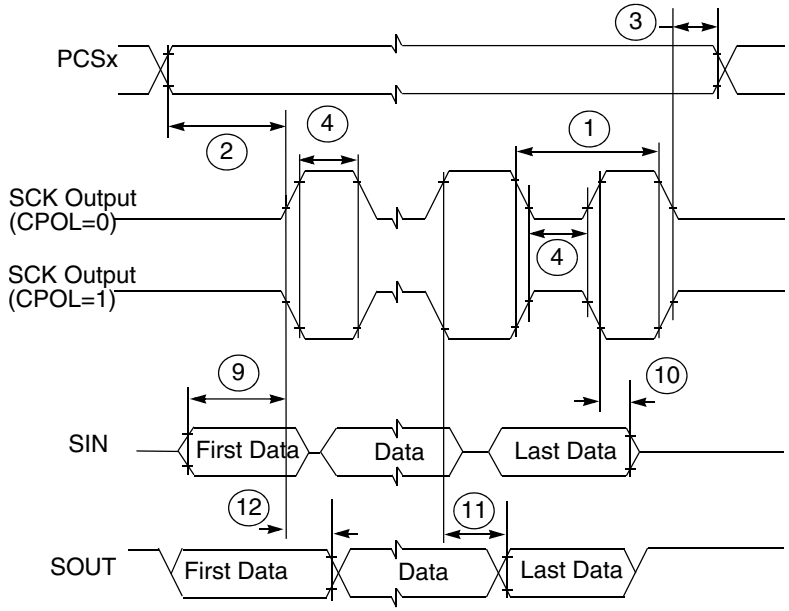


Figure 24. SPI modified transfer format timing — master, CPHA = 0

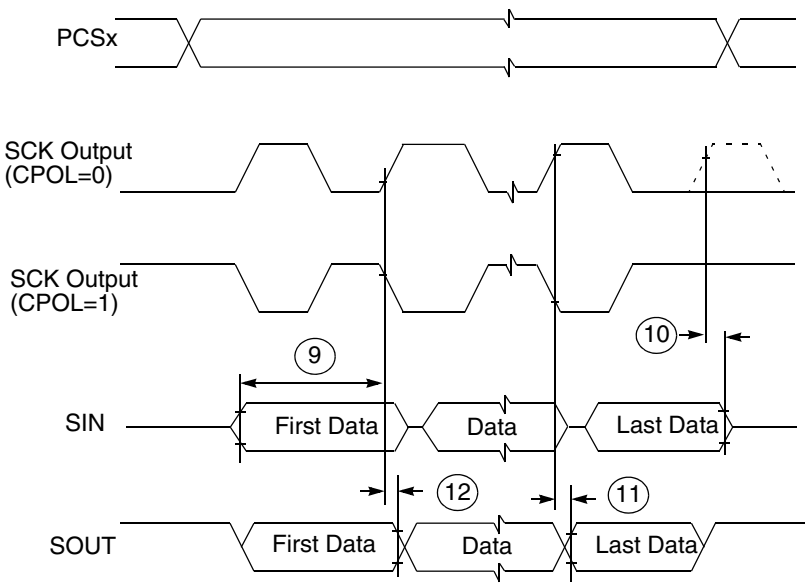


Figure 25. SPI modified transfer format timing — master, CPHA = 1

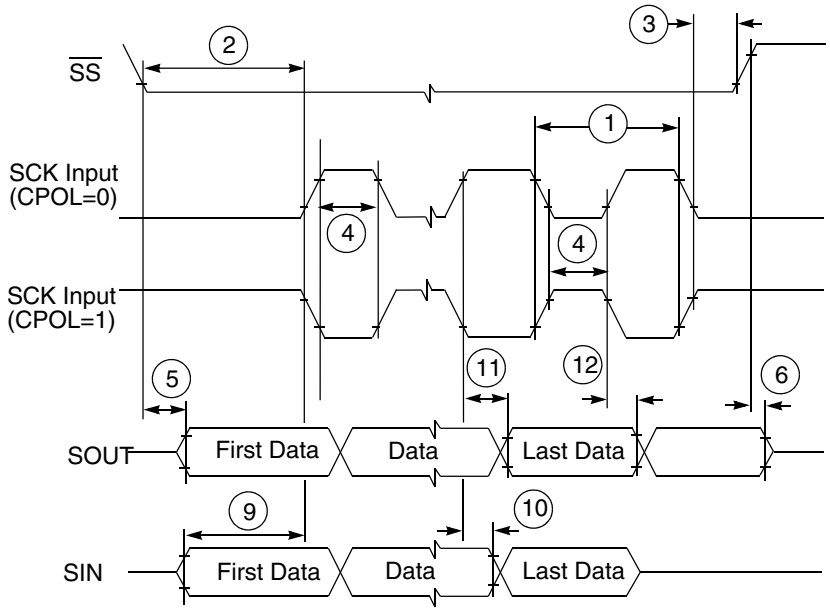


Figure 26. SPI modified transfer format timing – slave, CPHA = 0

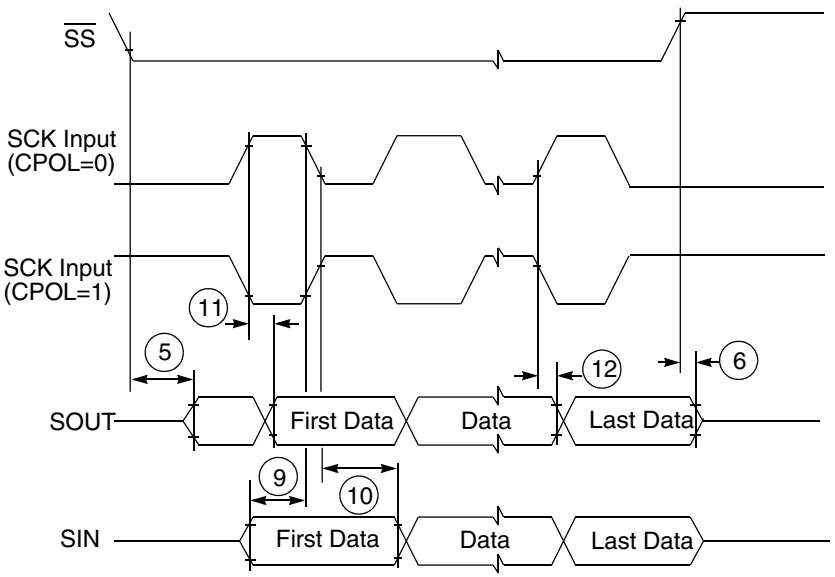


Figure 27. SPI modified transfer format timing — slave, CPHA = 1

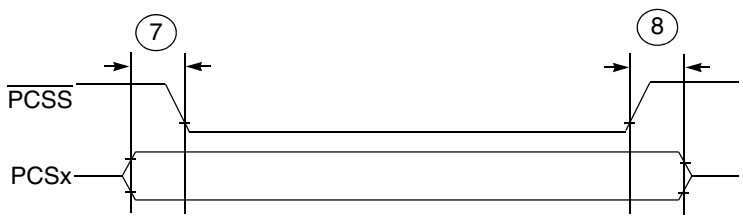


Figure 28. SPI PCS strobe (PCSS) timing

6.4.2 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.2.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 49. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

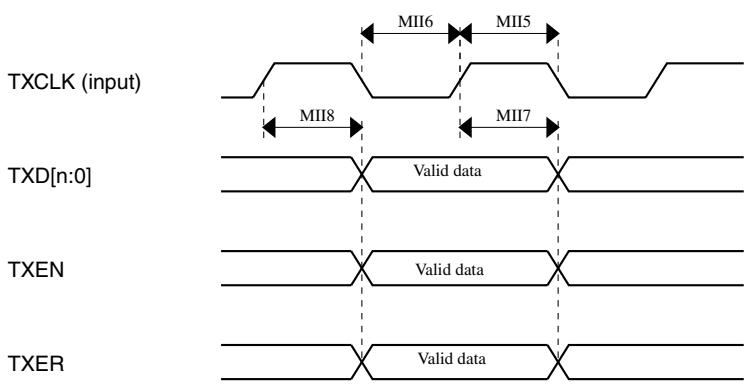


Figure 29. RMII/MII transmit signal timing diagram

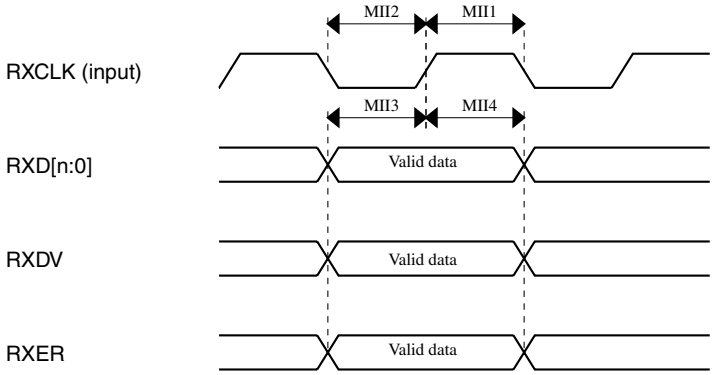


Figure 30. RMII/MII receive signal timing diagram

6.4.2.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 50. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.3 MediaLB (MLB) electrical specifications

6.4.3.1 MLB 3-wire interface DC specifications

The section lists the MLB 3-wire interface electrical specifications.

Table 51. MediaLB 3-wire interface DC specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V

Table continues on the next page...

Table 51. MediaLB 3-wire interface DC specifications (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	$_{IL}$	0 < Vin < VDD	—	±10	µA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

6.4.3.2 MLB 3-wire interface electrical specifications

This section describes the timing electrical information of the MLB module.

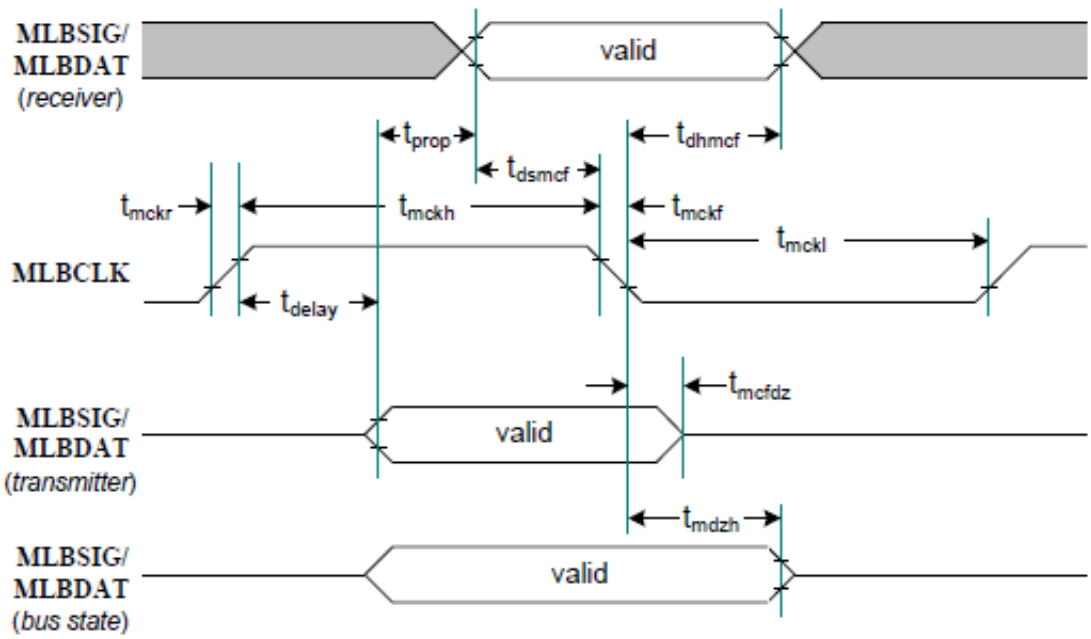


Figure 31. MediaLB 3-wire Timing

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 52. MLB 3-wire 256/512 Fs Timing Parameters

Symbol	Parameter	Min	Max	Unit	Comment
f_{mck}	MLBCLK operating frequency	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
$t_{mck}r$	MLBCLK rise time	–	1	ns	$V_{IL\ to\ V_{IH}}$
$t_{mck}f$	MLBCLK fall time	–	1	ns	$V_{IH\ to\ V_{IL}}$

Table continues on the next page...

Table 52. MLB 3-wire 256/512 Fs Timing Parameters (continued)

Symbol	Parameter	Min	Max	Unit	Comment
$t_{mck}l$	MLBCLK low time[1]	30	–	ns	256xFs
		14	–		512xFs
$t_{mck}h$	MLBCLK high time	30	–	ns	256xFs
		14	–		512xFs
t_{dsmcf}	MLBSIG/MLBDAT receiver input setup to MLBCLK falling	3	–	ns	–
t_{dhmcf}	MLBSIG/MLBDAT receiver input hold from MLBCLK low	2	–	ns	–
t_{mcfdz}	MLBSIG/MLBDAT output valid from MLBCLK low[2]	0	16	ns	256xFs
		0	12.5		512xFs[3]
t_{mdzh}	Bus output hold from MLBCLK low	2	–	ns	–

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.
3. Only 1 pair of MLB pads support 512 Fs:

   PK[11] - MLB Signal Output
   PK[12] - MLB Data Output
   PK[13] - MLB clock input

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 53. MLB 3-wire 1024 Fs Timing Parameters

Symbol	Parameter	Min	Max	Unit	Comment
f_{mck}	MLBCLK Operating Frequency[1]	45.056	–	MHz	1024 x fs at 44.0 kHz
		–	51.2		1024 x fs at 50.0 kHz
f_{mckr}	MLBCLK rise time	–	1	ns	$V_{IL\ to}\ V_{IH}$
f_{mckf}	MLBCLK fall time	–	1	ns	$V_{IH\ to}\ V_{IL}$
t_{mckl}	MLBCLK low time	6.1	–	ns	
t_{mckh}	MLBCLK high time	9.3	–	ns	
t_{dsmcf}	MLBSIG/MLBDAT receiver input setup to MLBCLK falling	3	–	ns	
t_{dhmcf}	MLBSIG/MLBDAT receiver input hold from MLBCLK low	2	–	ns	
t_{mcfdz}	MLBSIG/MLBDAT output valid from MLBCLK low	–	16	ns	
t_{mdzh}	Bus Hold from MLBCLK low	2	–	ns	

1. The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.

6.5 Display modules

6.5.1 LCD driver electrical specifications

NOTE

When using the LCD segment display module in the 208LQFP package options the V_{DDE_B} and V_{DDE_SDR} supply pins should be shorted together if LCD signal pins are used in both I/O supply domains.

Table 54. LCD driver specifications

Symbol	Parameter	Value[1]			Unit
		Min	Typ	Max	
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0], FP[m-1:0]) for output levels VLCD, VSS	-	-	10	kΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0], FP[m-1:0]) for outputs charge/discharge voltage levels VLCD2/3, VLCD1/2, VLCD1/3) [2,3]	-	2-180	-	µA
Offset	Offset of outputs with capacitive load	-	-	50 [4]	mV

1. VDD = 5.0 V ± 10%, TA = –40 to 105 °C, unless otherwise specified.
2. Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.
3. With PWR = 0-3, BSTEN = 0-1, BSTAO = 0-1.
4. 50 mV offset is only guaranteed across temperature with BSTEN=1 / BSTAO=1 up to 85ºC.

6.5.2 2D-ACE electrical specifications

6.5.2.1 Interface to TFT LCD Panels (2D-ACE)

The following figure depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 80 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

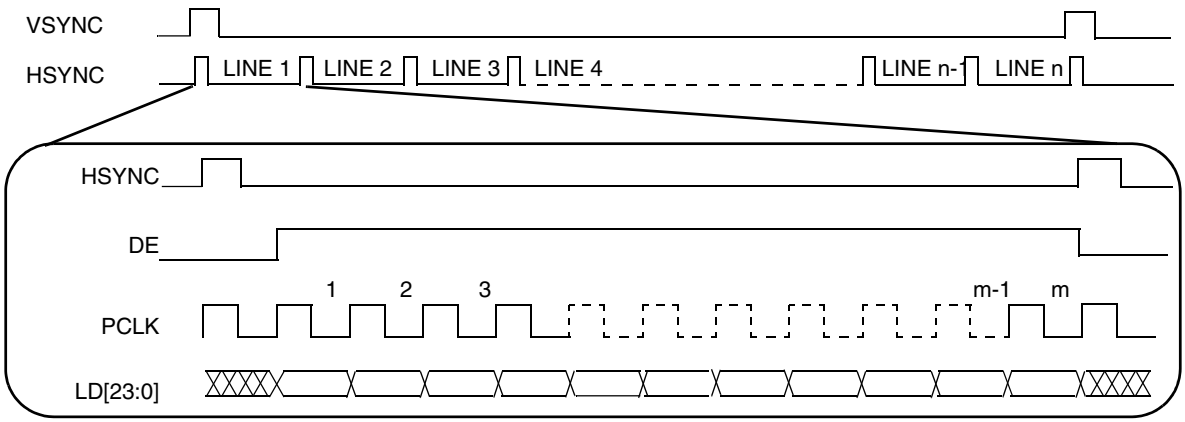


Figure 32. TFT LCD interface timing

6.5.2.2 Interface to TFT LCD Panels—pixel level timings

The following figure depicts depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high.

Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the DCU Clock Confide Register (DCCR) in the system clock module.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

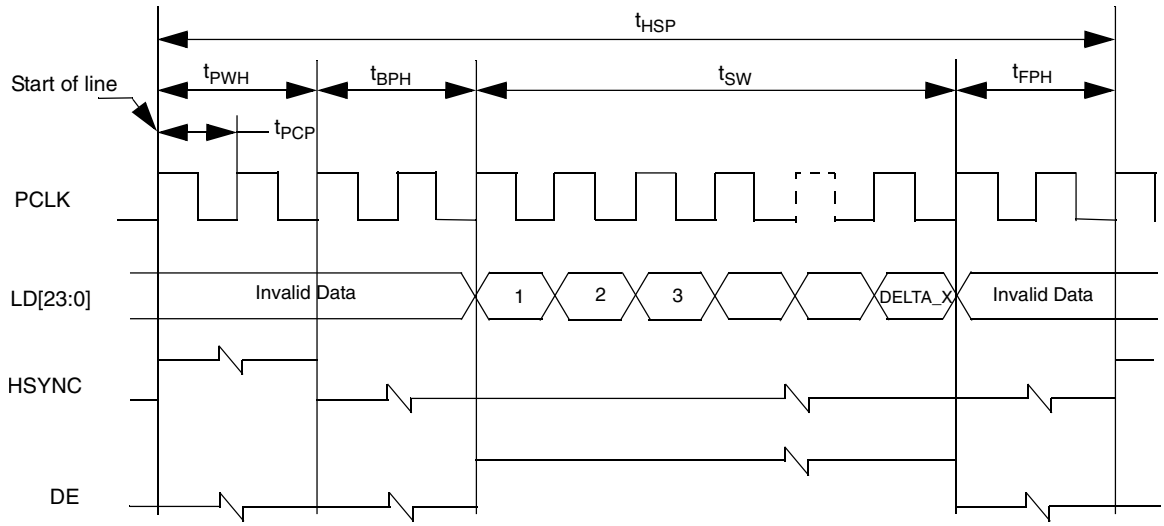


Figure 33. Vertical sync pulse

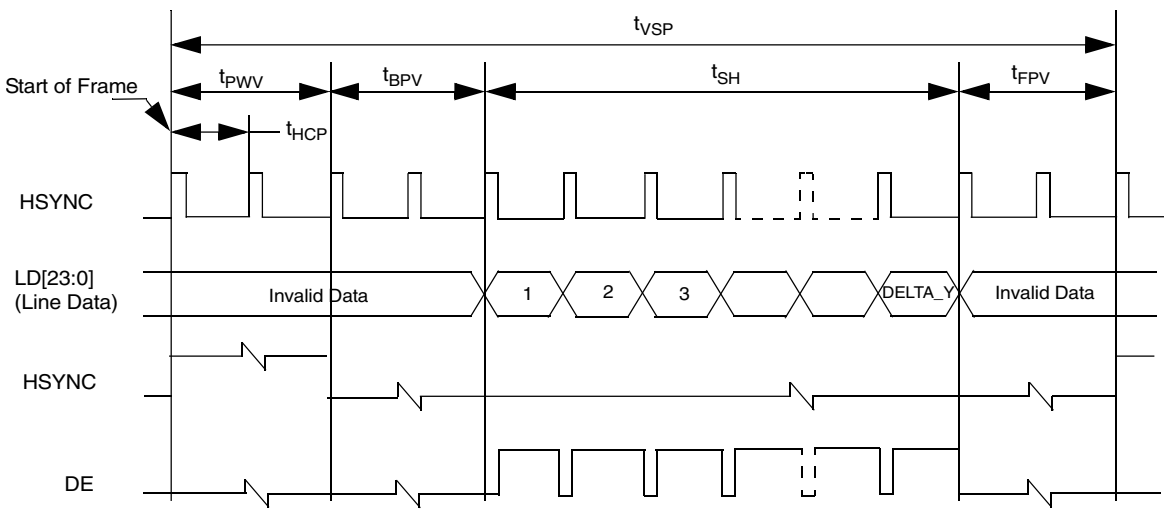


Figure 34. Horizontal sync timing

Table 55. TFT LCD interface timing parameters—horizontal and vertical

Symbol	Parameter	Value	Unit
t_{PCP}	Display pixel clock period	12.5	ns
t_{PWH}	HSYNC pulse width	PW_H × tPCP	ns
t_{BPH}	HSYNC back porch width	BP_H × tPCP	ns
t_{FPH}	HSYNC front porch width	FP_H × tPCP	ns
t_{SW}	Screen width	DELTA_X × tPCP	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) × tPCP	ns
t_{PWV}	VSYNC pulse width	PWV × tHSP	ns

Table continues on the next page...

Table 55. TFT LCD interface timing parameters—horizontal and vertical (continued)

Symbol	Parameter	Value	Unit
t_{BPV}	VSYNC back porch width	BP_V × tHSP	ns
t_{FPV}	VSYNC front porch width	FP_V × tHSP	ns
t_{SH}	Screen height	DELTA_Y × tHSP	ns
t_{VSP}	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) × tHSP	ns

6.5.2.3 Interface to TFT LCD panels—access level

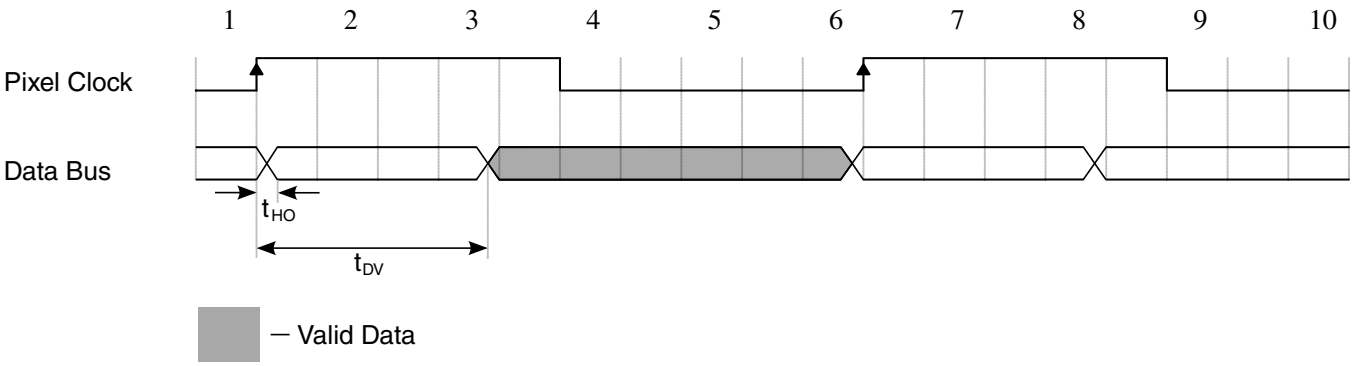


Figure 35. Display timing diagram

Table 56. Interface to TFT LCD panels—access level

Symbol	Parameter	Min	Max	Unit
T_{pix}	Pixel clock frequency	-	80	MHz
T_{DV}	Data valid after pixel clock for Data/Hysnc/ Vsync/DE	-	4.5	ns
T_{HO}	Output hold time for data and control bits	0	-	ns
T_{skew}	Relative skew between data bits	-	3	ns

NOTE

The timing diagram is on the assumption that timing path between this device and external display is full cycle.

6.5.3 Video input unit (VIU4) electrical specifications

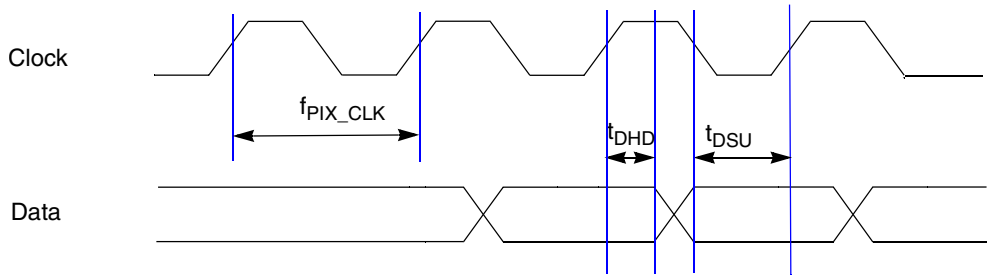


Figure 36. VIU4 timing diagram

Table 57. VIU4 timing parameters

Symbol	Parameter	Min	Typ	Max	Unit
f_{PIX_CK}	VIU4 pixel clock frequency	—	—	53	MHz
t_{DSU}	VIU4 data setup time	4	—	—	ns
t_{DHD}	VIU4 data hold time	1	—	—	ns

6.5.4 TCON electrical specifications

6.5.4.1 TCON RSDS electrical specifications

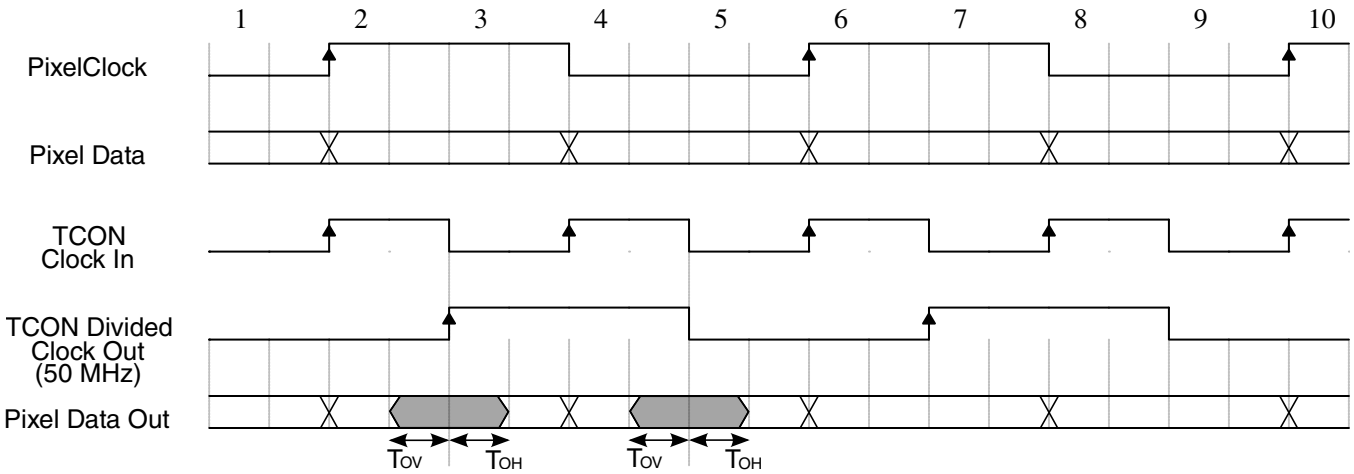


Figure 37. TCON RSDS timing diagram

Table 58. TCON RSDS timing parameters

Symbol	Parameter	Value		Unit
		Min	Max	
T_{OV}	Output data valid time	2	-	ns
T_{OH}	Output data hold time	2	-	ns

6.5.4.2 TCON TTL electrical specifications

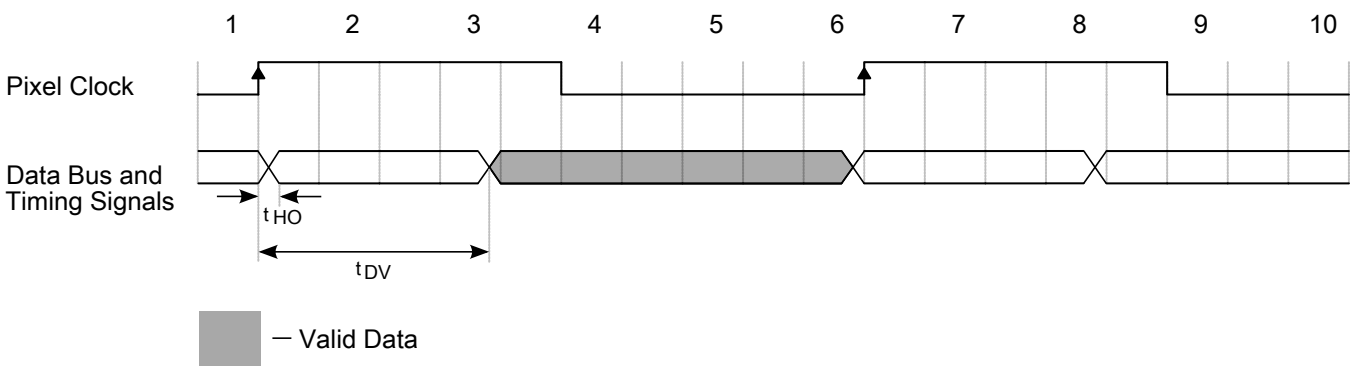


Figure 38. TCON TTL timing diagram

Table 59. TCON TTL timing parameters

Symbol	Parameter	Min	Max	Unit
T_{pix}	Pixel clock frequency	-	80	MHz
T_{DV}	Data valid after pixel clock for data and timing signals	-	5.5	ns
T_{HO}	Output hold time for data and control bits	0	-	ns
T_{skew}	Relative skew between data bits	-	3	ns

6.6 Motor control modules

6.6.1 Stepper Stall Detect (SSD) specifications

Table 60. SSD electrical specifications

Symbol	Parameter	Value[1]			Unit
		Min	Typ	Max	
V_{VREF}	Reference voltage (I_{VREF} = 0)	$V_{DDM}/2 - 0.03$	$V_{DDM}/2$[2]	$V_{DDM}/2$[2] + 0.03	V
I_{VREF}	Reference voltage output current	1.85	—	—	mA
R_{IN}	Input resistance (against $V_{DDM}/2$)	0.8	1.0	1.2	MΩ
V_{IN}	Input common mode range	V_{SSM}	—	V_{DDM}	V
SSD_{CONST}	SSD constant [3]	0.539	0.574	0.610	—
SSD_{OFFSET}	SSD offset (unipolar, N_{sample} = 1024)	–53	—	45	counts
	SSD offset (bipolar, N_{sample} = 1024)	-40	—	40	
	SSD offset (bipolar with offset cellation, N_{sample} = 1024)	-5	—	5	
f_{SSDSMP}	SSD cmpout sample rate	0.5	—	2.0	MHz

1. V_{DDM_SMD} = 5.0 V ±10%, T_j = –40 to +125 °C.
2. V_{DDM} is the voltage level of V_{DDM_SMD} supply
3. If offset cancellation is enable, OFFCNC must equal 0b01 and the integration window must be greater than or equal to 2 ms. The integration window = f_{SSDSMP} x Nsample.

6.7 Debug specifications

6.7.1 JTAG interface timing

Table 61. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.

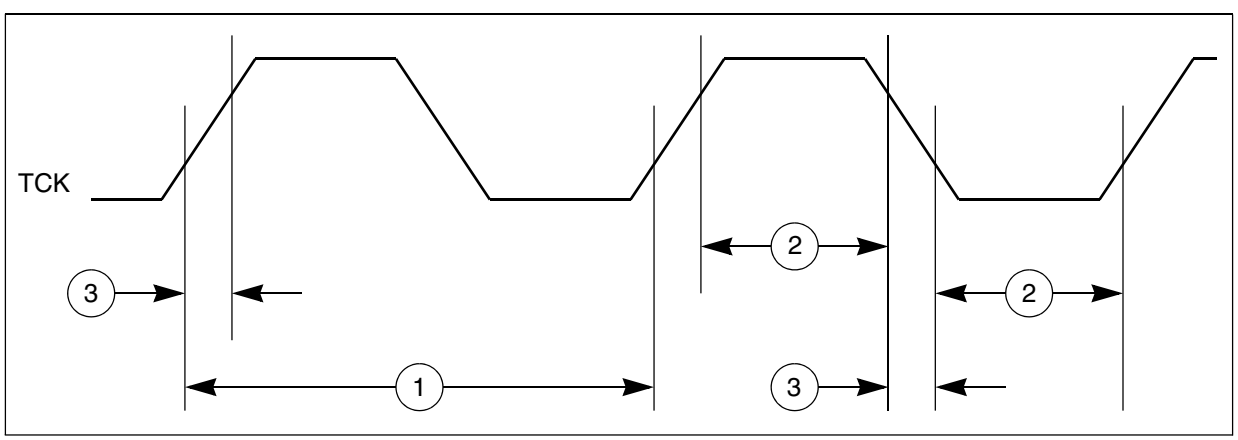


Figure 39. JTAG test clock input timing

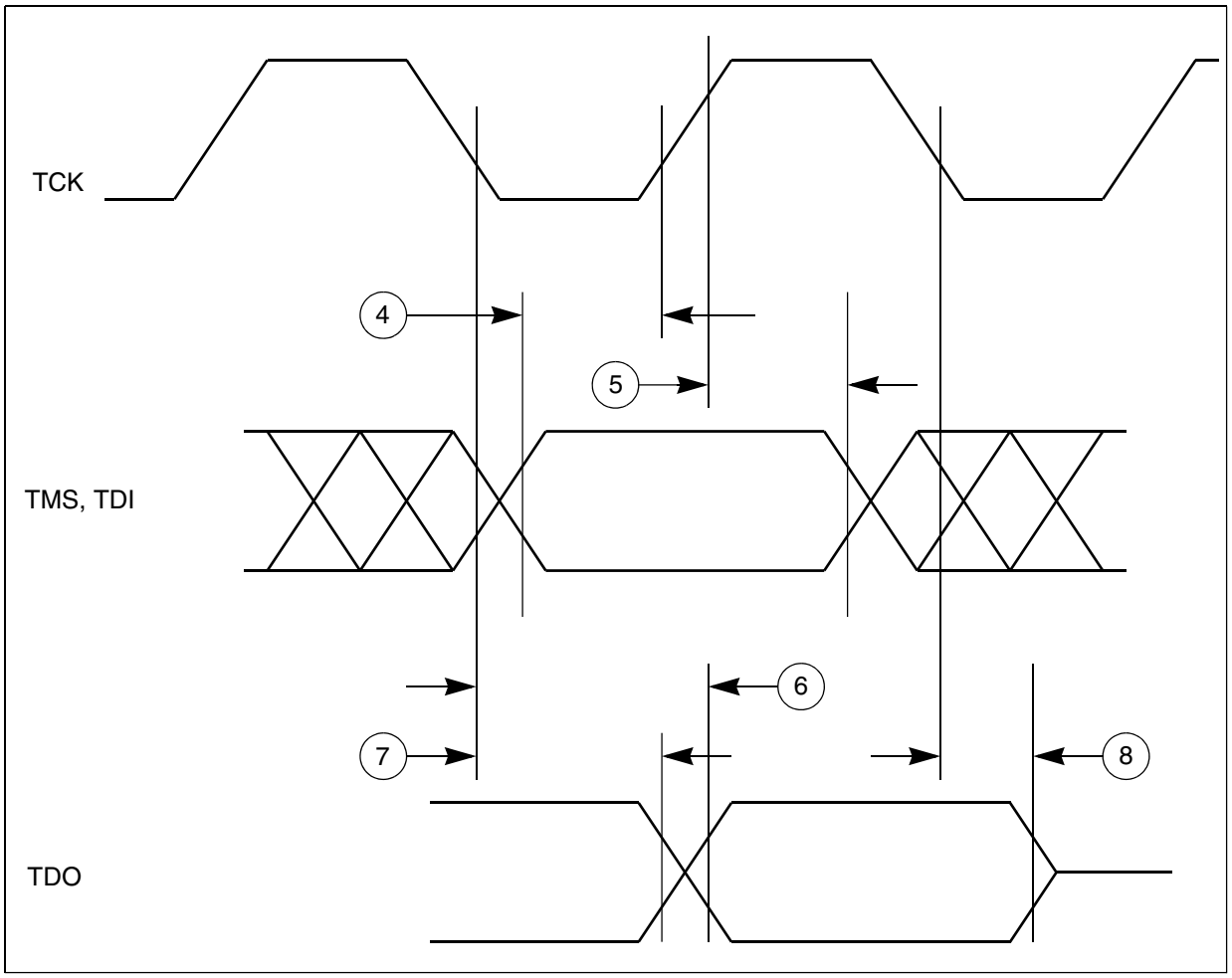


Figure 40. JTAG test access port timing

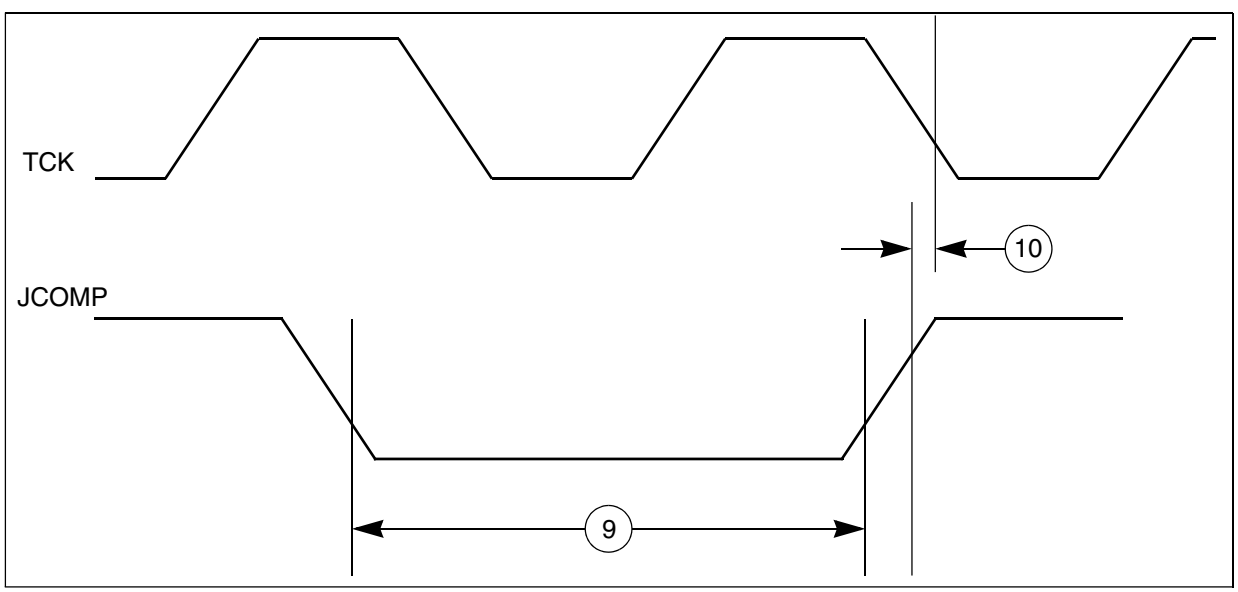


Figure 41. JTAG JCOMP timing

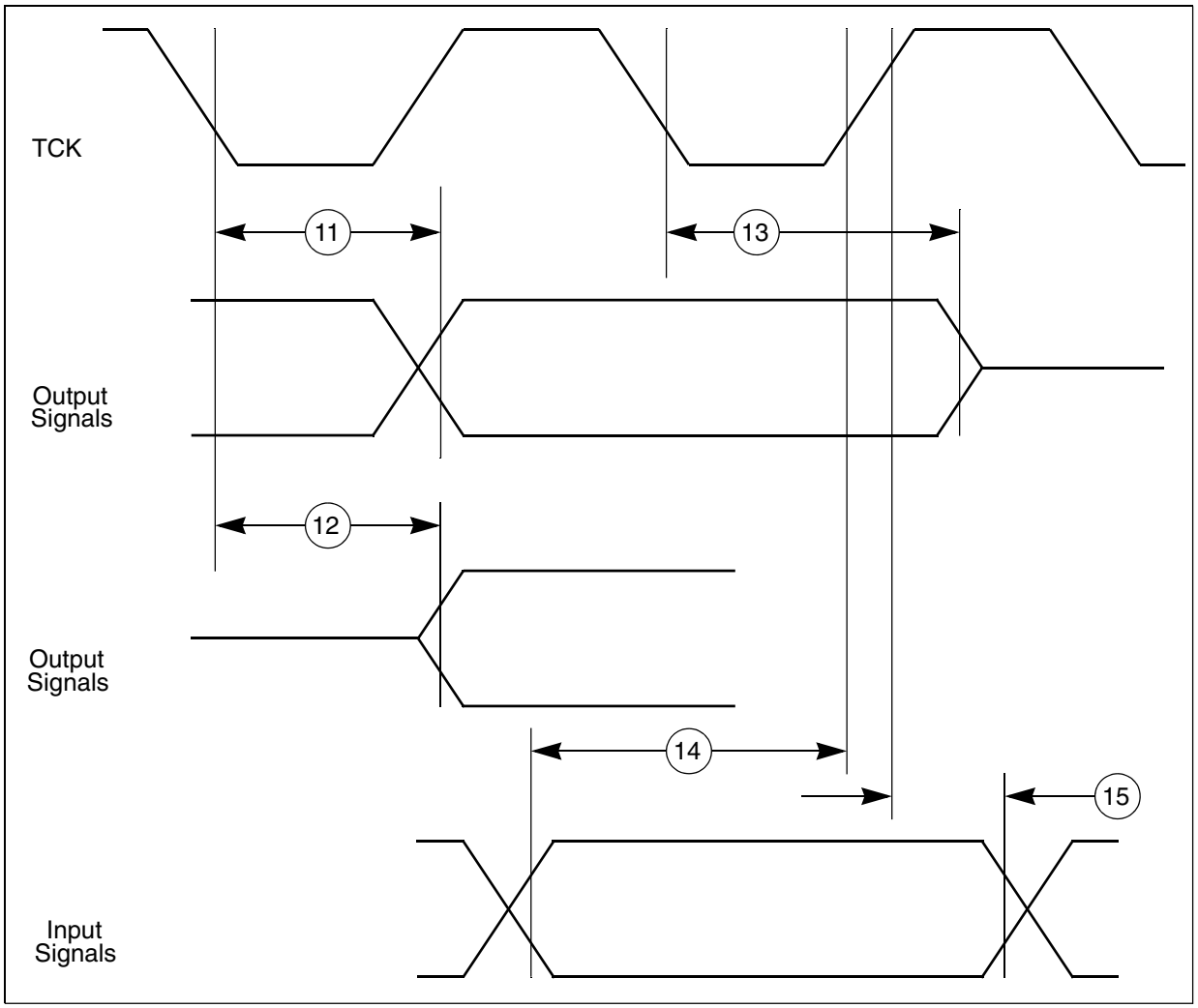


Figure 42. JTAG boundary scan timing

6.7.2 Debug trace timing specifications

Table 62. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	40		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
t_{DV}	Data output valid	7.5	—	ns
t_{HO}	Data output hold	0.5	—	ns

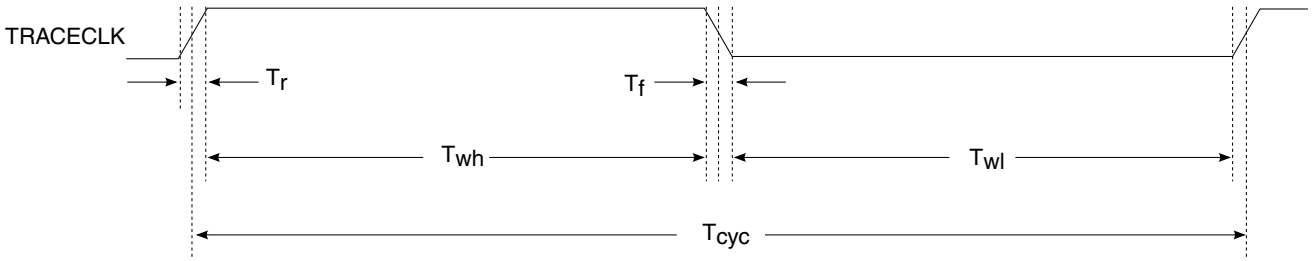


Figure 43. TRACE_CLKOUT specifications

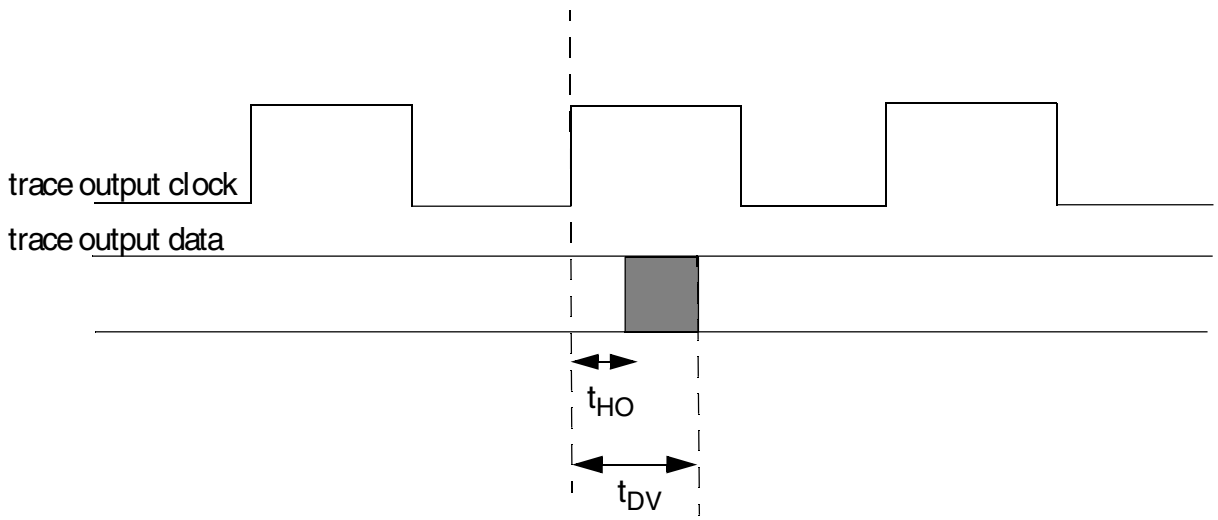


Figure 44. Trace data specifications

6.7.3 Wakeup Unit (WKPU) AC specifications

Table 63. WKPU glitch filter specifications

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_F	Pulse width that is rejected	—	—	20	ns
2	W_{NF}	Pulse width that is passed	400	—	—	ns

6.7.4 External interrupt timing (IRQ pin)

Table 64. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time	—	6	—	t_{CYC}

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

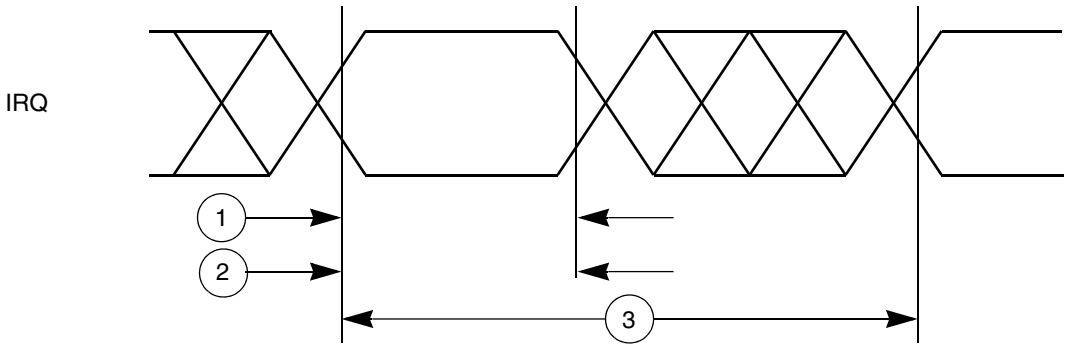


Figure 45. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	208LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.1	°C/W	1,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	16.4	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	12.4	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	12.4	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	7.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	5.3	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	6

Table continues on the next page...

Board type	Symbol	Description	208LQFP	Unit	Notes
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package. With provided Theta-JB, Max junction temperature must be 125 degreeC.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

Board type	Symbol	Description	516MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	23.2	°C/W	1,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	16.2	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	15.9	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	12.2	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	7.0	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	3.7	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.1	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	2.7	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package. With provided Theta-JB, Max junction temperature must be 125 degreeC.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package	Body Size	Pitch	NXP Document Number
208 LQFP	28 mm x 28 mm	0.5 mm	98ASA00649D
516 MAPBGA	27 mm x 27 mm	1.0 mm	98ASA00623D

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 65. Revision History

Rev. No.	Date	Substantial Changes

6	22 Nov 2016	• In Voltage monitor electrical specifications table, updated $V_{LVD\_IO\_A\_LO}$ fall trimmed values 'Typ' and 'Max' to 3.0260 V and 3.0750 V respectively.
		• In Recommended operating conditions table,
		  • removed the phrase, "Design may experience up to 30 mA.....additional current.
		• In Flash memory program and erase specifications changed symbols for specifications:
		  • Quad-page (1024 bits) program time: Changed symbol from t_{qppgn} to t_{qppgm}
		  • 16 KB Block program time: Changed symbol from t_{16kpgn} to t_{16kpgm}
		• In Flash memory AC timing specifications for t_{psus}:
		  • Changed Typical from 7 µs plus four system clock periods to 9.4 µs plus four system clock periods
		  • Changed Max from 9.1 µs plus four system clock periods to 11.5 µs plus four system clock periods

5	05 May 2016	• Updated part number from MAC57D5xx to SAC57D5xx throughout the document.
		• Changed the term 'Freescale' to 'NXP':
		  • In Determining valid orderable parts : web link address changed to NXP
		  • In Electromagnetic Compatibility (EMC) specifications : changed Freescale to NXP.
		• Removed CAN-FD references from:
		  • system connectivity row of Table 1,
		  • communication bullet in "Features".
		• In the feature list, removed the phrase 'using external ballast transistor' from 'External 3.3 V input supply'.
		• Removed reference to 176 LQFP package from the following sections:
		  • Table 1
		  • Ordering information
		  • LCD driver electrical specifications
		  • Thermal attributes
		  • Obtaining package dimensions
		• In Recommended operating conditions,
		  • removed phrase, "....and internal regulator cannot be used if peak application demand is more than 800 mA".
		  • added a phrase, 'Design may experience up to 30 mA.....additional current'.
		• In Voltage regulator electrical specifications,
		  • removed VRC_CTL and all connection to FPREG, RC_BALLAST and HDD_HV_BALLAST related content in the Voltage regulator capacitance connection figure and Voltage regulator electrical specifications table,
		  • removed VDD_HV_BALLAST options section,
		  • updated Recommended decoupling capacitor values.
		• In Table 5,
		  • removed 'V_{LVD_FLASH}' and 'V_{LVD_FLASH} during low power mode using LPBG as reference' parameters.
		  • updated $V^{HVD\_LV\_cold}$ fall trimmed typical value.
		• In Power consumption section,
		  • updated Table 6 for standby current specs for 25°C,
		  • removed VDDE_B supply name from footnote 5,
		  • removed figure, "3.3 V Vreg Supply, External Ballast. DDR2, Mixed 3.3 V / 5 V IO",
		  • renamed Figure 4 title from '1.2 V External Supply, DDR2, Mixed 3.3 V / 5 V IO' to 'Supply configuration', removed VRC_CTL block from the figure.
		• In Table 11, added Vol and Voh specs.
		• In Table 13 updated $I_{oh(dc)}$ and $I_{ol(dc)}$ minimum values.
		• In Table 17, removed 'Vsum', 'Voh delta / Vol delta', 'Rdsonh' and 'Rdsonl' parameters.
		• Removed the column for 'Prop. Delay' parameter from the following tables:
		  • Table 8
		  • Table 10
		  • Table 12

Table continues on the next page...

Table 65. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Table 16 • Table 18 • Removed reference to 5V Typ and 5.5V max in Table 19 and Table 20. • In Table 24, • updated min and max values for 'INL' parameter. • removed '5V Reference Voltage' row in I_{DAC6b} parameter. • In Table 28, • updated 'Temp Dependence' value as 600 ppm/C, • updated 'Supply Dependence' as 18%V, • updated 'Oscillator Frequency' as 119 KHz (min) and 136.5 KHz (max), • added 'Supply Current (Run)' as 2.75 uA and 'Supply Current (Stop)' as 200 nA. • In Table 27, updated T_{STJIT} value to '1.5%' and T_{LTJIT} value to '0.2%' • In Table 29 updated Modulation Depth (Center Spread), max value updated to +/- 3.0%. • In SDR AC specifications, • added note, 'All transitions measured at mid-supply .....with EMC improvement'. • added footnotes for DD1 and DD2 specs of Table 45 and Table 46 that these parameters also apply to command and address buses. • In Table 47, updated DD2 and DD3 values and unit. • In Table 54, in footnote 4, added phrase '..up to 85ºC'. • In Table 55 updated 'Display pixel clock period' (tPCP) value to 12.5 ns. • In Table 60, updated the values for all parameters of SSD_{OFFSET} and added footnote 3.
4	17 Jun 2015	• In "Recommended operating conditions", removed phrase, "V_{DDE_A} (4.5 V to 5.5 V) configuration is only supported in 176 LQFP". • In "LVDS pads electrical specifications", • V_{dde} parameter, updated foonote, from "V_{DDE} is the V_{DDE_OLDI} supply" to "V_{DDE} is the V_{DDE_B} supply" • "Differential o/p voltage" parameter, added foonote, "The limit applies to the default drive current". • "Rise/Fall time" parameter, added footnote, "Rise/fall time is assumed to be measured with 20%-80% levels". • In "Analog Comparator (CMP) electrical specifications", updated min V_{AIO} from -35 mV to -42 mV and max V_{AIO} from 35 mV to 42 mV. • Editorial changes in "Memory Interfaces" section. • In "QuadSPI electrical specifications", • updated table title from "QuadSPI delay chain read/write settings" to "QuadSPI read/write settings" and revised the content. • revised notes in the "SDR mode" section. • "QuadSPI input timing (SDR mode)" diagram, renamed SFCK to SCK • "QuadSPI output timing (SDR mode)" diagram, renamed SFCK to SCK • "QuadSPI input timing (SDR mode) specifications" table, added "$F_{SCK"}$ parameter • removed notes in the "DDR mode" section. • added new table, "QuadSPI input timing (DDR mode) specifications with learning". • "QuadSPI output timing (DDR mode) specifications" table, removed "T_{ck} ". • "QuadSPI output timing (Hyperflash mode) specifications" table, renamed "T_{dvMAX}" to "T_{DVO} ". • In "SDR AC specifications", • SDR @ 160 MHz AC timing specification table, moved value of t_{SDCK} from Min to Typ • SDR @ 80 MHz AC timing specification table, moved value of t_{SDCK} from Min to Typ • In "DDR2 SDRAM AC specifications", added a note, "If self-refresh mechanism needs to be supported, an external pull-down resistance needs to be connected to the DDR CKE pin". • Revised "TCON RSDS timing diagram" • In "TCON RSDS timing parameters" table, updated T_{DS} to T_{OV} and updated T_H to T_{OH}.
3	13 March 2015	• Updated High Level Block Diagram • Updated Family Comparison table • In Absolute maximum ratings table

Table continues on the next page...

Table 65. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed Vss and Tj spec. Added footnote, "Tj=125°C. Assumes Ta=105°C. Assumes maximum θ_{JA} of 2s2p board. See Thermal attributes section for details." Updated description of VINA spec. • Removed VDD_HV_FLA parameter. • In Recommended operating conditions section, added the following paragraph: The following table describes .... in the given range. • In Recommended operating conditions (VDDE_x = 3.3 V) • removed the footnote "This supply should be shorted on board with VSSA.V_{DDA_REF} Min voltage changed to 3.15V from -3.15V • Recommended operating conditions (VDDE_x = 5 V) table: • Clarified parameter description for several paramters • Removed Vss • VSSEH_ADC: Updated min to -0.1 and max to 0.1V. • Added footnote: All parameters are with reference to Vss, unless otherwise specified. • Added Tj condition in the footnote. • Added a footnote in VDD12 pin description in Recommended operating conditions (VDDE_x = 3.3 V) table: VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating. • In Voltage regulator electrical specifications section, • Changed the text "Supports up to 800 mA load internal generation of the 3.3 V flash supply when device connected in 5 V applications" into following bullet: • Supports up to 800mA current (on VDD12 supply) when using external NPN ballast transistor for generating core supply • Updated Voltage regulator capacitance connection figure to remove Flash voltage regulator, VDD_HV_FLA and CFLASH_REG • In block description, changed low range to low threshold and high range to high threshold. In Voltage regulator electrical specifications table, added Combined ESR of external capacitor parameter for C_{lp/ulp_reg}. Added a foonote in the C_{flash_reg} • Added VDD_HV_BALLAST options section In Voltage monitor electrical specifications table, • Updated parameter description to remove the term internal/external from LV supply. • Removed VLVD_IO_A_HI parameter, added parameter description for "VLVD_FLASH during low power mode using LPBG as reference", in footnote 3, renamed VDD_HV_FLA to flash HV supply. In Power consumption table, • removed reference to "5 V Vreg Supply, External Ballast, 5 V only IO" figure, updated 3.3 V Vreg Supply, External Ballast. DDR2, Mixed 3.3 V / 5 V IO figure and 1.2 V External Supply, DDR2, Mixed 3.3 V / 5 V IO figure.
3 (continued)	13 March 2015	• In DC electrical specifications @ 3.3 V Range, • Updated Pull_Ioh with Pull_Ioh_vil_hys data and its values, updated Pull_Iol with Pull_Iol_vil_hys data and its values • In DC electrical specifications @ 5 V Range, • Updated Pull_Ioh with Pull_Ioh_vil_hys data and its values, updated Pull_Iol with Pull_Iol_vil_hys data and its values • In DDR2 pads AC electrical specifications at 1.8V V_{DDE_DDR},added reference to SIUL_MSCR[SRE] in the Drive Strength Select cell. • In RSDS pads electrical specifications, updated Data rate TYP and MAX to 50 MHz, added Tskew value

Table continues on the next page...

Table 65. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In LVDS pads electrical specifications, updated Rise/Fall time specification for open LDI LVDS pads from 1.5 ns to 800 ps.
		• In ADC conversion characteristics (for 12-bit) table,
		  • renamed TUEIS1WINJ to TUE for precision channels
		  • added parameter name as Trecovery for STOP mode to Run mode recovery time
		  • added parameter - ADC Analog Pad
		  • aded Total unadjusted error with current injection
		  • removed footnote in "Conditions" column
		• Revised the whole section "Comparator and 6-bit DAC electrical specifications table"
		• In Fast Oscillator electrical characteristics table, removed FOSC VIH/VIL Min and Max spec and replaced with TYP specs: VIH as 1.84V, VIL as 1.48V .
		• In Fast internal RC Oscillator electrical specifications table, removed $F_{Untrimmed}$ spec
		• In Slow internal RC oscillator electrical specifications table, removed F_{oscu} spec.
		• Revised PLL electrical specifications table
		• Revised the whole section "Flash Read Wait State and Address Pipeline Control Guidelines"
		• In LCD driver electrical specifications, added offset, $I_{BP/FP}$, $Z_{BP/FP}$
		• In 208LQFP and 516BGA thermal attribute tables, for RθJB updated footnote to add, "With provided Theta-JB, Max junction temperature must be 125 degreeC".

3 (continued)	13 March 2015	• Revised Voltage monitor electrical specifications • Revised Voltage regulator electrical specifications • Revised Power consumption specifications • Revised SSD electrical specifications • Updated SAR-ADC electrical specifications by providing values for both 12-bit and 10-bit modes • Revised QuadSPI, VIU and TCON specifications • Updated Debug trace operating behaviors • Renamed VDD_0P9_DDR to DDR_VREF throughout the document
2	20 May 2014	• Updated device part number to MAC57D54H • "Feature list", updated Program and Data Trace support from "32-bit" to "16-bit" • Updated block diagram, added detailed block diagram. • Revised "Feature Sets" table. • Removed parameter classifications throughout the document. • Revised "Ordering information" section. • Removed "Key electrical parameter" section. • Revised "Absolute maximum ratings" table. • In the "Recommended operating conditions (V_{DDE_x} = 3.3 V)", revised note, added VDDA_REF, updated footnote with VDD_HV_FLA. • In the "Recommended operating conditions (V_{DDE_x} = 3.3 V)", revised note, added VDDA_REF, updated footnote with VDD_HV_FLA. • Added Voltage monitor electrical specifications
2 (continued)	20 May 2014	• In the "Voltage regulator electrical specifications", renamed VDD_PMC to VDDE_A, removed $C_{HV\_VDD\_A}$, C_{HV_ADC}, C_{HV_ADR}, added a new section, "Recommended decoupling capacitor value". • In the "Voltage monitor electrical specifications", updated V_{LVD_FLASH} configuration and threshold. • In the "Power consumption" table, updated Target Typ and Target Max for IOP Run Mode, IOP Stop Mode, Standby Mode. Added footnote for Standby Mode parameter. • Added note below Figure 6. • Revised "Electromagnetic Compatibility (EMC) specifications". • In the "Functional Pad AC Specifications @ 3.3 V Range table", added recommended settings, removed asymmetry drive load, added footnote: "Auto levels are applicable only to the ADC pins" • In the "DC electrical specifications @ 3.3 V Range table", removed footnote showing ramp rate.

Table continues on the next page...

Table 65. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In the "Functional Pad AC Specifications @ 5 V Range table", added recommended settings, removed asymmetry drive load. • In the "DDR2 pads AC electrical specifications at 1.8 V VDDE_DDR table",updated Prop. Delay (ns) L>H/ H>L. • In the "SSTL_18 Class II 1.8 V DDR2 DC specifications table", updated VDD12, removed JESD8-15 A notes from V_{DD0P9_DDR}. • In the "SMC 5 V IO DC specifications", added R_{dsonh}, R_{dsonl}. • In the "SMC 5V pads IO AC specifications", updated pad_smc_io _hv values. • In the "SMC 3.3 V pads IO DC specifications", added R_{dsonh}, R_{dsonl} • In the "SMC 3.3 V functional pads IO DC specifications", updated pad_smc_io _hv values.
1	30 Jan 2014	• Updated family comparison table • Updated Ordering information • Updated Absolute Maximum Ratings and Recommended Operating Conditions tables • Updated Power consumption table • Revised parameter classifications in several tables • Updated Main oscillator electrical characteristics table • Added DDR2 Read timing figure in the DDR2 SDRAM AC specifications section and revised the parameter values • Updated QuadSPI Input timing (RPC mode) table

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