INTRODUCTION

High-reliability DC power distribution system normally consists of several DC power supplies with each output connected in parallel to the system load bus. These power converters may come with current sharing and/or hot-swapping circuit but each of them will have a common basic feature that is output fault isolation. Passive solution using Schottky diodes becomes a popular choice before, but due to ever increasing load current demand, the power loss due to its forward voltage drop becomes significantly high which requires separate thermal management and additional cost.

With the introduction of the active OR-ing as a more efficient scheme for fault isolation, the use of low Rds-on mosfet(s) and discrete solution for gate drives has become a more attractive solution.

GENERAL DESCRIPTION

This Active OR-ing demo board is an evaluation kit which aims to demonstrate the functionality of the IR5001 OR-ing controller IC by driving 4 low-Rds-on 20V N-channel mosfets (IRF6609 DirectFETs as OR-FETs) connected in parallel. Its basic circuit is intended for use as a simple and efficient means of providing the OR-ing function by actively linking the positive side of individual 12-Volt power converter to the system bus and output fault isolation during short circuit condition of any of the power source.

The board is tested for 65 – 100 Amp max and requires a floating 12Volt dc supply to power up the IR5001 IC. It is equipped with normally-open microswitch for FETCHK function. This switch is intended to check manually the output status of the IC controller as well as giving the user a quick way of knowing if there is an abnormality on the board itself, such as bad mosfets (please refer to Table1).

SPECIFICATION

1. **Fast Reverse polarity sensing of IR5001 OR-ing Controller IC**
2. **IC's gate drive capability of $3A_{pk}$**
3. **Low dissipation of IRF6609 Low-Rds-on (2mOhm) DirectFET (OR-FETs)**
4. **Highside implementation (positive rail) of OR-ing function capable of handling continuous 65-100Amp max in a 12Volt system**
5. **Less than $10A_{pk}$ reverse current during short circuit.**
6. **With FETCHK feature (for quick checking of IC output and OR-FETs functionality)**

Figure1A. Front side of the IRAC5001-HS100A Demo Board

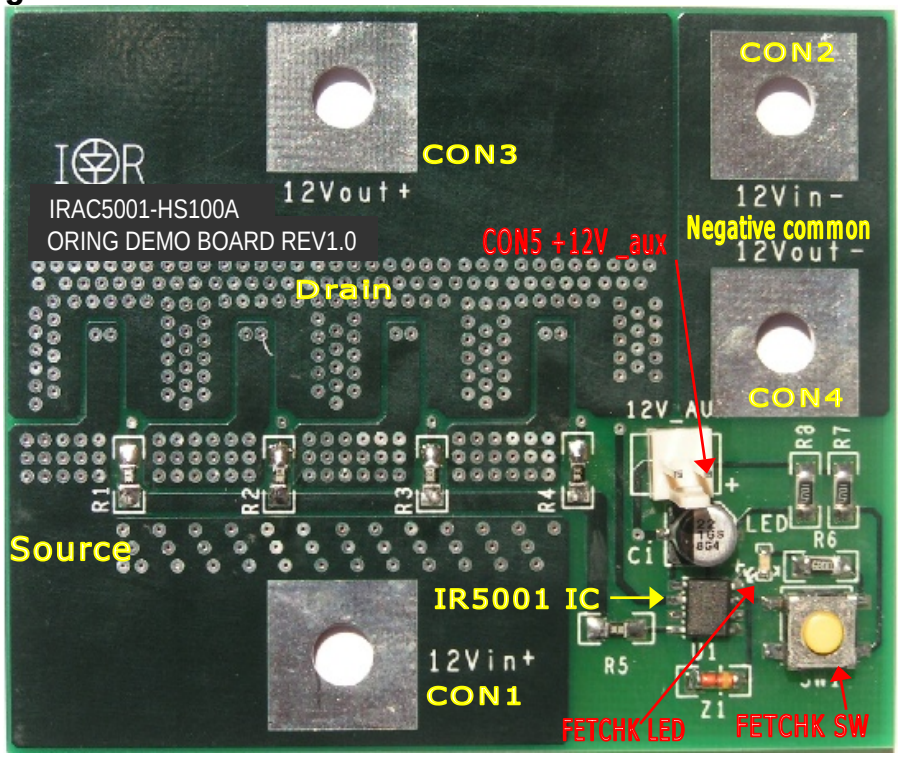
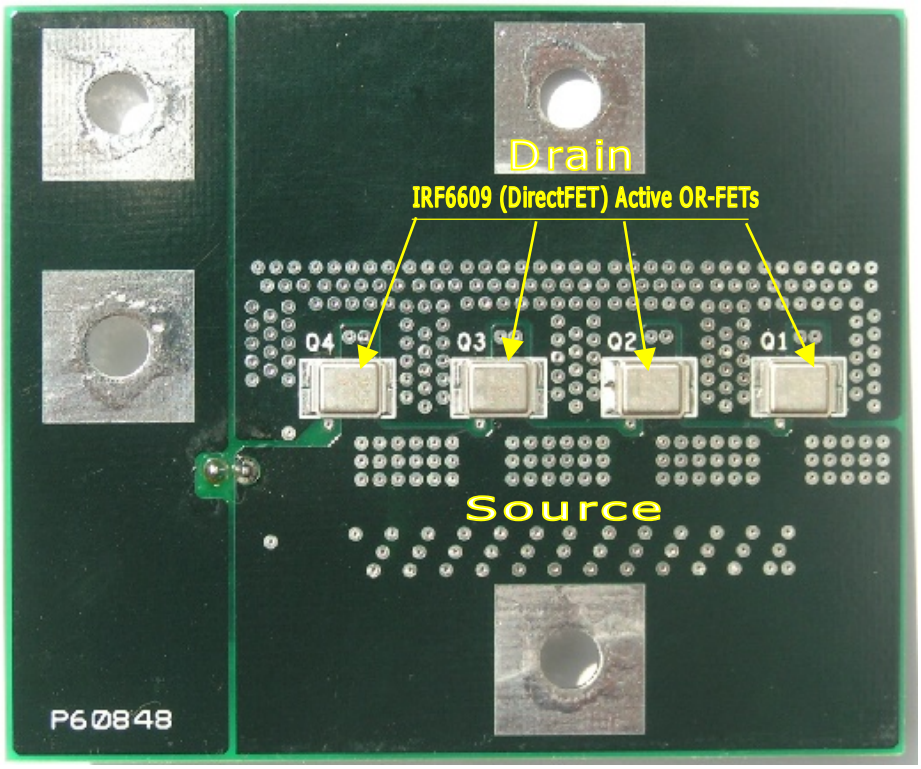


Figure1B. Back side of the IRAC5001-HS100A Demo Board



CIRCUIT OPERATION :

The diagram in Figure 2 shows the test setup to evaluate the functionality of this demo board in each of 12Volt power supply output connected to the system bus load.

The power load can be a single high power E-load (~1kW) or composed of several medium power E-loads (3 x 300W) connected in parallel. At least 2 units of high power converter - each capable of sourcing 100Amp is required to check the OR-ing functionality. Each power supply should have an output voltage setting of about 12V (+/- 0.01 V) to simulate a near balanced current sharing condition, and each output is link to the bus by one demo board- individually powered by a floating 12Volt DC supply (bias voltage) through connector CON5. This connector route the positive bias voltage to the IC's pin 7 (Vcc : < 13.9Vmax) and the negative bias to the output rail connector (Con1) of the power converter. This is necessary to drive the gates of 4 IRF6609 OR-FETs in parallel linking the highside (or positive output rail) to the positive of the bus. The negative rails of all power converters are all connected together to the negative rail of the bus.

Since this is a high current test setup, extra care should be observed in proper connections on the board to avoid unnecessary contact resistance which may further add heat to the board itself.

As a general design practice in choosing the appropriate mosfets, they must have low Rds_{on} and the Vsd generated should be at least ~50mV when the OR-FET is "ON".

FETCHK FEATURE

Ensure the test setup is correct and both power converters and OR-ing boards are in good condition before starting-up. For safe initial test, it is recommended to power up the OR-ing boards first with system load preset to less than 10Amps as startup load before doing the full load test. The thermal performance should be acceptable at room temperature testing even if the OR-ing board has no heatsink but do not press one or both FETSW for too long . This test will force the circuit to conduct the total load current through the body diodes of the OR-FET which will increase the heat dissipation at a very fast rate; thus extra precaution must be observed during this FETCHK test.

The board takes advantage of a unique feature that comes with the IR5001 IC to assess the redundancy status of the system as well as the functionality of the OR-ing mosfets as a group (OR-FET1 or OR-FET2). Referring to Figure 6, the FETCHK feature enables the system designer to manually switch OFF the IC's Vout pin (gate drive) by pressing a normally-open microswitch "FETCHK SW1/2". This switch link the +12V_aux thru R7 to the clamping zener Z1 (5.1V) in order to provide a logic voltage of ~5V (with reference to the IC's GND (pin (7)) to FETCHK/OFF pin 3. The desired outcome if FETCHK is initiated (while the OR-FET is ON) is to toggle OFF the output of the IC, which will turn-off the OR-FET. This will result in an increase of Vsd of more than 0.3V and a comparator inside will compare it to a 0.3V reference voltage. The internal comparator will turn-ON an open-drain mosfet to pull down pin 4 (FETSHORT pin), providing a ground path for the LED to light up.

SHORT CIRCUIT TEST

During a fault condition such as short circuit of one of the converter, a finite amount of reverse current in the form of short duration negative current spike will occur just before the OR-FET completely turn-off. The peak of this reverse current is dependent on how fast the controller circuit switches off the OR-FETs during this fault condition. The IR5001 IC is capable of sourcing and sinking $3A_{pk}$ to fast turn - ON or OFF of the OR-FETs.

If short circuit occur at the secondary side of any power converter unit before the Active OR-ing circuit, this faulty unit will be isolated by turning-off the OR-FET(s) as quickly as possible, preventing the faulty unit from further drawing any current from the other remaining good power converter(s) connected in the system bus.

It is recommended to set the E-load to 65Amp and set the current limit of the converters to ~120Amp before the evaluation of the reverse current during short circuit test.

Caution : Use appropriate size of shorting wire (larger than #10 AWG with thick insulation) when performing short circuit test. Shorting V1 or V2 should be done very quickly. It is recommended to use a DC high current probe with amplifier initially set to >50A/V to avoid overloading the probe or the amplifier on the first test trial.

INPUT / OUTPUT CONNECTION :

FIGURE 2. TEST APPLICATION SETUP OF IR5001_HS100A OR-ING DEMOBOARD

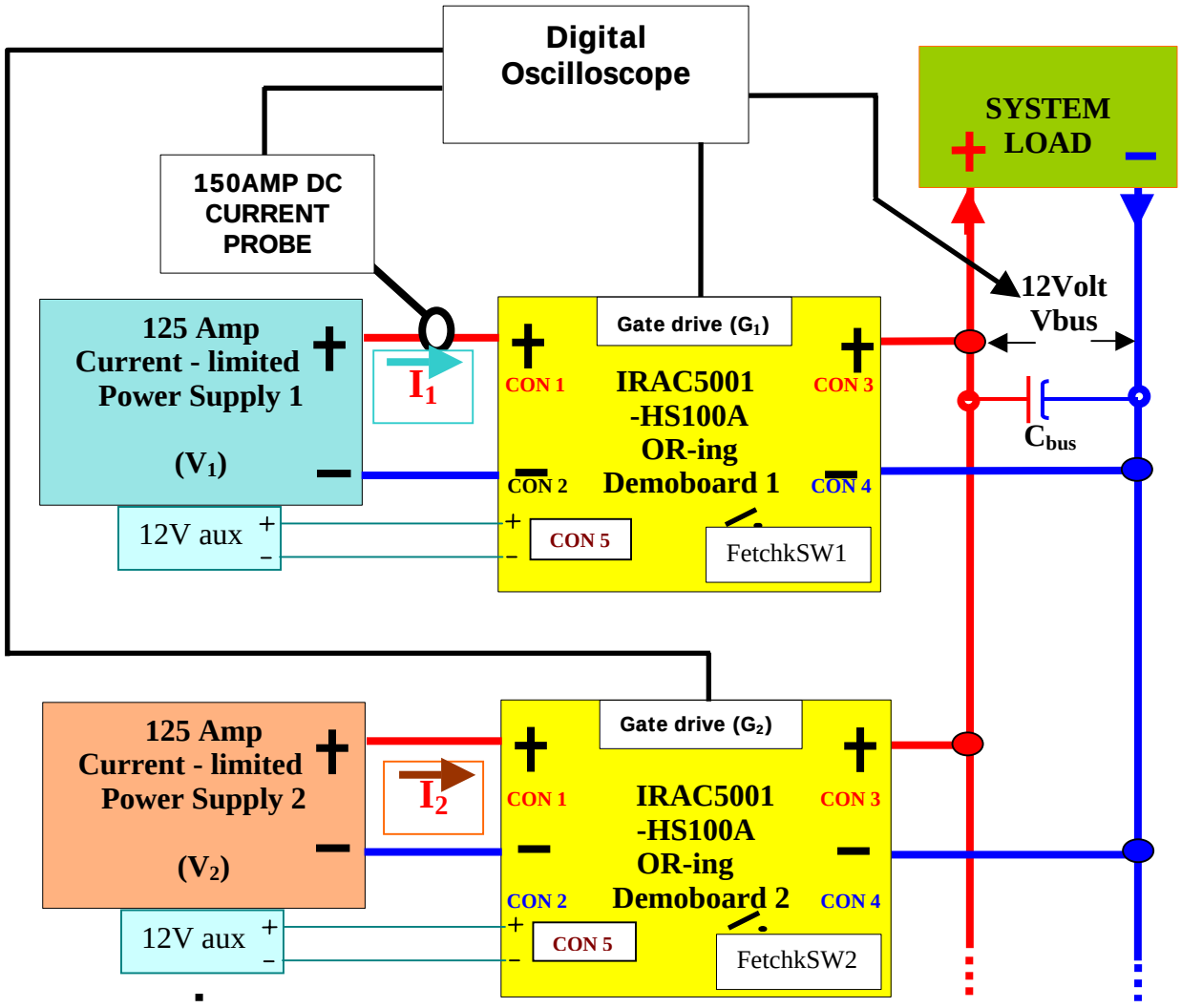


FIGURE 3. Schematic Diagram of IRAC5001-HS100A Highside Active OR-ING Demo board

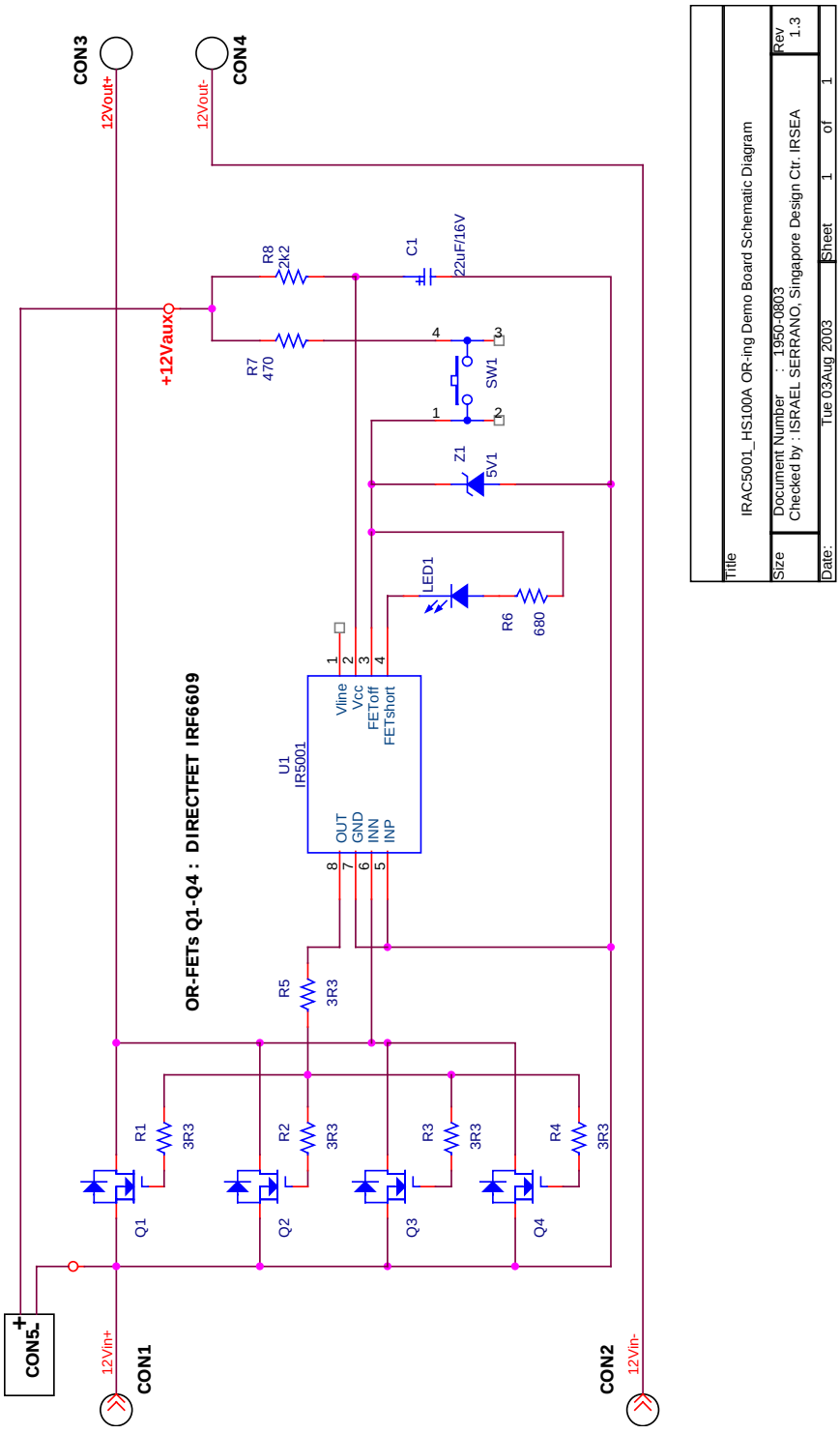
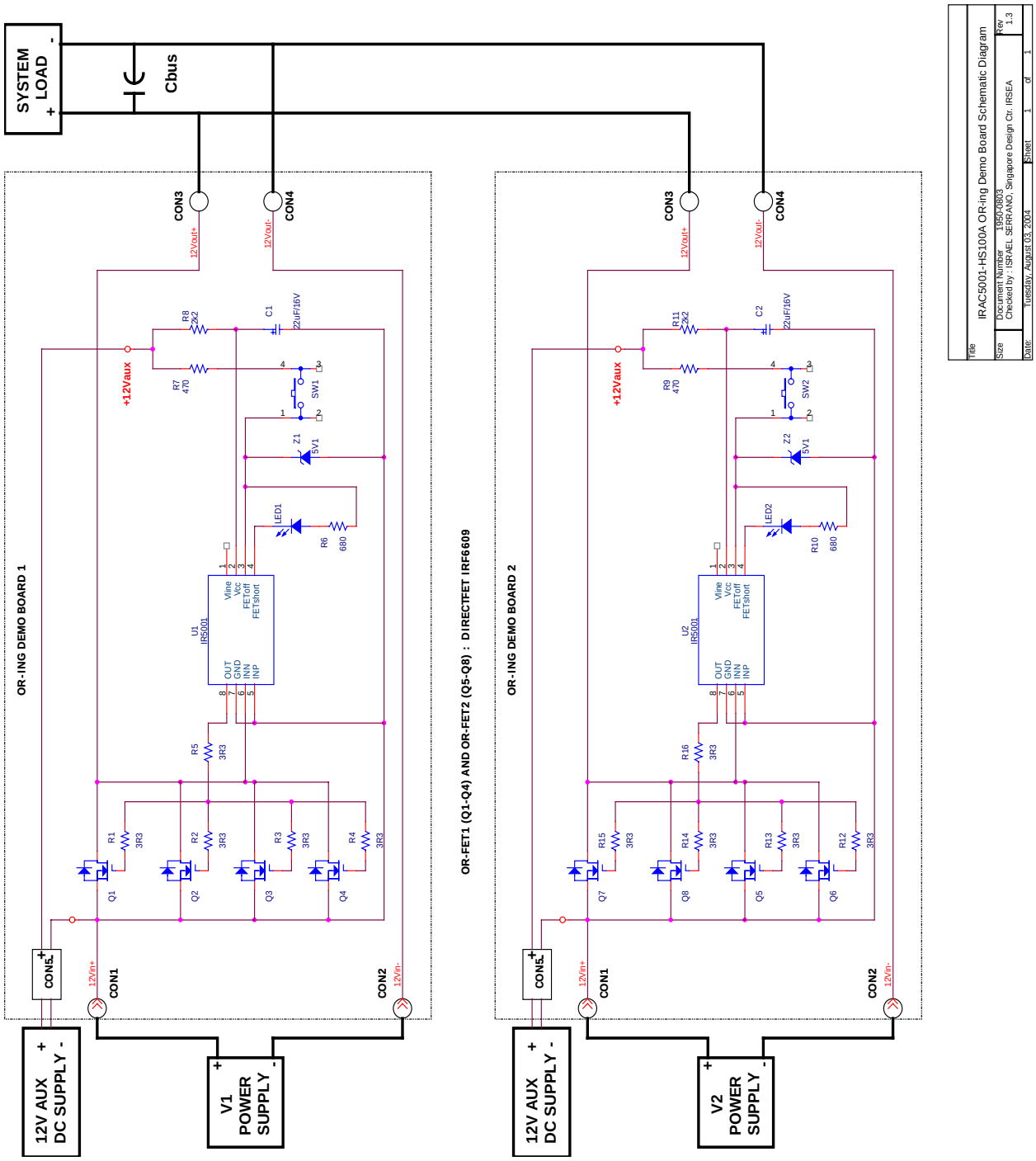
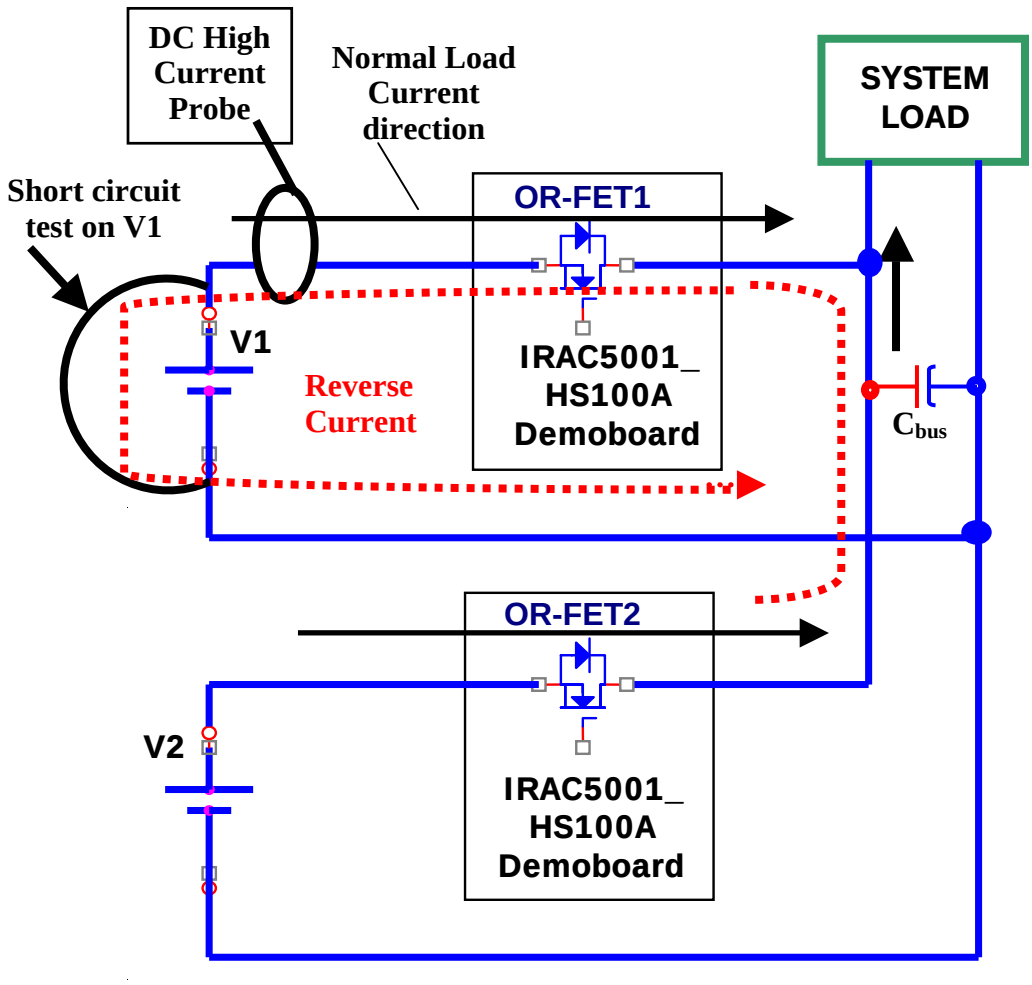


Figure 4. DETAILED DIAGRAM FOR TEST SETUP CONNECTION



Note : Observe the correct polarity and connection of 12Volt auxiliary supply before power up the whole test setup.

Figure 5. SHORT CIRCUIT TEST AND PATH OF THE REVERSE CURRENT



TEST WAVEFORMS

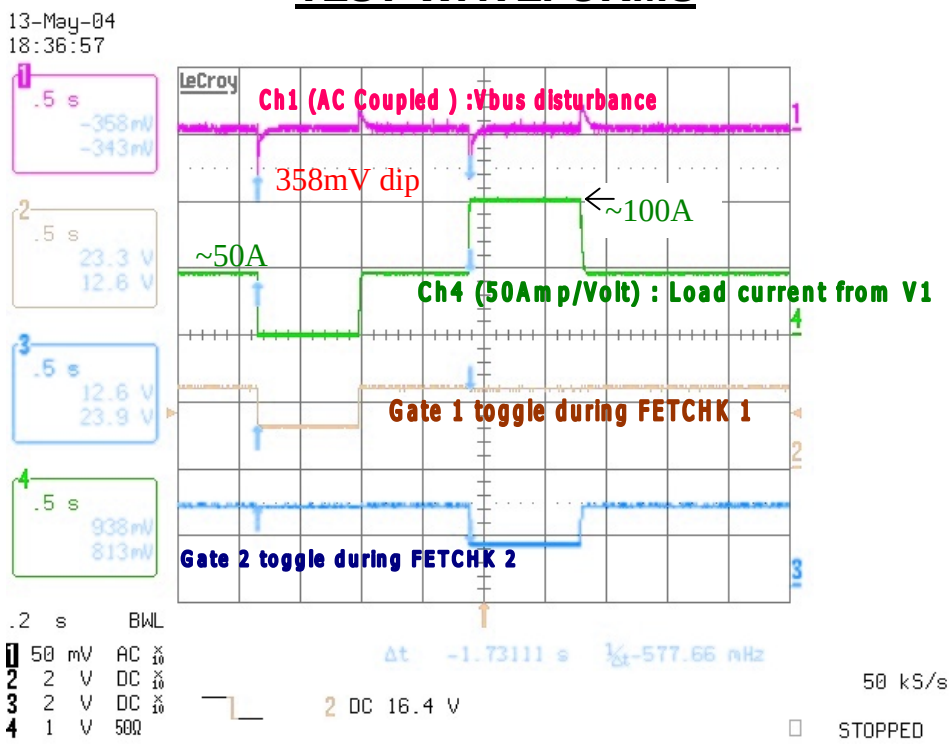


Figure 6A. FETCHK test shows the minimum bus voltage disturbance.

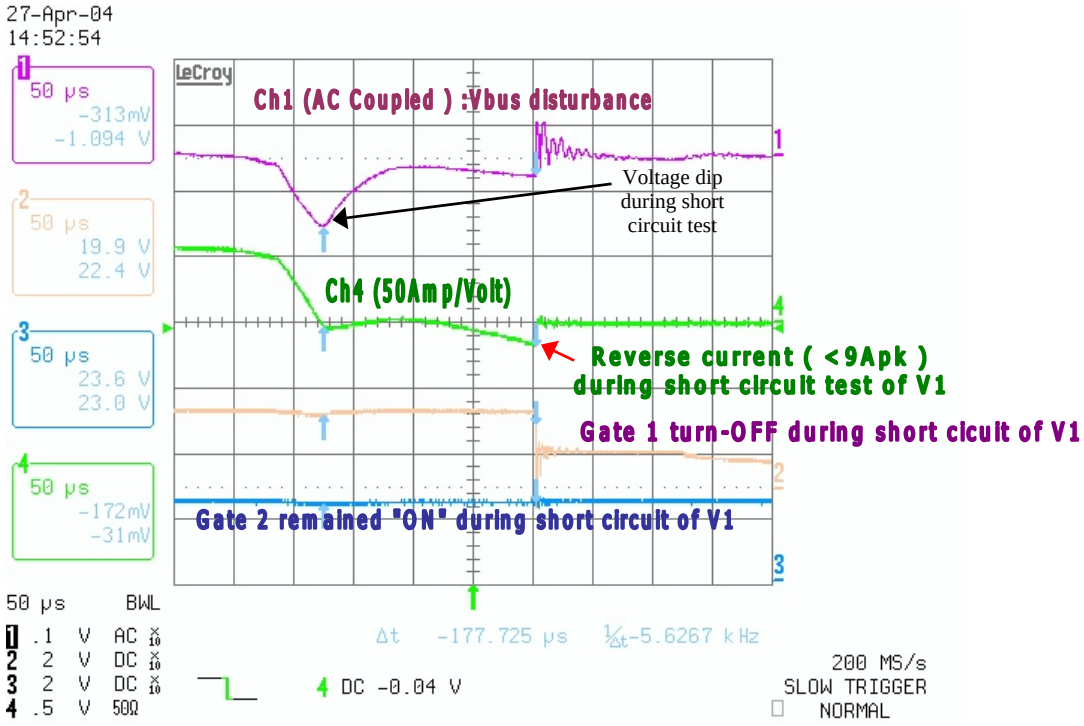


Figure 6B. Reverse current measurement during short circuit test of V1. (With initial system load of ~65Amp)

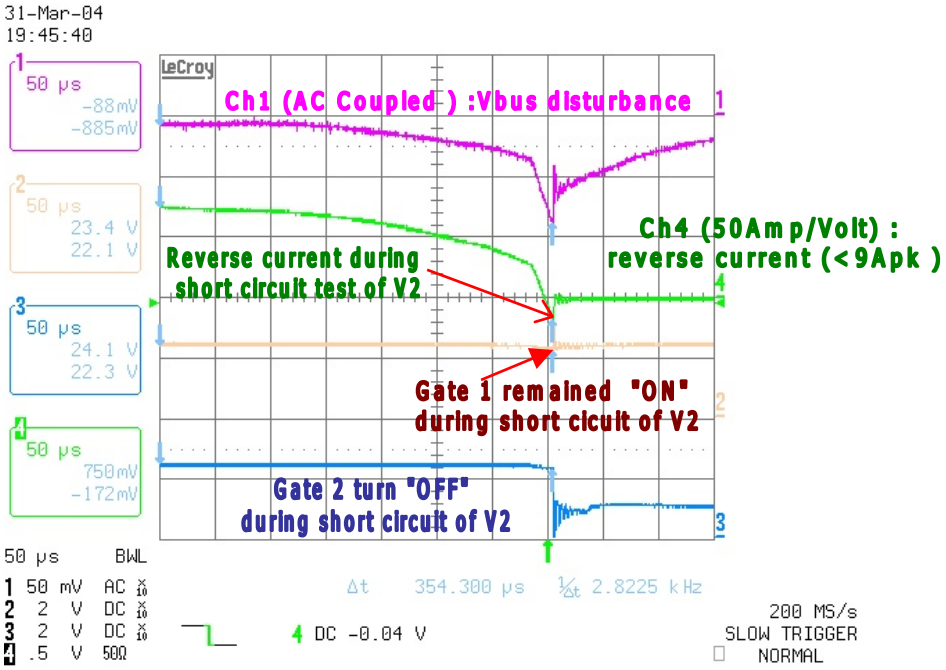


Figure 6C. Reverse current measurement during short circuit test of V2 (With initial system load of ~65Amp)

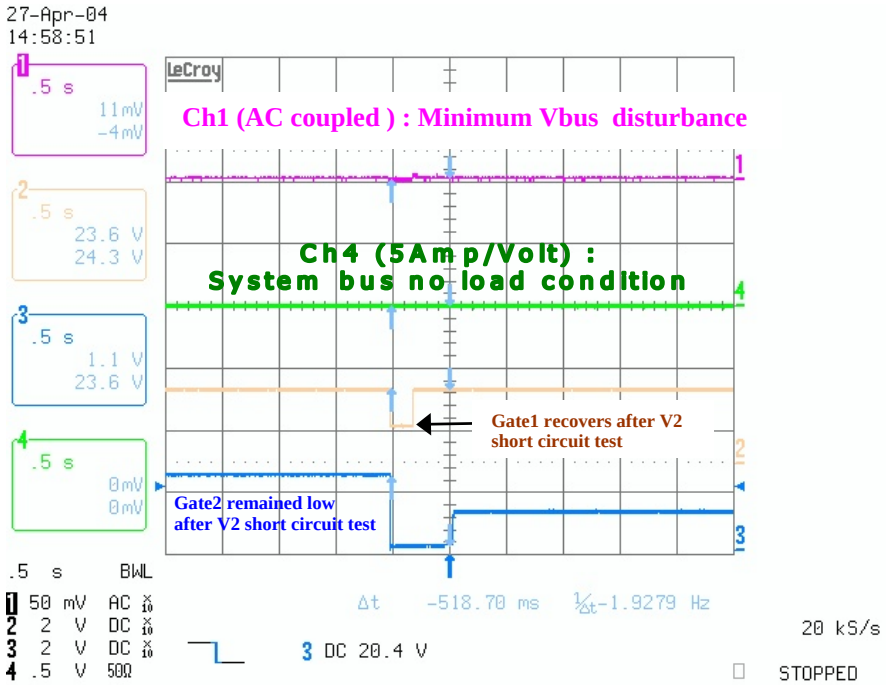


Figure 6D. Minimum reverse current during short circuit test of V2 at no load condition.

Figure 6E. Reverse current during short circuit test of V1 at no load condition.

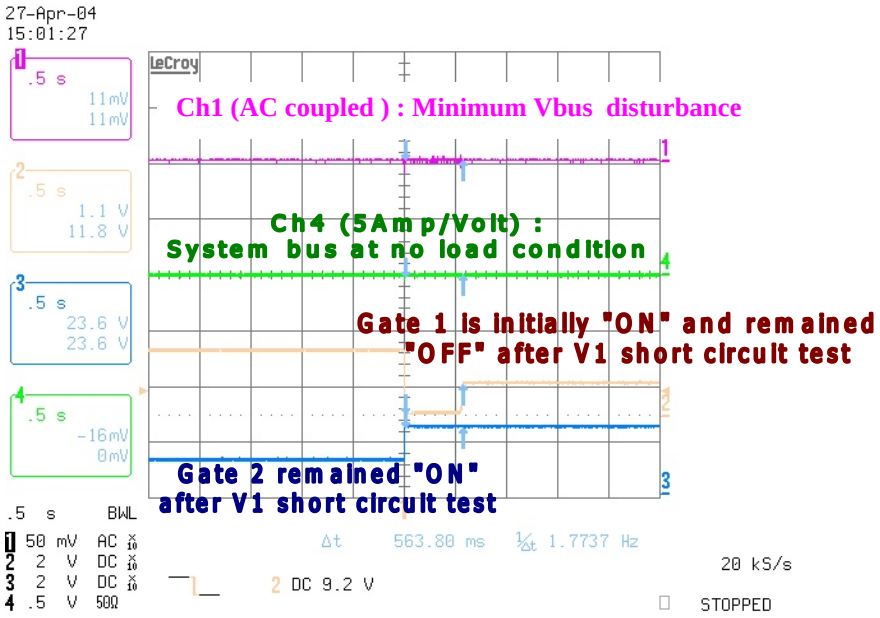


Table 1. Truth table for IR5001 "FET Check Feature"

Case	LED	Initial	During the CHK		OR-FET 1	OR-FET 2	Comment
1	A	off	on	Vsd of FET 1 > 300mV	Good	N/A	V1 > V2 + 0.4V
	B	off	off	Vsd of FET 2 < 300mV			
2	A	off	on	Vsd of FET 1 > 300mV	Good	Good	|V1 – V2| < 0.4V
	B	off	on	Vsd of FET 2 > 300mV			
3	A	off	off	Vsd of FET 1 < 300mV	Short	N/A	V1 > V2 + 0.3V
	B	off	off	Vsd of FET 2 < 300mV	At least one is short		|V1 – V2| < 0.3V
					N/A	Short	V2 > V1 + 0.3V

Figure 7. PCB Layout