Datasheet

LDO Regulators with Voltage Detector

500 mA Output LDO Regulator with Voltage Detector

BD42754FP2-C

General Description

BD42754FP2-C, BD42754FPJ-C are automotive suited voltage regulator with 1ch Reset and offers the output current of 500mA while limiting the low quiescent current.
These regulators are therefore ideal for applications requiring a direct connection to the battery and a low current consumption. A reset signal is generated for an output voltage VO of Typ 4.62 V.
The reset delay time can be programmed by the external capacitor.

Features

- Low ESR ceramic capacitors applicable for output.
- Low drop voltage: PDMOS output transistor
- Power on and under-voltage reset
- Programmable reset delay time by external capacitor.

Applications

- Onboard vehicle device
  (Engine ECU, Body-control car stereos, satellite navigation system, etc.)

Key Specifications

- Qualified for Automotive Applications
- Input Voltage Range: -0.3 V to +45 V
- Low Quiescent Current: 75 µA (Typ)
- Output Load Current: 500 mA
- Output Voltage: 5.0 V ±2 %
- Reset Detect Voltage Accuracy: 4.50 V to 4.75 V (Typ 4.62V)
- Over Current Protection (OCP)
- Thermal Shut Down (TSD)
- AEC-Q100 qualified.

(Note 1:Grade1)

Package

Package	W (Typ) × D (Typ) × H (Max)
FP2: TO263-5	10.16 mm × 15.10 mm × 4.70 mm

Figure 1. Package image

Typical Application Circuit

- VCC and VO pin capacitors: 0.1 µF ≤ C_{IN} (Typ), 6 µF ≤ C_O (Min)
  Please refer to the "Selection of Components Externally Connected".

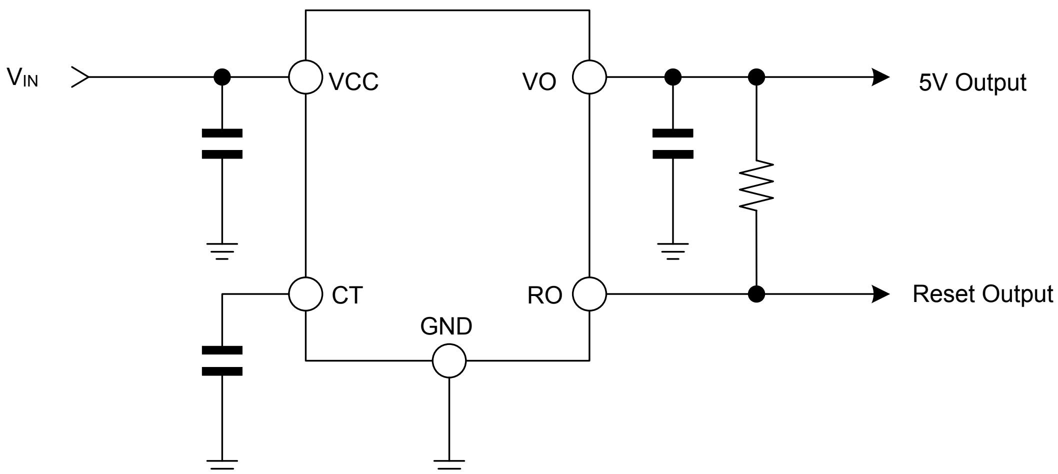


Figure 2. Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Pin Configurations

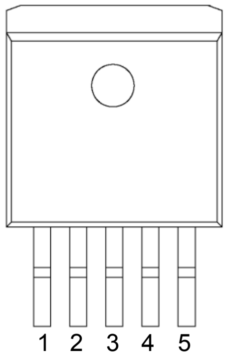


Figure 3. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input
2	RO	Reset Output; Open-Collector output.
3	GND	Ground; Pin3 internally connected to FIN.
4	CT	Reset Delay; connect capacitor to GND for setting delay time.
5	VO	5V Output;
FIN	FIN	FIN; FIN internally connected to Pin3.

Block Diagram

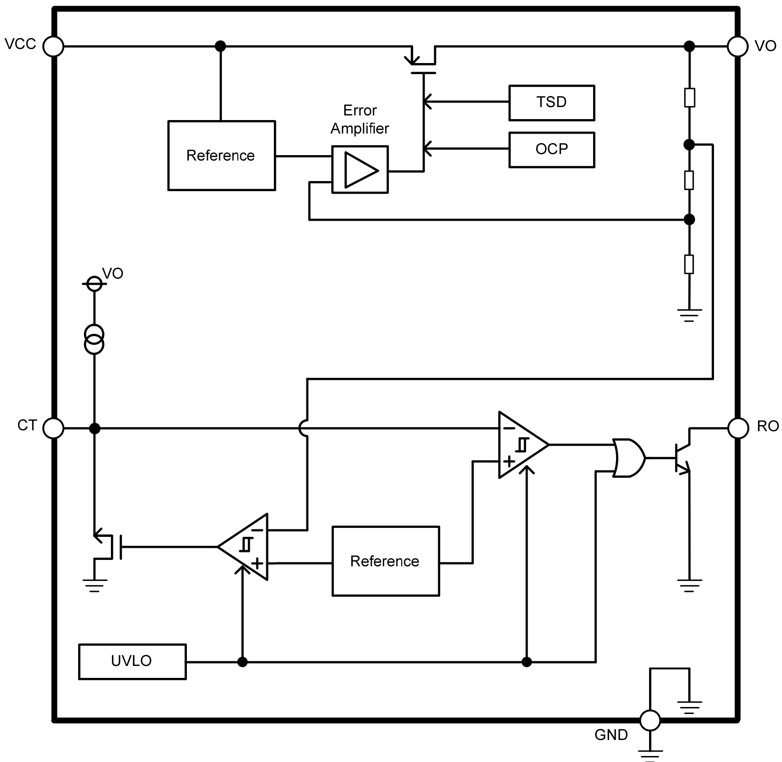


Figure 4. Block Diagram

Block Descriptions

Block Name	Function	Description of Blocks
Reference	Reference voltage	The Reference generates the Reference Voltage.
Error Amplifier	Error amplifier	The Error Amplifier amplifies the difference between the feed back voltage of the output voltage and the reference voltage.
TSD	Thermal shutdown protection	The TSD protects the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
OCP	Over current protection	The OCP protects the device from damage caused by over current.
UVLO	Under voltage lock out	The UVLO prevents malfunction of the reset block in case of very low output voltage.

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
VCC Voltage	V_{CC}	-0.3 to +45.0	V
RO Voltage	V_{RO}	-0.3 to +18.0	V
VO Voltage	V_{O}	-0.3 to +7.0	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Caution) Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage ($I_O \leq$ 300mA)	V_{CC}	5.5	45.0	V
Supply Voltage ($I_O \leq$ 500mA)	V_{CC}	5.9	45.0	V
Start -Up Voltage (Note 1)	V_{CC}	3.0	—	V
Output Current	I_O	0	500	mA
Operating Ratings Temperature	Ta	-40	125	°C

(Note 1)When I_O=0mA.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
TO263-5				
Junction to Ambient	θ_{JA}	80.7	20.3	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	8	2	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Electrical Characteristics (LDO)

(Unless otherwise specified , Tj = -40 °C to +150 °C, V_{CC} = 13.5 V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	—	75	150	μA	I_O = 0 mA
Output Voltage 1	V_O	4.90	5.00	5.10	V	5 mA ≤ I_O ≤ 400 mA 6 V ≤ V_{CC} ≤ 28 V
Output Voltage 2	V_O	4.90	5.00	5.10	V	5 mA ≤ I_O ≤ 200 mA 6 V ≤ V_{CC} ≤ 40 V
Dropout Voltage	ΔVd	—	0.25	0.5	V	V_{CC} = 4.75 V, I_O = 300 mA
Load Regulation	Reg.L	—	10	30	mV	I_O = 10 mA to 250 mA
Line Regulation	Reg.I	-15	—	15	mV	V_{CC} = 8 V to 16 V, I_O = 5 mA
Current Limit	I_{OCP}	500	—	—	mA	—
Ripple Rejection	R.R.	—	60	—	dB	f = 120 Hz, ein = 1 Vrms, I_O = 100 mA
Thermal Shut Down Temperature	T_{TSD}	—	175	—	°C	

Electrical Characteristics (RESET)

(Unless otherwise specified , Tj = -40 °C to +150 °C, V_{CC} = 13.5 V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Switching Threshold	V_{RT}	4.50	4.62	4.75	V	—
Switching Hysteresis	V_{RHY}	20	60	100	mV	—
Upper Delay Switching Threshold	V_{CTH}	—	1.18	—	V	—
Lower Delay Switching Threshold	V_{CTL}	—	0.25	—	V	—
Charge Current	I_{CT}	—	8.8	—	μA	V_{CT} = 0.5 V
Delay time L→H	t_{POR}	10	14	18	ms	C_{CT} = 0.1 μF(Note 1)
RO L Voltage	V_{ROL}	—	—	0.4	V	RO pull-up resister ≥ 4.7 kΩ V_O ≥1V

(Note 1) T_{POR} can be varied by changing the CT capacitance value(T_{POR_ADJ}). (0.001μF to 10 μF available)

T_{POR_ADJ} (ms) ≈ T_{POR} (the reset delay time at C_{CT} = 0.1 μF) × C_{CT} (μF) / 0.1 CT capacitor : 0.1μF ≤ C_{CT} ≤ 10 μF

example: When C_{CT}= 1μF, 100ms ≤ T_{POR} ≤ 180 ms

T_{POR_ADJ} (ms) ≈ T_{POR} (the reset delay time at C_{CT} = 0.1 μF) × C_{CT} (μF) / 0.1 ±0.1 CT capacitor : 0.001μF ≤ C_{CT} < 0.1 μF

example: When C_{CT}= 0.01μF, 0.9ms ≤ T_{POR} ≤ 1.9 ms

Typical Performance Curves (Unless otherwise specified , Tj = 25 °C, V_{CC} = 13.5 V)

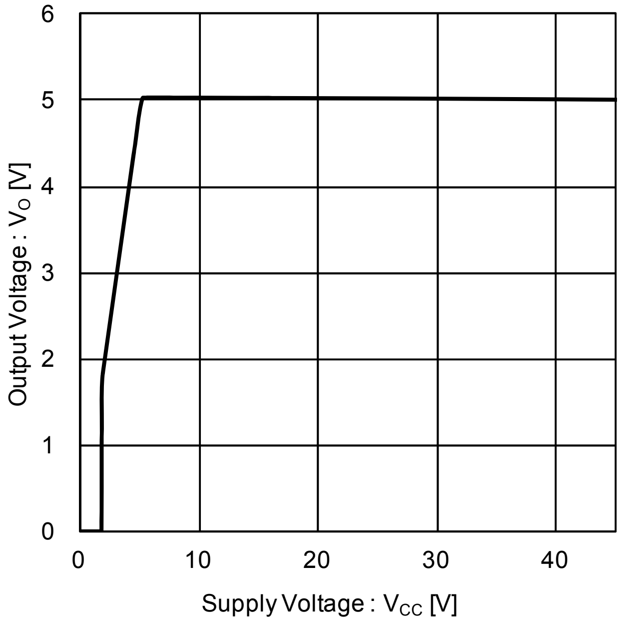


Figure 5. Output Voltage vs Supply Voltage
(R_L = 25 Ω)

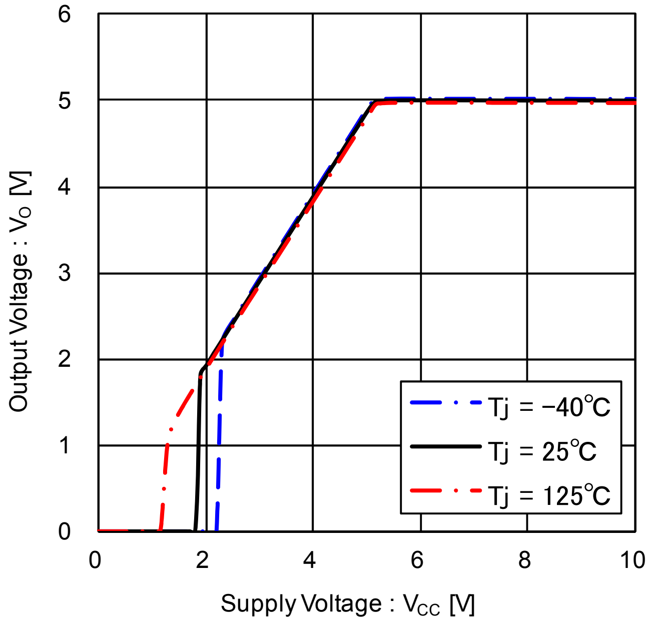


Figure 6. Output Voltage vs Supply Voltage
(at Low supply voltage, R_L = 25 Ω)

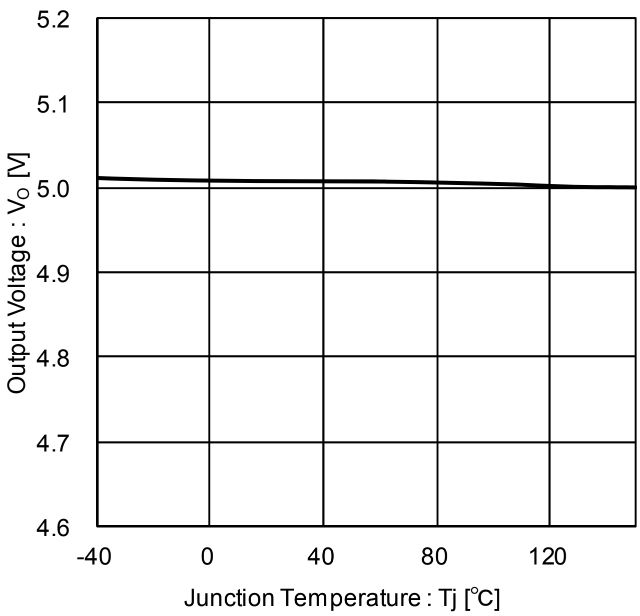


Figure 7. Output Voltage vs Temperature
(R_L = 1 kΩ)

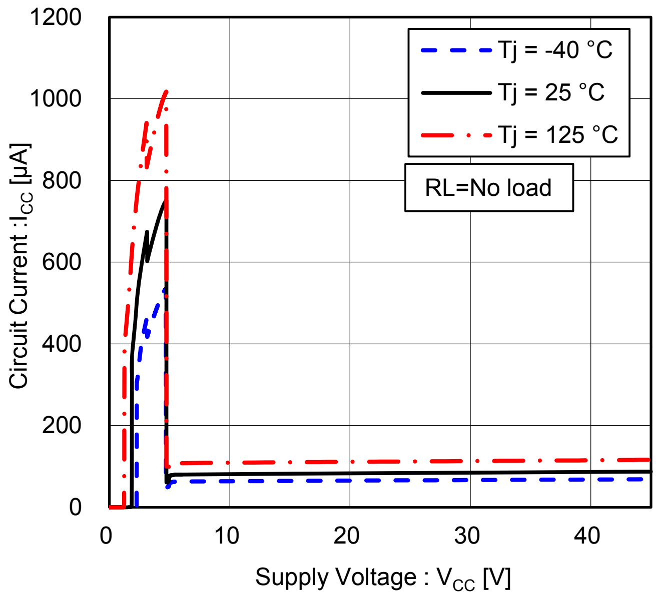


Figure 8. Circuit Current vs Supply voltage

Typical Performance Curves -Continue

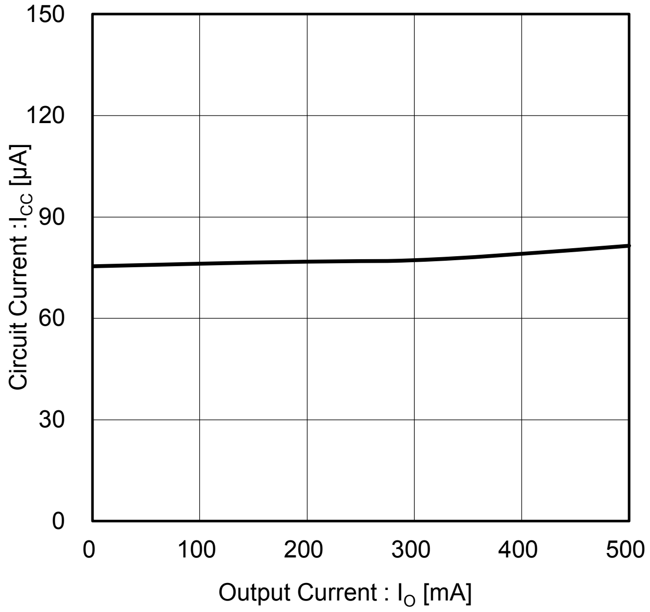


Figure 9. Circuit Current vs Output Current

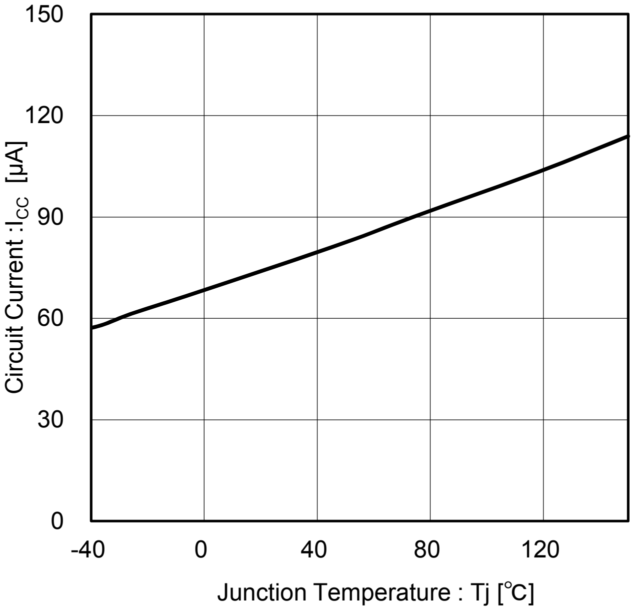


Figure 10. Circuit Current vs Temperature

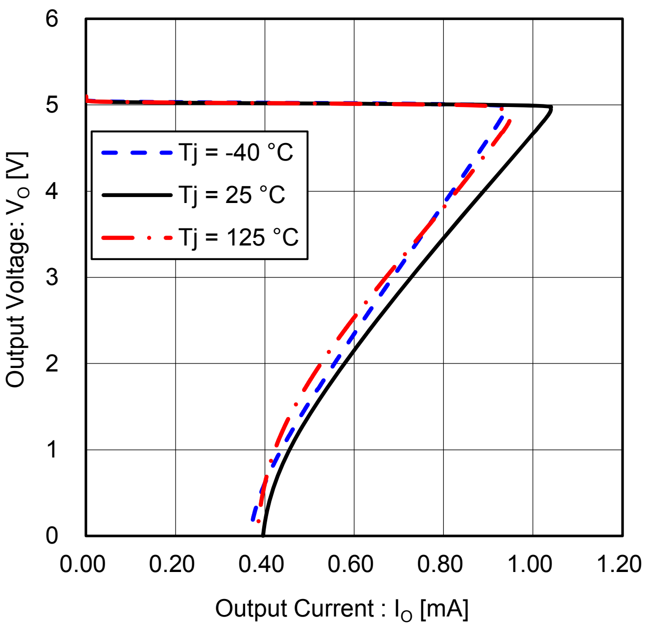


Figure 11. Output Voltage vs Output Current (Over Current Protection)

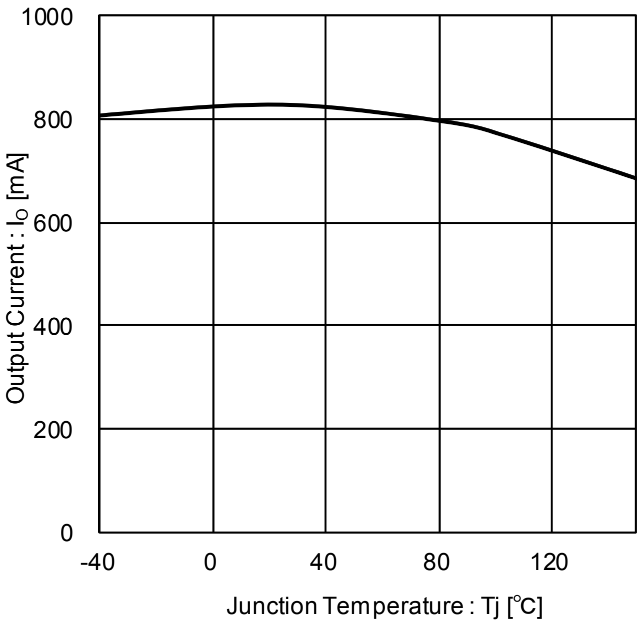


Figure 12. Output Current vs Temperature

Typical Performance Curves -Continue

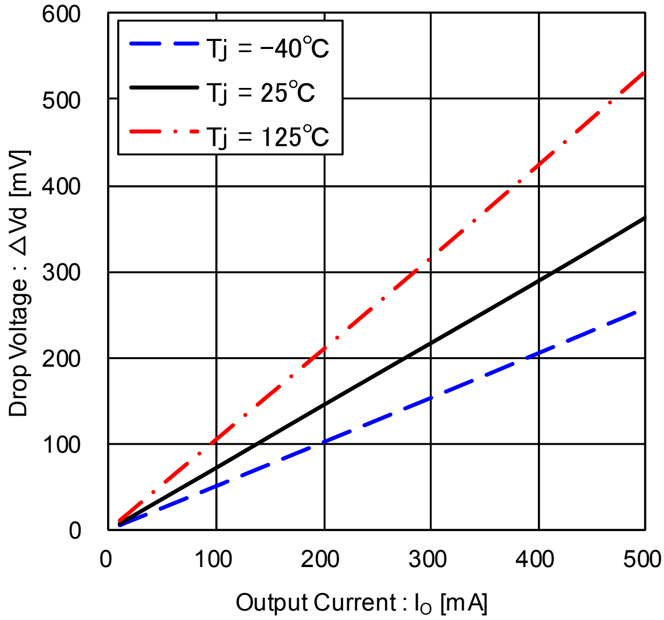


Figure 13. Drop voltage vs Output Current
(V_{CC} = 4.75 V)

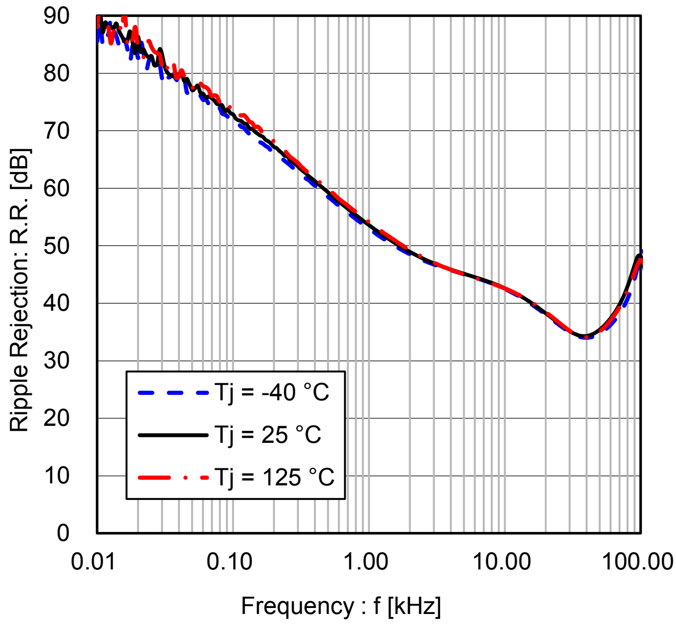


Figure 14. Ripple Rejection
(ein=1Vrms, I_{OUT}=100mA)

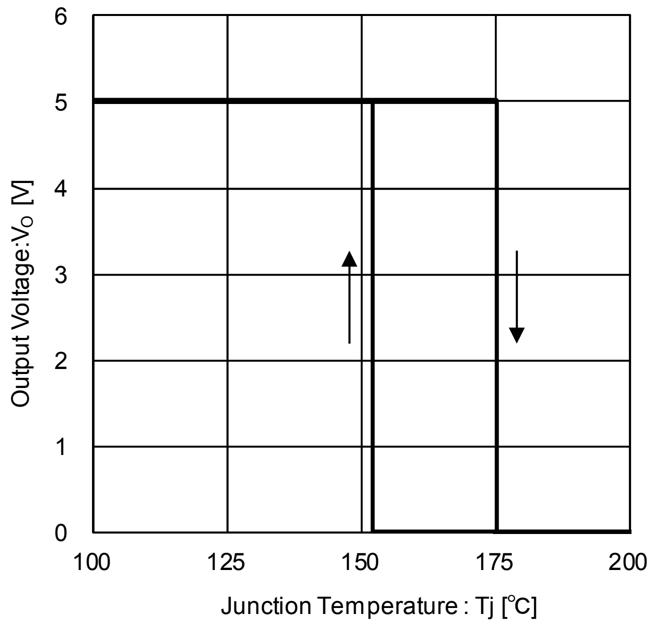


Figure 15. Output Voltage vs Temperature
(Thermal Shut Down)

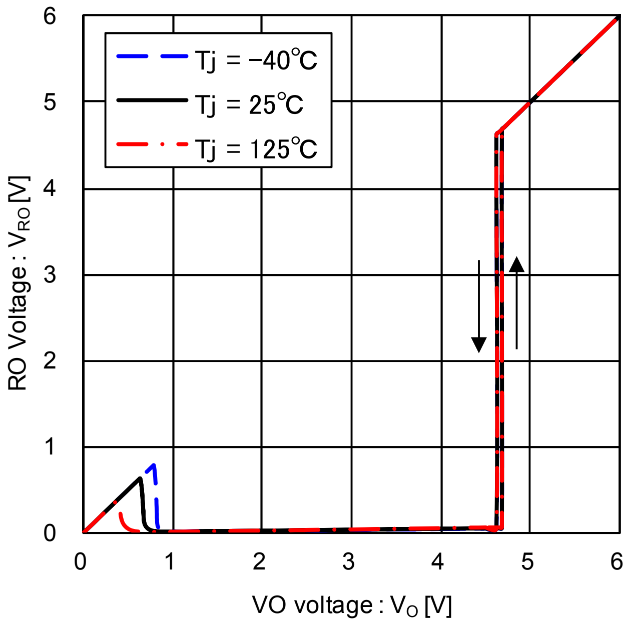


Figure 16. RO Voltage vs VO Voltage
(RO: 10 kΩ pull-up to VO)

Typical Performance Curves -Continue

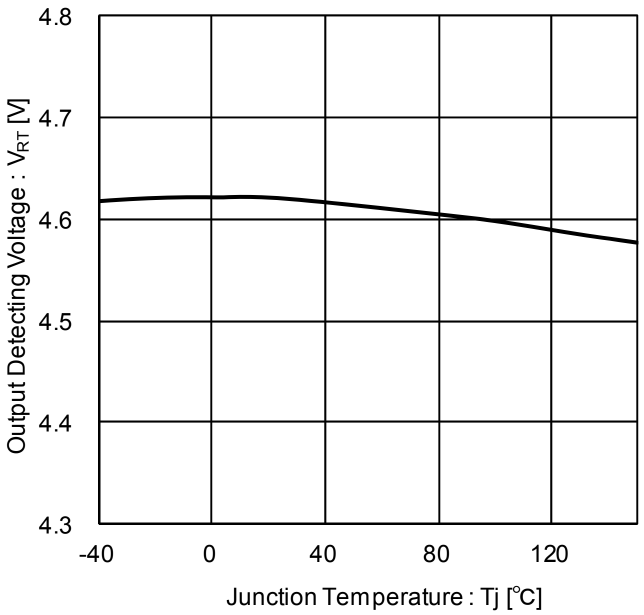


Figure 17. Output Detecting Voltage vs Temperature
(RO: 10 kΩ pull-up to VO)

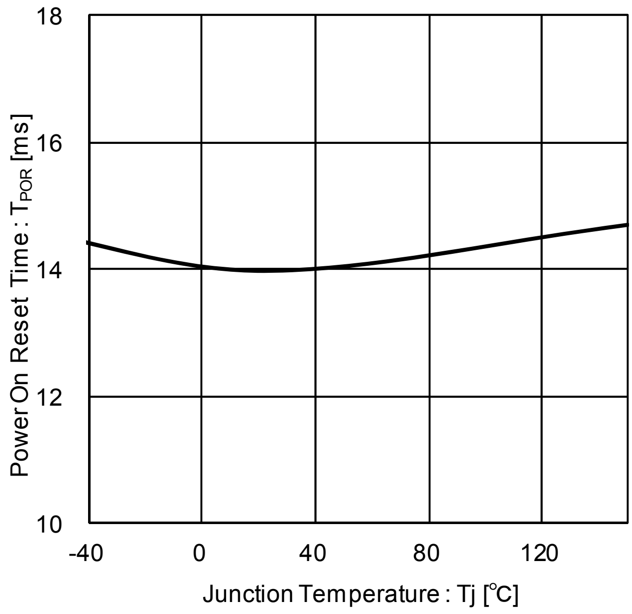


Figure 18. Power on Reset Time vs Temperature
(C_{CT} = 0.1 µF)

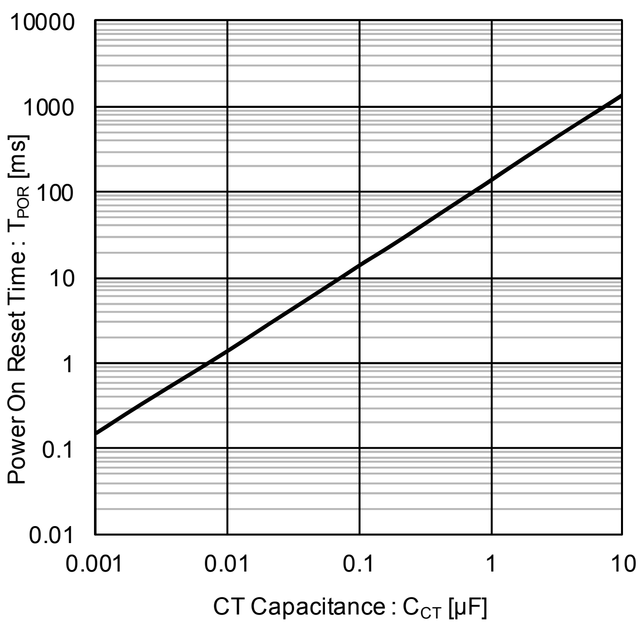
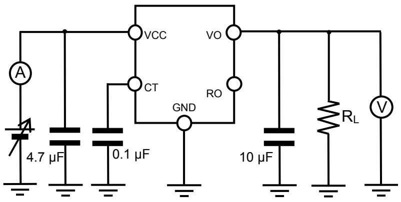
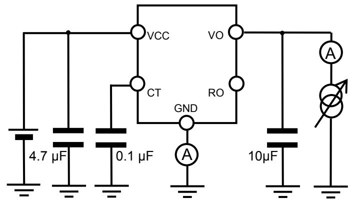


Figure 19. Power on Reset Time vs CT Capacitance

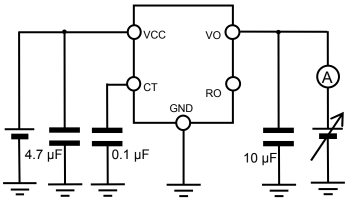
Measurement circuit for Typical Performance Curves



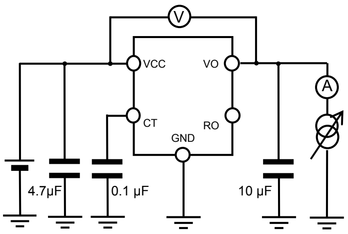
Measurement circuit for
Figure. 5, 6, 7, 8, 10, 14,15



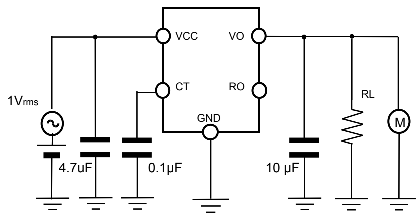
Measurement circuit for
Figure.9



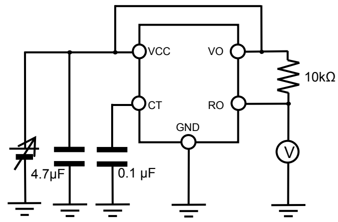
Measurement circuit for
Figure.11, 12



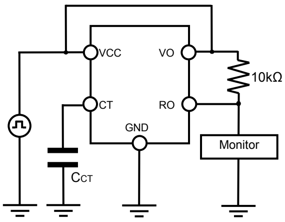
Measurement circuit for
Figure.13



Measurement circuit for
Figure.14



Measurement circuit for
Figure.16, 17



Measurement circuit for
Figure.18, 19

Figure 20. Measurement circuit for Typical Performance Curves

Timing Chart

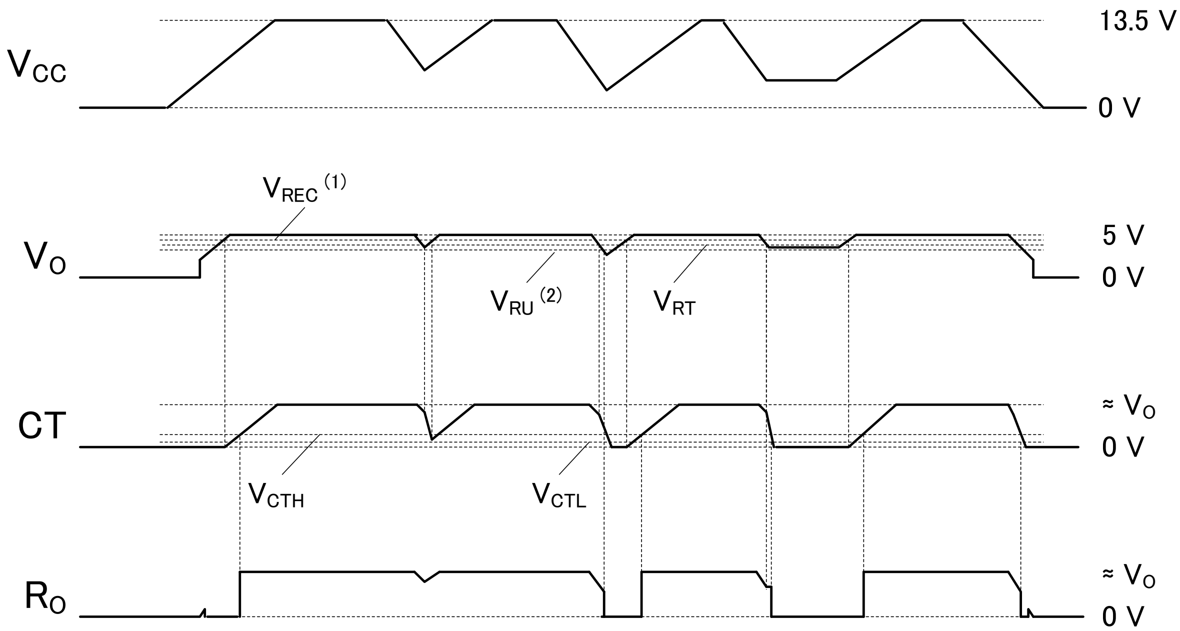


Figure 21. Timing Chart

(1) $V_{REC} = V_{RT} + V_{RHY}$
(2) V_{RU} = 2V to 3.5 V

Power Dissipation

■TO263-5

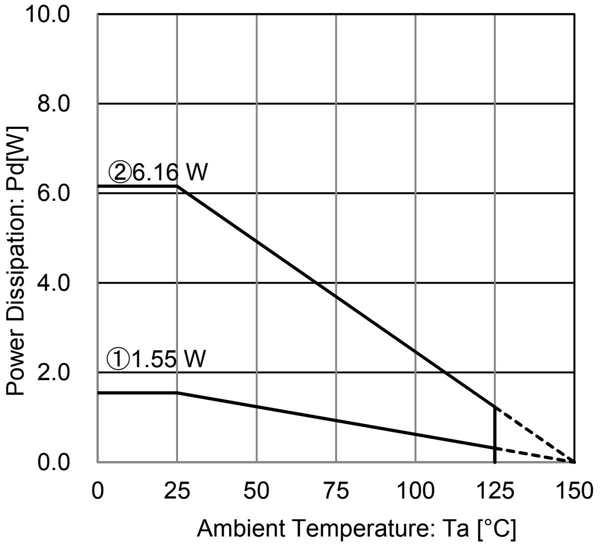


Figure 22. Package Data
(TO263-5)

IC mounted on ROHM standard board based on JEDEC.
①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
Board material: FR4
Board size: 114.3mm × 76.2mm × 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

②: 4-layer PCB
(Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
Board material: FR4
Board size: 114.3mm × 76.2mm × 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 80.7 °C/W、Ψ_{JT} (top center) = 8 °C/W

Condition②: θ_{JA} = 20.3 °C/W、Ψ_{JT} (top center) = 2 °C/W

Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement.
Within this IC, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to power dissipation curves illustrated in Figure 22 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 ℃ in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150℃ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj.

$Tj = Ta + P_C \times \theta_{JA}$

Tj : Junction Temperature
Ta : Ambient Temperature
P_C : Power Consumption
θ_{JA} : Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj.

$Tj = T_T + P_C \times \Psi_{JT}$

Tj : Junction Temperature
T_T : Top Center of Case's (mold) Temperature
P_C : Power consumption
Ψ_{JT} : Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

Pc = (VCC - VOUT) × IOUT + VCC × Icc

P_C : Power Consumption
VCC : Input Voltage
VOUT : Output Voltage
I_O : Load Current
Icc : Circuit Current

・Calculation Example(TO263-5)

If VCC = 13.5 V, VOUT = 5.0 V, I_O = 200 mA, Icc = 75 μA, the power consumption Pc can be calculated as follows:

P_C = (VCC - VOUT) × I_O + VCC × Icc
= (13.5 V – 5.0 V) × 200 mA + 13.5 V × 75 μA
= 1.7 W

At the ambient temperature Tamax = 85°C, the thermal impedance (Junction to Ambient)θ_{JA} = 20.3 °C / W(4-layer PCB),

$Tj = Tamax + P_C \times \theta_{JA}$
= 85 °C + 1.7 W × 20.3 °C / W
= 119.5 °C

When operating the IC, the top center of case's (mold) temperature T_T = 100℃、Ψ_{JT} = 8 °C / W(1-layer PCB),

$Tj = T_T + P_C \times \Psi_{JT}$
= 100 °C + 1.7 W × 8 °C / W
= 113.6 °C

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

Selection of Components Externally Connected

・VCC pin

Insert capacitors with a capacitance of 0.1 μF or higher between the VCC and GND pin. Choose the capacitance according to the line between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the application. Verify the application and allow for sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

・Output pin capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend using a ceramic capacitor with a capacitance of 6 μF or higher. In selecting the capacitor, ensure that the capacitance of 6 μF or higher is maintained at the intended applied voltage and temperature range. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC - biasing characteristics and high voltage tolerance.

In case the application requires large capacitance for output pin, we recommend using a capacitor with a capacitance of 10μF or higher and ESR of 5 Ω or lower. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed. For the rapid fluctuation of input voltage and the load current, it is possible that output voltage fluctuates. In case this fluctuation can be problematic for the application, connect low ESR capacitor (capacitance > 6 μF, ESR < 1 Ω) in paralleled to large capacitor (not low ESR).

I/O equivalence circuits

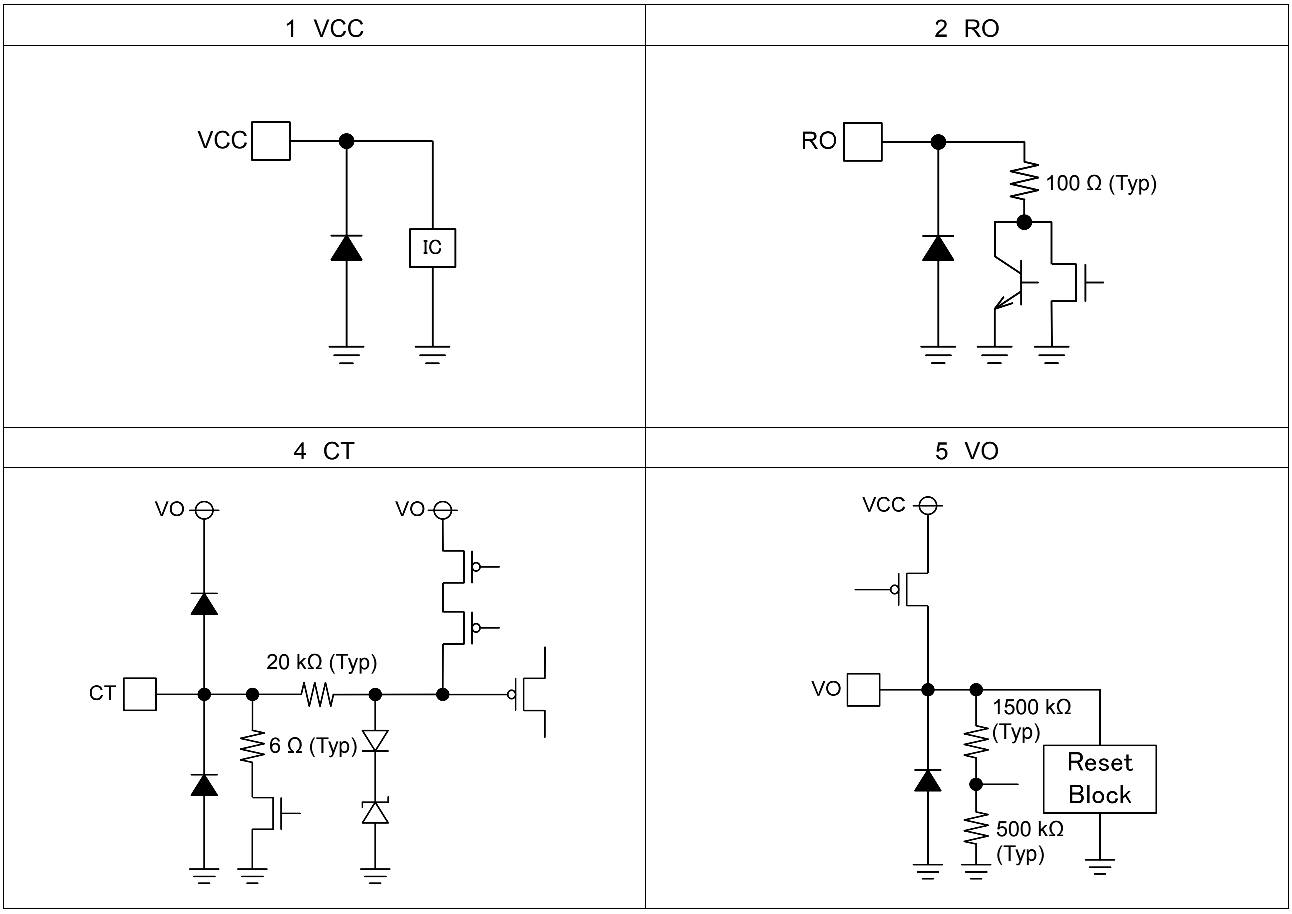


Figure 23. I / O equivalence circuits

Application Examples

・Applying positive surge to the VCC
If the possibility exists that surges higher than 45 V will be applied to the VCC, a Zener Diode should be placed between the VCC and GND as shown in the figure below.

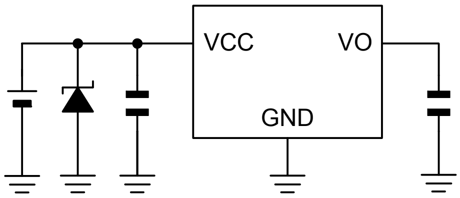


Figure 24. Application Example 1

・Applying negative surge to the VCC
If the possibility exists that negative surges lower than the GND are applied to the VCC, a Shottky Diode should be place between the VCC and GND as shown in the figure below.

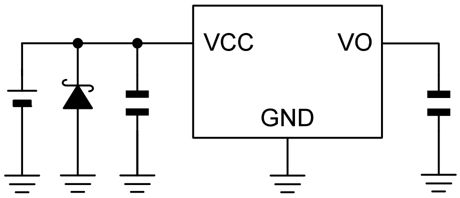


Figure 25. Application Example 2

・Implementing a Protection Diode
If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.

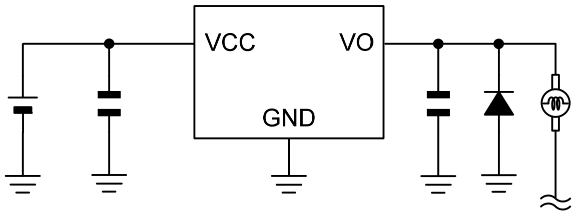


Figure 26. Application Example 3

・Reverse Polarity Diode
In some applications, the VCC and pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the A point shorts to the GND. Use a capacitor with a capacitance with less than 1000 µF. We also recommend using reverse polarity diodes in series or a bypass between all pins and the VCC.

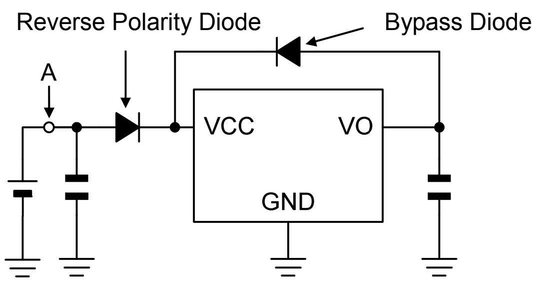


Figure 27. Application Example 4

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

10. Unused Input Pins

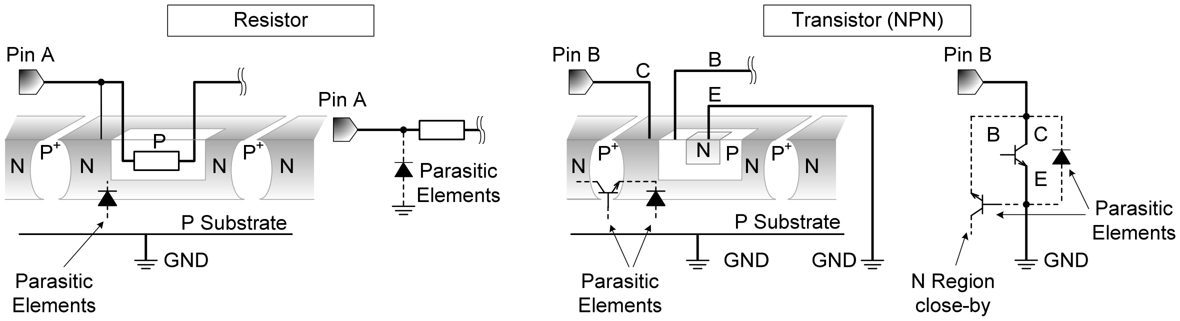
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

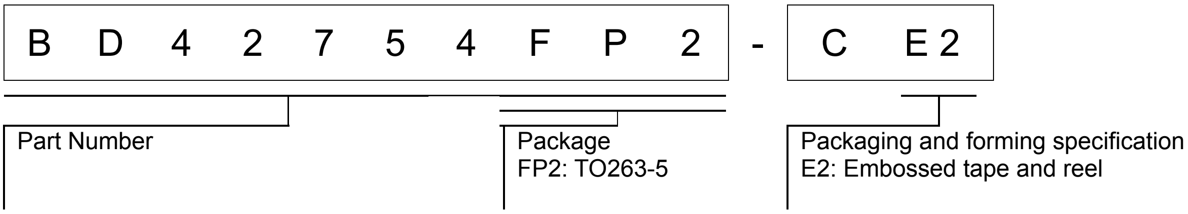
13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

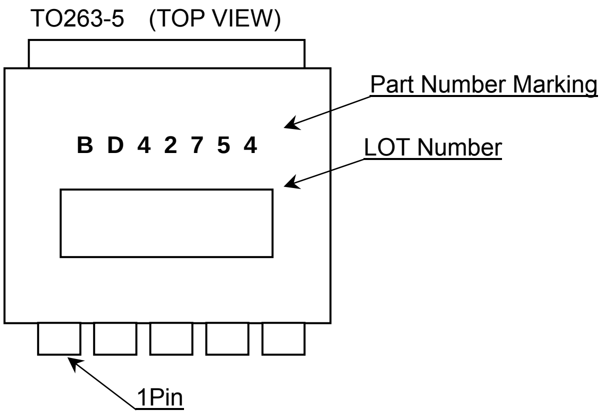
14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

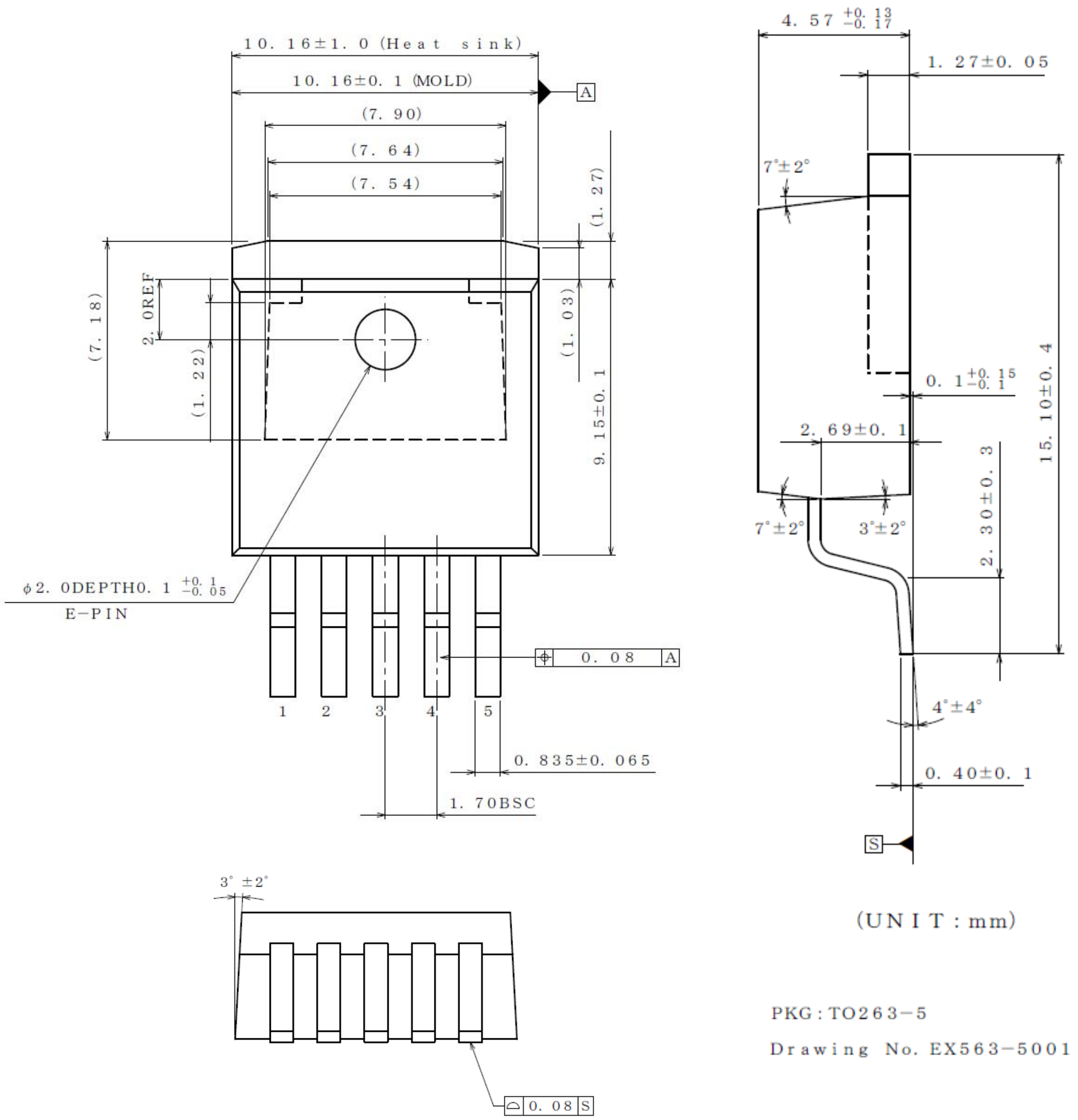


Marking Diagram



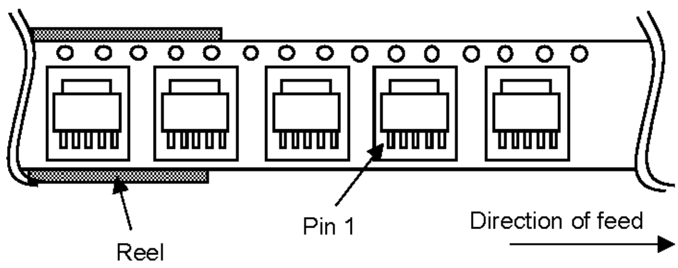
Physical Dimension Tape and Reel Information

Package Name	TO263-5



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
31.Aug.2016	001	New Release.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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Distribution Inventory

Part Number	BD42754FP2-C
Package	TO263-5F
Unit Quantity	500
Minimum Package Quantity	500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes