USBULC6-3F3

3-line low capacitance protection for high speed USB

Datasheet – production data

Features

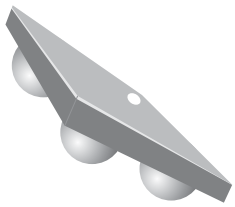
- Ultra low capacitance 0.85 pF
- Unidirectional device
- Low clamping factor V_{CL}/V_{BR}
- Fast response time
- Very thin package: 0.605 mm max
- Low leakage current

Benefits

- High ESD and EOS protection level
- High integration
- Suitable for high density boards

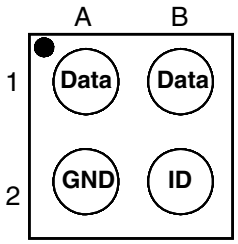
Complies with the following standards:

- IEC 61000-4-2 level 4
- MIL STD 883G - Method 3015.7: class 3B



Flip Chip
(4 bumps)

Figure 1. Pin configuration (bump side)



Application

High speed USB port in wireless handsets (up to 480 Mb/s according to USB 2.0 high speed specification)

Description

The USBULC6-3F3 is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultralow line capacitance secures a high level of signal integrity without compromising the protection of downstream sensitive chips against the most stringently characterized ESD strikes.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, level 4 contact discharge		8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)	T_j initial = T_{amb}	50	W
I_{PP}	Peak pulse current (8/20 µs)		2.5	A
T_j	Maximum junction temperature		125	°C
T_{op}	Operating temperature range		-30 to + 85	°C
T_{stg}	Storage temperature range		-55 to +150	°C

Figure 2. Electrical characteristics (definitions)

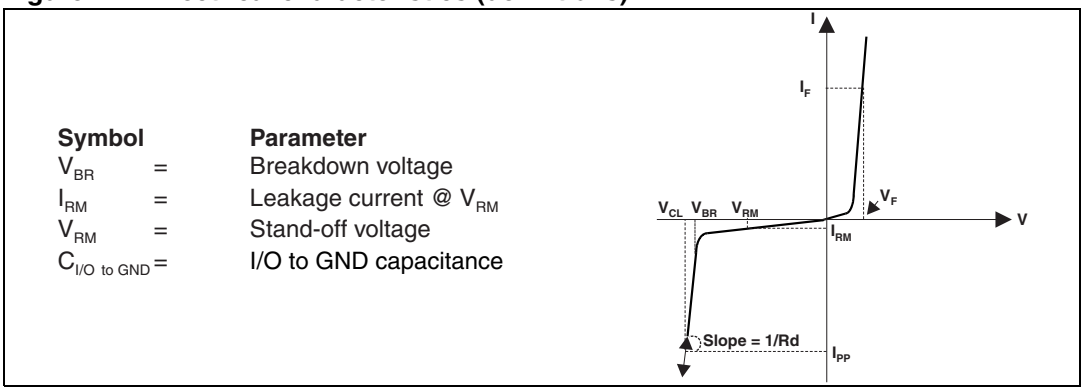


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	-	-	V
I_{RM}	V_{RM} = 3 V	-	-	100	nA
$C_{I/O\ to\ GND}$	Data (A1 and B1 bumps): V_R = 0 V DC, F=1 MHz, V_{OSC} = 30 mV	-	0.85	1.2	pF
	ID (B2 bump): V_R = 0 V DC, F = 1 MHz, V_{OSC} = 30 mV_{RMS}	-	-	3	

Figure 3. Relative variation of peak pulse power versus initial junction temperature (typical value)

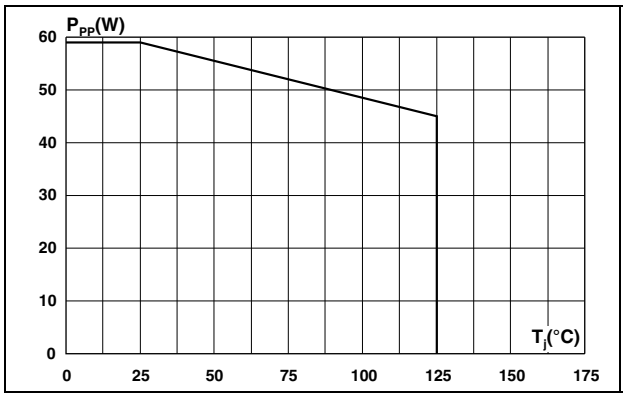


Figure 4. Peak pulse power versus exponential pulse duration (typical)

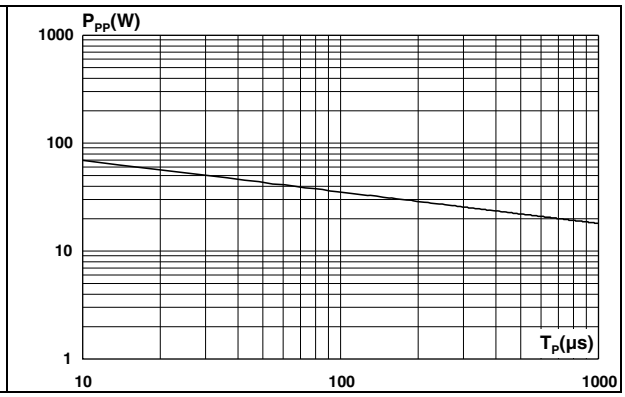


Figure 5. Clamping voltage versus peak pulse current (typical values, exponential waveform)

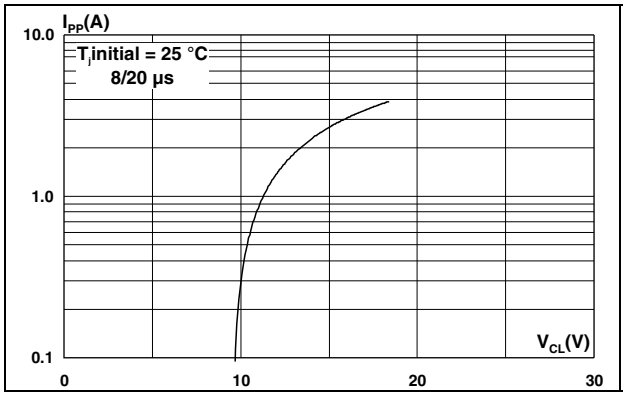


Figure 6. Forward voltage drop versus peak forward current (typical values)

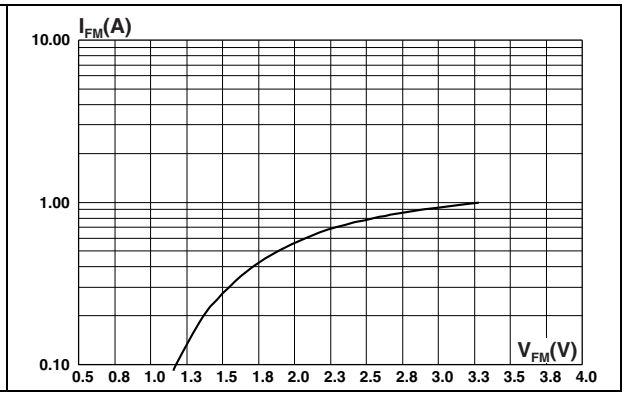


Figure 7. Junction capacitance versus reverse voltage applied (typical values)

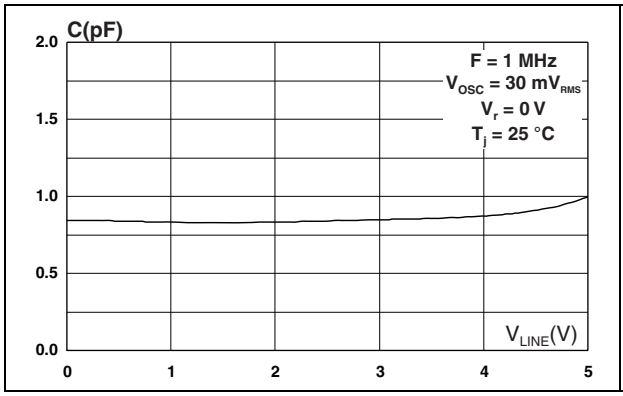


Figure 8. Junction capacitance versus frequency (typical values)

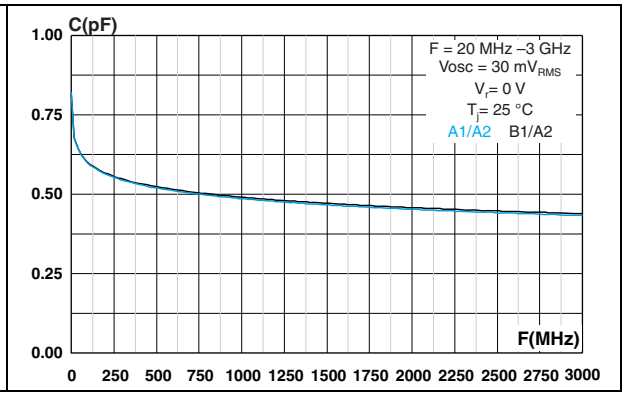


Figure 9. Leakage current versus junction temperature (typical values)

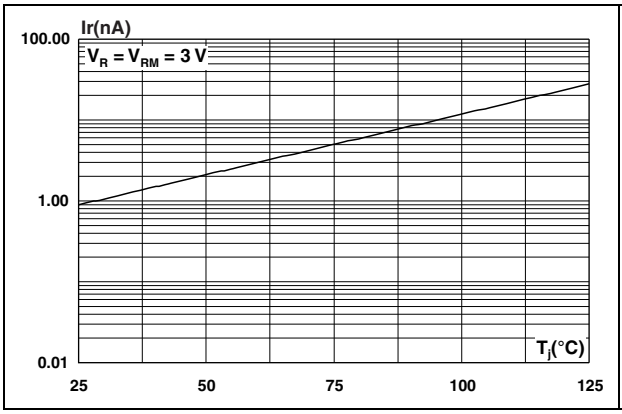


Figure 10. S21 (dB) attenuation

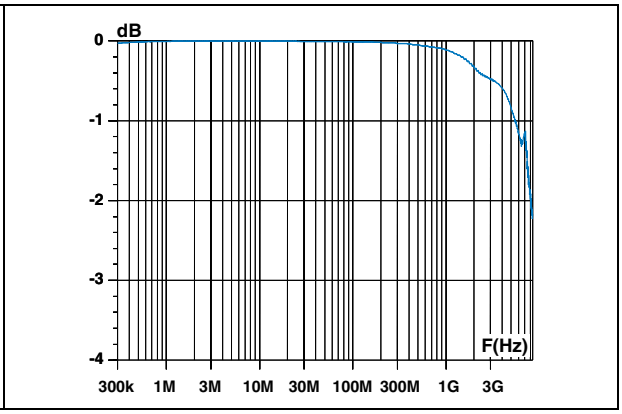


Figure 11. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

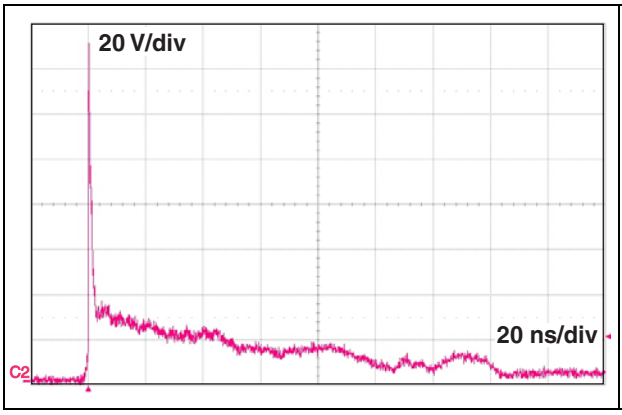


Figure 12. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

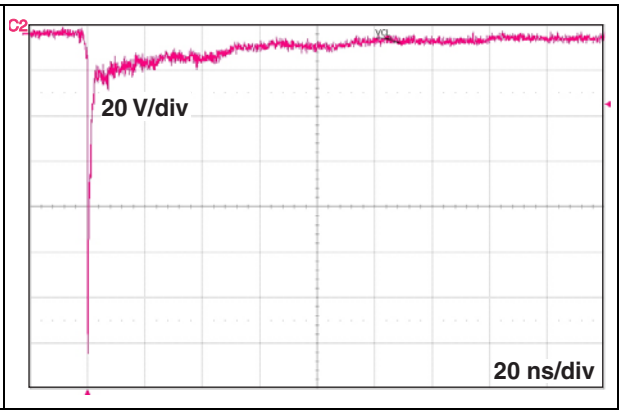


Figure 13. Eye diagram PCB only, 400 mV amplitude, F = 480 Mbps

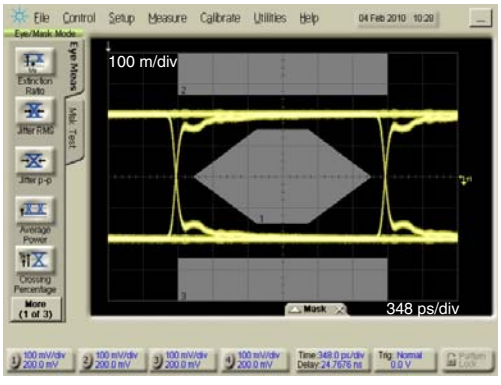
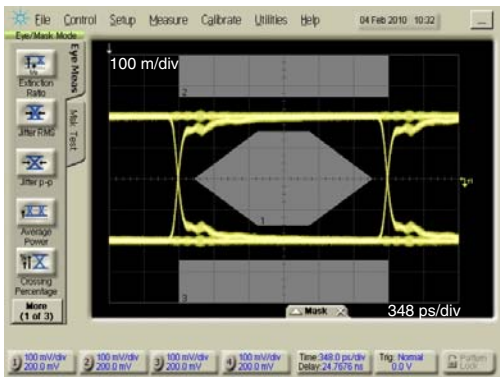
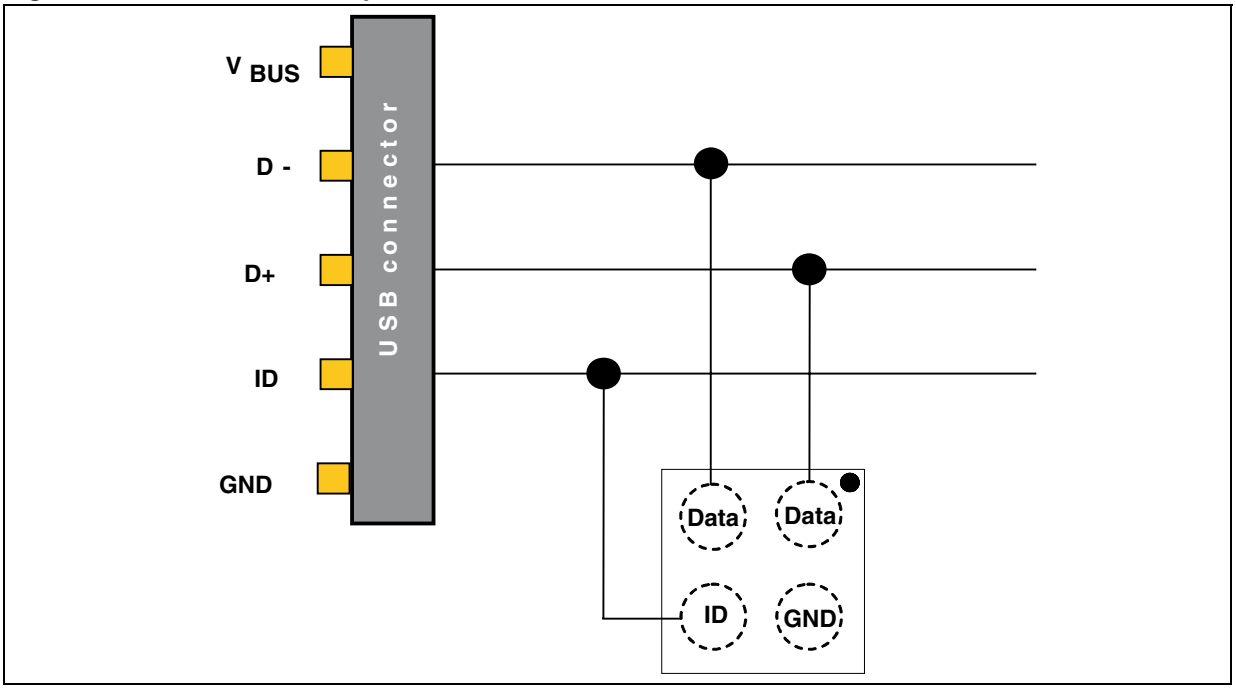


Figure 14. Eye diagram PCB + USBULC6-3F3 400 mV amplitude, F = 480 Mbps



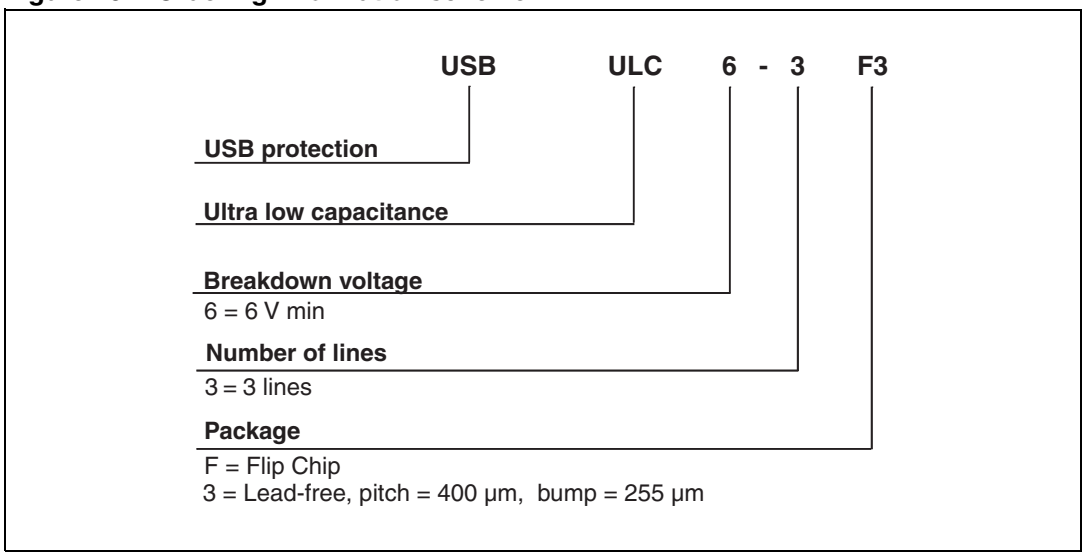
2 Application schematic example

Figure 15. Schematic example



3 Ordering information scheme

Figure 16. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 17. Package dimensions

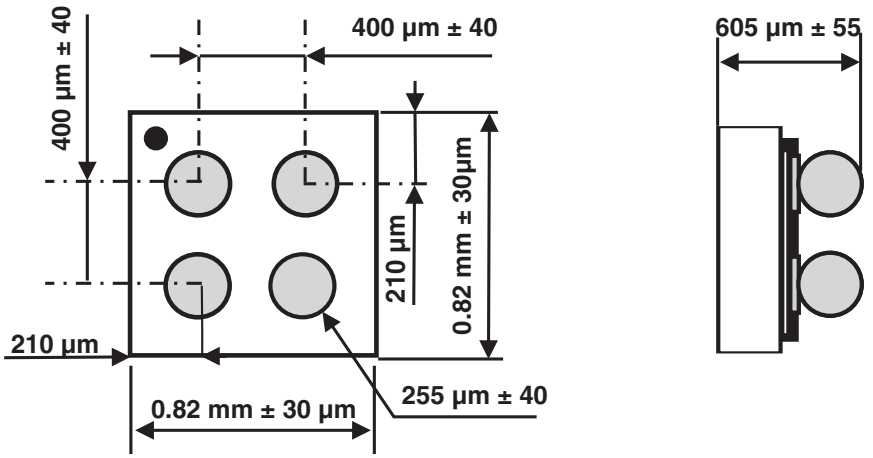


Figure 18. Footprint recommendations

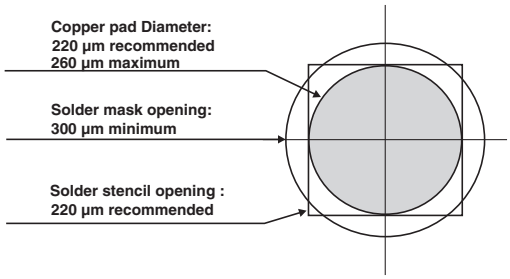
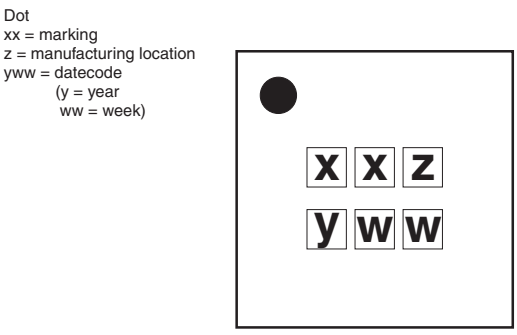
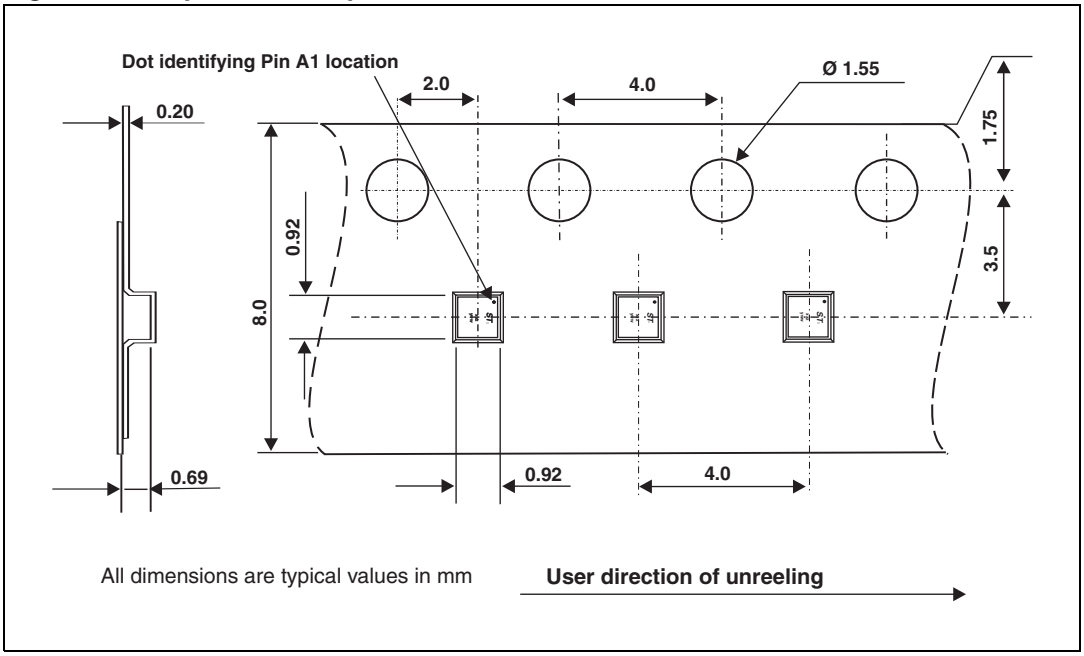


Figure 19. Marking



5 Tape and reel specification

Figure 20. Tape and reel specifications



6 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-3F3	EV	Flip Chip	0.86 mg	5000	Tape and reel

7 Revision history

Table 4. Document revision history

Date	Revision	Changes
01-Jul-2010	1	Initial release.
28-Mar-2012	2	Updated pin references in *Table 2*. Corrected units for I_{pp} in *Table 1*. Updated *Figure 20* for device pitch.

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