



# STS14N3LLH5

N-channel 30 V, 0.005  $\Omega$ , 14 A, SO-8  
STripFET™ V Power MOSFET

## Features

| Type        | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub>      |
|-------------|------------------|---------------------|---------------------|
| STS14N3LLH5 | 30 V             | <0.006 $\Omega$     | 14 A <sup>(1)</sup> |

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Application

- Switching applications

## Description

This product utilizes the 5<sup>th</sup> generation of design rules of ST's proprietary STripFET™ technology. The lowest available R<sub>DS(on)</sub> \* Q<sub>g</sub>, in SO-8 package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

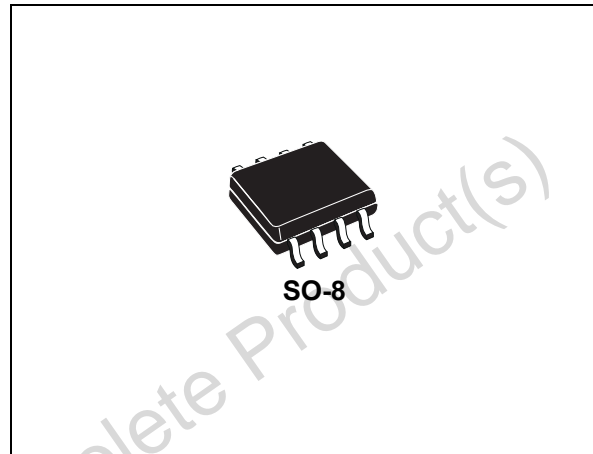


Figure 1. Internal schematic diagram

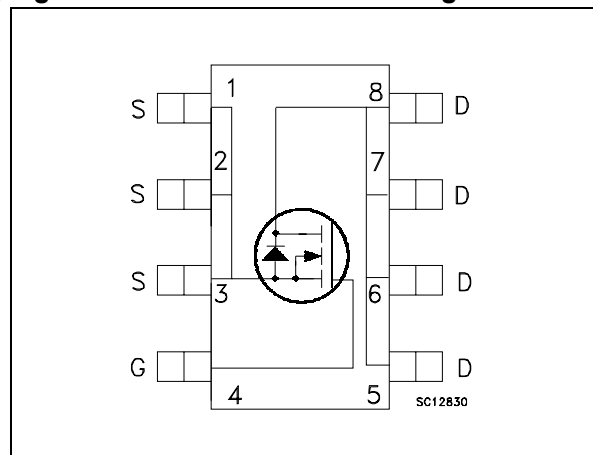


Table 1. Device summary

| Order code  | Marking | Package | Packaging     |
|-------------|---------|---------|---------------|
| STS14N3LLH5 | 14D3L   | SO-8    | Tape and reel |

# Contents

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Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol          | Parameter   | Value      | Unit                |
|-----------------|---|------------|---------------------|
| $V_{DS}$        | Drain-source voltage ( $V_{GS} = 0$ )                           | 30         | V                   |
| $V_{GS}$        | Gate-source voltage   | $\pm 22$   | V                   |
| $I_D^{(1)}$     | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 14         | A                   |
| $I_D^{(1)}$     | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 8.75       | A                   |
| $I_{DM}^{(2)}$  | Drain current (pulsed)  | 56         | A                   |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$           | 2.7        | W                   |
|                 | Derating factor   | 0.02       | W/ $^\circ\text{C}$ |
| $T_J$           | Operating junction temperature                                  | -55 to 150 | $^\circ\text{C}$    |
| $T_{stg}$       | Storage temperature   |            |                     |

1. The value is rated according  $R_{thj-pcb}$
2. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

| Symbol              | Parameter                           | Value | Unit                      |
|---------------------|-------------------------------------|-------|---------------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-ambient | 47    | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{sec}$

**Table 4. Avalanche data**

| Symbol   | Parameter   | Value | Unit |
|----------|---|-------|------|
| $I_{AV}$ | Not-repetitive avalanche current,<br>(pulse width limited by $T_J \text{ Max}$ )  | 8.5   | A    |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 24\text{ V}$ ) | 180   | mJ   |

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

| Symbol        | Parameter  | Test conditions  | Min. | Typ.            | Max.            | Unit                 |
|---------------|--|--|------|-----------------|-----------------|----------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 250 \mu A, V_{GS} = 0$  | 30   |                 |                 | V                    |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{max rating},$<br>$V_{DS} = \text{max rating} @ 125^{\circ}C$ |      |                 | 1<br>10         | $\mu A$<br>$\mu A$   |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 22 V$  |      |                 | $\pm 100$       | nA                   |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}, I_D = 250 \mu A$   | 1    |                 |                 | V                    |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10 V, I_D = 7 A$<br>$V_{GS} = 4.5 V, I_D = 7 A$                    |      | 0.005<br>0.0062 | 0.006<br>0.0077 | $\Omega$<br>$\Omega$ |

**Table 6. Dynamic**

| Symbol    | Parameter                    | Test conditions                                     | Min. | Typ. | Max. | Unit     |
|-----------|------------------------------|---|------|------|------|----------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 25 V, f = 1 \text{ MHz},$<br>$V_{GS} = 0$ | -    | 1500 |      | pF       |
| $C_{oss}$ | Output capacitance           |   |      | 295  |      | pF       |
| $C_{rss}$ | Reverse transfer capacitance |   |      | 39   |      | pF       |
| $R_G$     | Intrinsic gate resistance    | $f = 1 \text{ MHz open drain}$                      |      | 1    | 1.25 | $\Omega$ |
| $Q_g$     | Total gate charge            | $V_{DD} = 15 V, I_D = 14 A$                         | -    | 12   | 14.5 | nC       |
| $Q_{gs}$  | Gate-source charge           | $V_{GS} = 4.5 V$                                    |      | 4    |      | nC       |
| $Q_{gd}$  | Gate-drain charge            | (see Figure 14)                                     |      | 4.7  |      | nC       |

**Table 7. Switching times**

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD}=15\text{ V}$ , $I_D=7\text{ A}$ ,<br>$R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$<br><i>(see Figure 13)</i> |      | 9.3  |      | ns   |
| $t_r$        | Rise time           |   | -    | 14.5 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |   |      |      | 22.7 | ns   |
| $t_f$        | Fall time           |   |      |      | 4.5  | ns   |

**Table 8. Source drain diode**

| Symbol          | Parameter                     | Test conditions  | Min | Typ. | Max | Unit |
|-----------------|-------------------------------|--|-----|------|-----|------|
| $I_{SD}$        | Source-drain current          |  | -   |      | 14  | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -   |      | 56  | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 14\text{ A}$ , $V_{GS}=0$  | -   |      | 1.1 | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 14\text{ A}$ ,<br>$di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 25\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ |     | 25   |     | ns   |
| $Q_{rr}$        | Reverse recovery charge       |  | -   | 17.5 |     | nC   |
| $I_{RRM}$       | Reverse recovery current      |  |     |      | 1.4 | A    |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

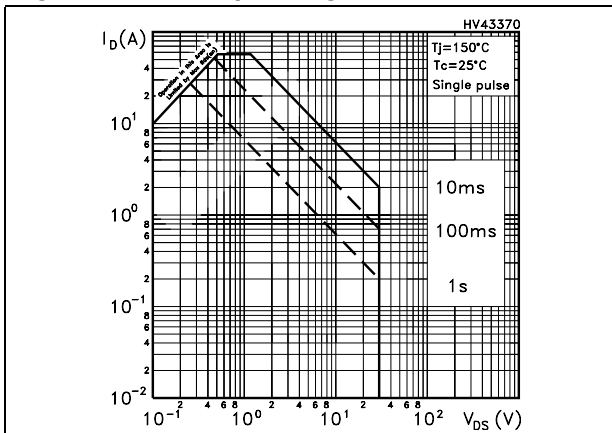


Figure 3. Thermal impedance

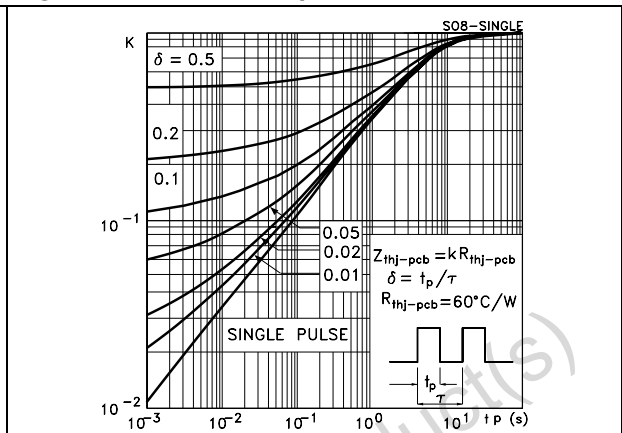


Figure 4. Output characteristics

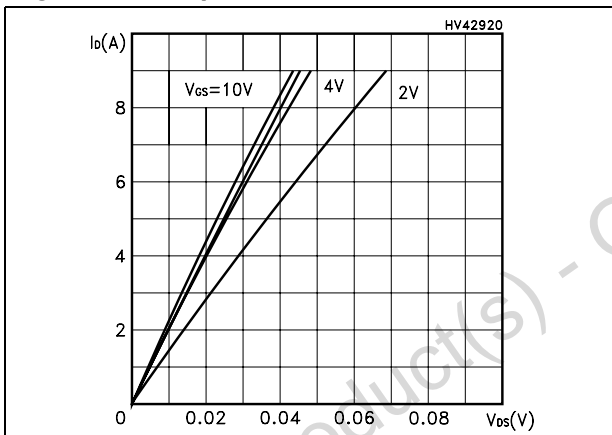


Figure 5. Transfer characteristics

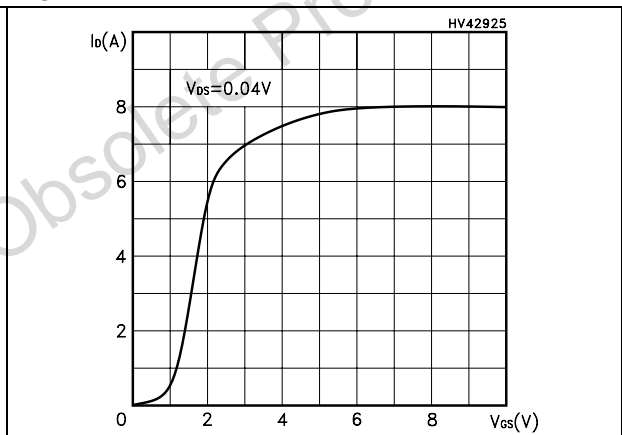


Figure 6. Normalized  $B_{V_{DS}}$  vs temperature

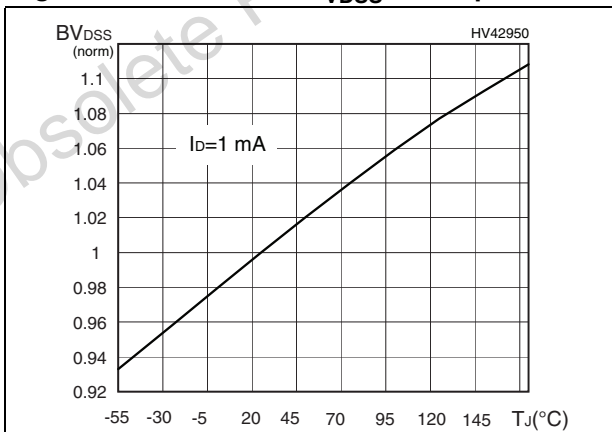


Figure 7. Static drain-source on resistance

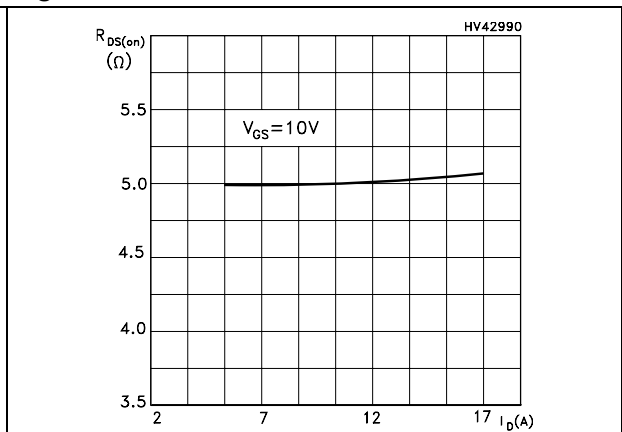


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

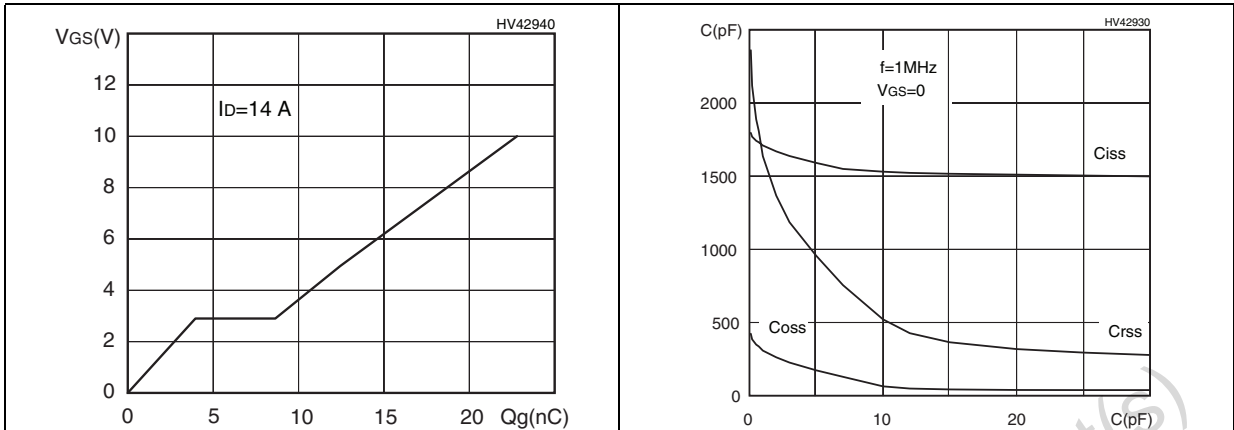


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

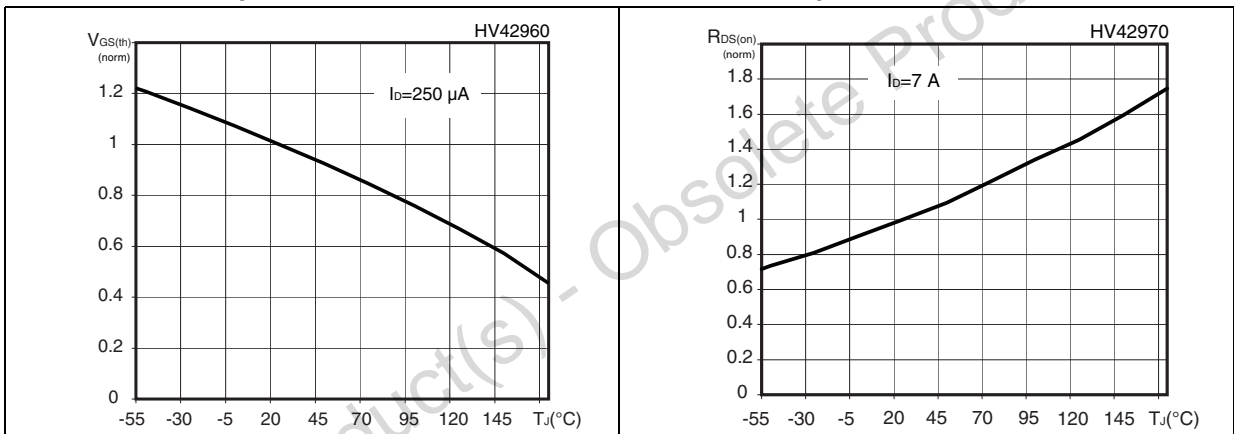
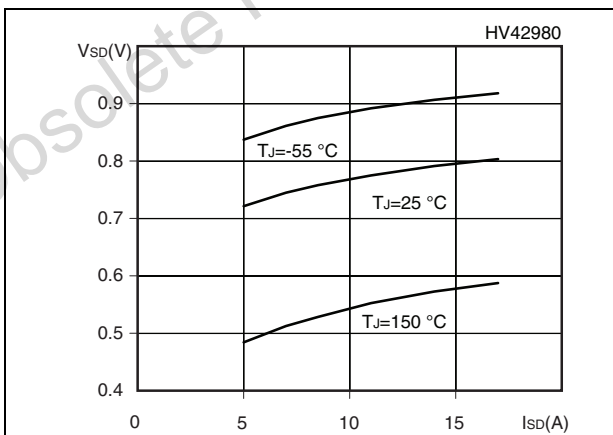
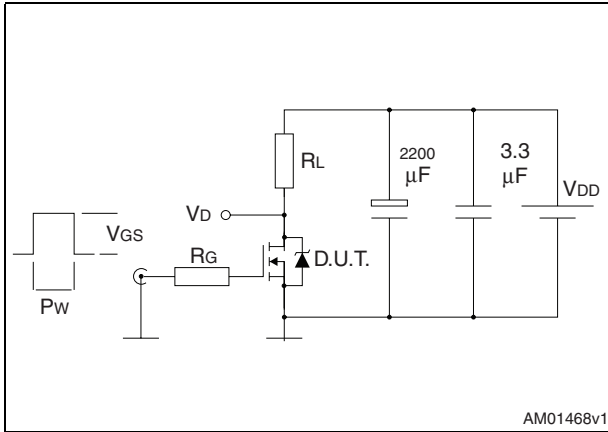


Figure 12. Source-drain diode forward characteristics



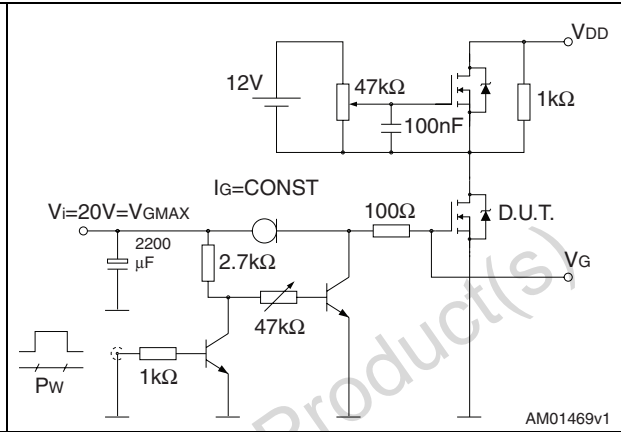
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



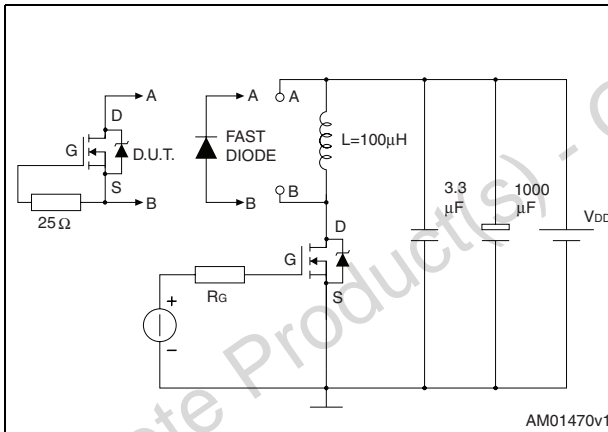
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**Figure 14. Gate charge test circuit**



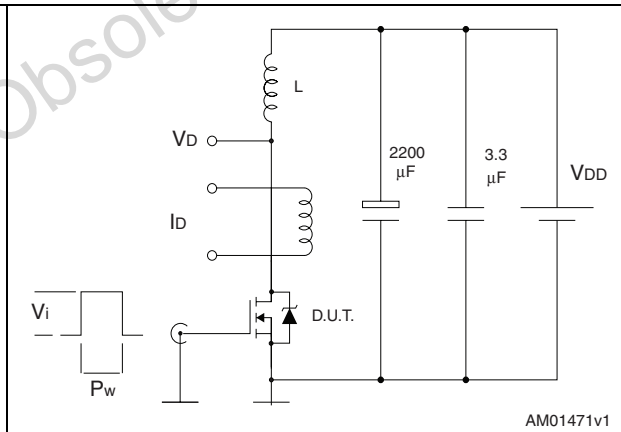
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



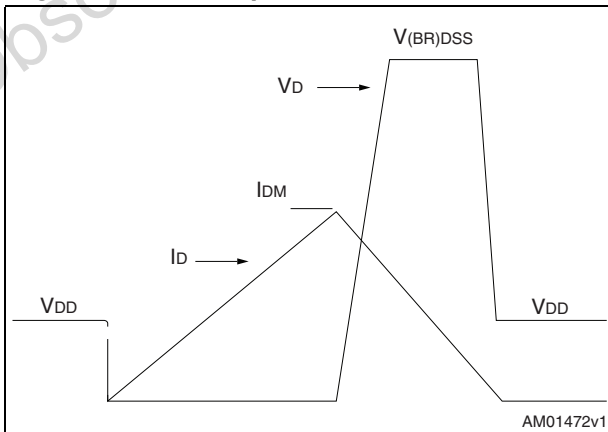
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**Figure 16. Unclamped inductive load test circuit**



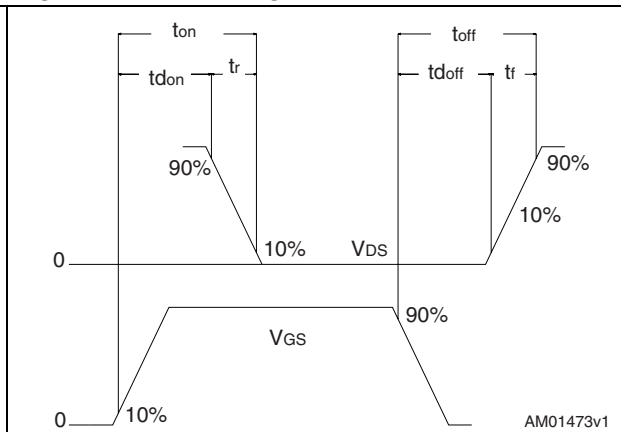
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**Figure 17. Unclamped inductive waveform**



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**Figure 18. Switching time waveform**



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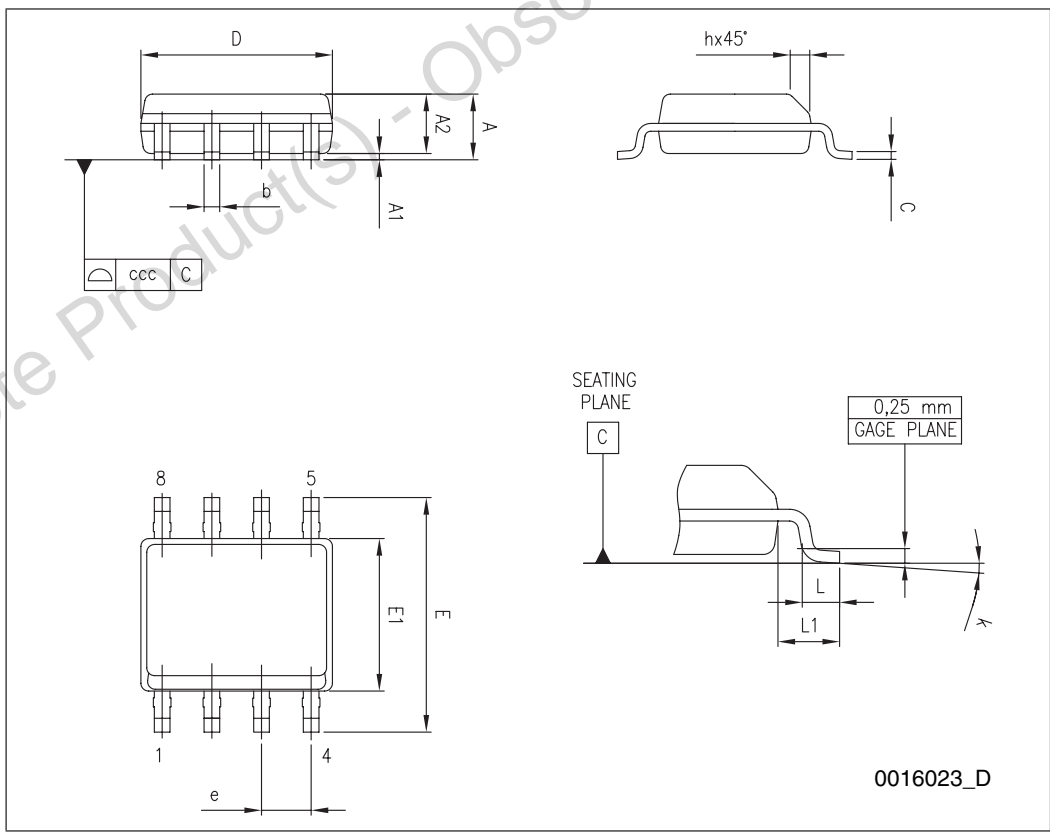
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

**SO-8 mechanical data**

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    |      |      | 1.75 |
| A1   | 0.10 |      | 0.25 |
| A2   | 1.25 |      |      |
| b    | 0.28 |      | 0.48 |
| c    | 0.17 |      | 0.23 |
| D    | 4.80 | 4.90 | 5.00 |
| E    | 5.80 | 6.00 | 6.20 |
| E1   | 3.80 | 3.90 | 4.00 |
| e    |      | 1.27 |      |
| h    | 0.25 |      | 0.50 |
| L    | 0.40 |      | 1.27 |
| L1   |      | 1.04 |      |
| k    | 0°   |      | 8°   |
| ccc  |      |      | 0.10 |



## 5 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 12-Nov-2007 | 1        | First release  |
| 15-Apr-2008 | 2        | – Updated <a href="#">Figure 1: Internal schematic diagram</a><br>– Document status promoted from preliminary data to datasheet. |
| 23-Sep-2008 | 3        | $V_{GS}$ value has been changed on <a href="#">Table 2</a> and <a href="#">Table 5</a>   |
| 19-Nov-2009 | 4        | – Added $Q_g$ max. value in <a href="#">Table 6</a><br>– Added new row in <a href="#">Table 6</a>                                |

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