NCN7200MTGEVB

NCN7200 Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

OVERVIEW

This document gives a detailed description of the NCN7200 Evaluation Board with the bill of materials, board schematic, and a layout overview of the board. The appropriate lab test setups are also provided.

The NCN7200 Evaluation Board has been designed for a quick evaluation of the NCN7200 Gigabit Ethernet LAN Switch with 2:1 Mux/Demux and Power-down Feature. Among its main characteristics, this evaluation board has been constructed to easily interface with the customer's systems and equipment through Ethernet connectors as well as SMA connectors.

This document must be used with the NCN7200 datasheet available on www.onsemi.com. The datasheet contains full technical details about the NCN7200 specifications and operation. The board is implemented in four metal layers with FR-4 dielectric. The total PCB thickness is 1.62 mm with dimensions of 51 mm by 133 mm.

This evaluation board can be used to evaluate the device performance and it allows the user to place the NCN7200 device in a real application environment. When the intention is to evaluate the device considering the specifications given in the datasheet, it is important to take into account the additional circuitry which may include changes in the input impedance matching and termination.

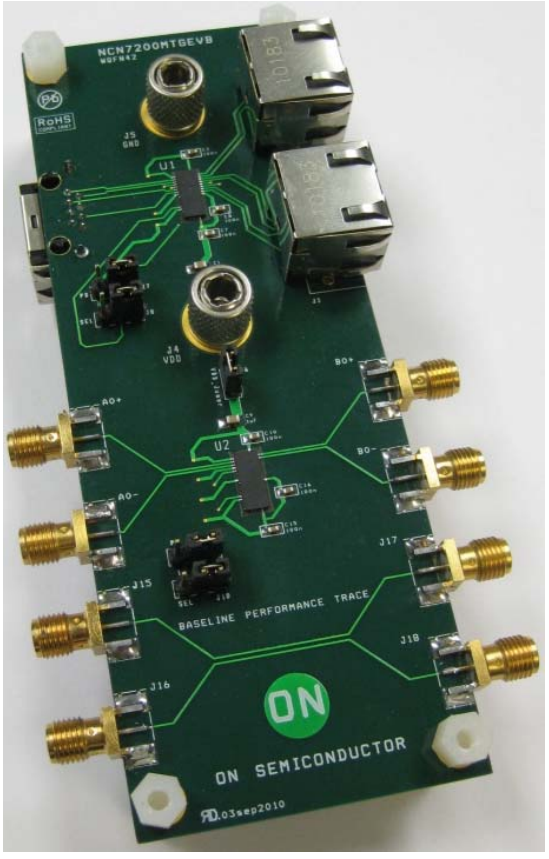

Figure 1. NCN7200 Evaluation Board

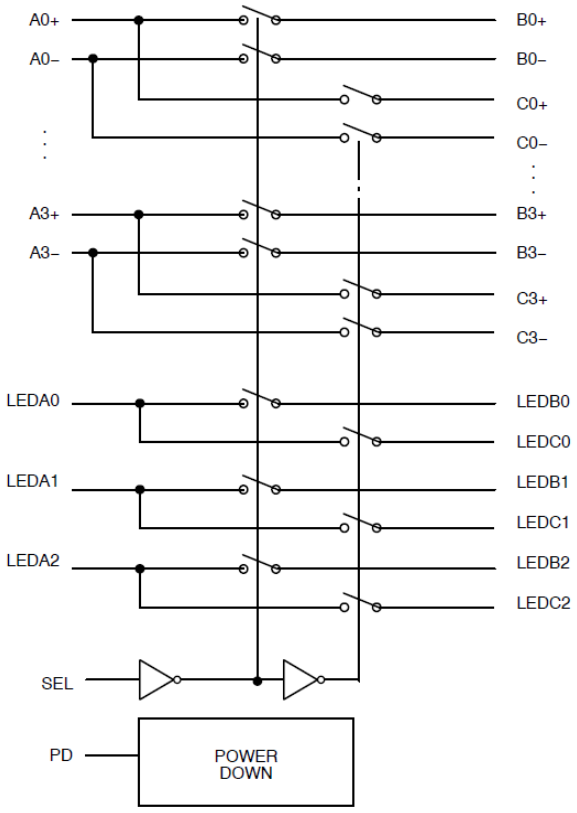

Figure 2. Block Diagram

TRUTH TABLE

PD	SEL	Function
L	L	AX to BX: LEDAX to LEDBX
L	H	AX to CX: LEDAX to LEDCX
H	X	Hi−Z

EQUIPMENT

The following table details the equipment used in the context of this application note manual:

TABLE 2. EQUIPMENT

Description	Quantity
Regulated DC Power Supply	1
Banana Cable	2
Oscilloscope with SMA Adapters	1
Differential Waveform Generator	1
SMA Cable	2−4
Ethernet Cable	2−3
Computer with Ethernet Port	1

GET STARTED…

This demo board features three sections. Refer to Figure 3 on the next page.

Section 1: A half pin-out (differential channels A0+/- and A1+/-) of the device with Ethernet jacks

1. Use the regulated DC power supply to set V_{DD} = 3.3 V. Connect the supply between the V_{DD} and GND banana connectors on the PCB using the banana cables.
2. Connect one of the Ethernet Cables between the Ethernet port on the computer and the Common I/O J1.
3. Connect the second Ethernet Cable from the desired I/O at J2 or J3 to a network internet connection. Adjust the Logic Controls PD and SEL for the desired output.
4. When the switch is turned on between the computer and the network connection, use the detected network to confirm operation of the device by accessing the internet.

Section 2: A single differential pair with SMA connectors

1. Use the regulated DC power supply to set V_{DD} = 3.3 V. Connect the supply between the V_{DD} and GND banana connectors on the PCB using the banana cables.
2. Use the jumper to connect the pins on J6 to power the second device U2.
3. Use the SMA cables to connect the Waveform Generator to A0+/- connectors and the Oscilloscope to the B0+/- connectors. Adjust the Logic Controls PD and SEL for the desired output.
4. Set the waveform generator to the desired bit rate up to 1 Gbps (1000BASE-T) and amplitude up to 3 Vpp per differential channel.
5. Observe the output at the oscilloscope.

Section 3: A pass-through on the board for baseline measurements with SMA connectors

1. Use the SMA cables to connect the Waveform Generator to connectors J15 and J16, and connect the Oscilloscope to connectors J17 and J18. Adjust the Logic Controls PD and SEL for the desired output.
2. Set the waveform generator to the desired bit rate up to 1 Gbps (1000BASE-T) and any nominal amplitude.
3. Observe the output at the oscilloscope.

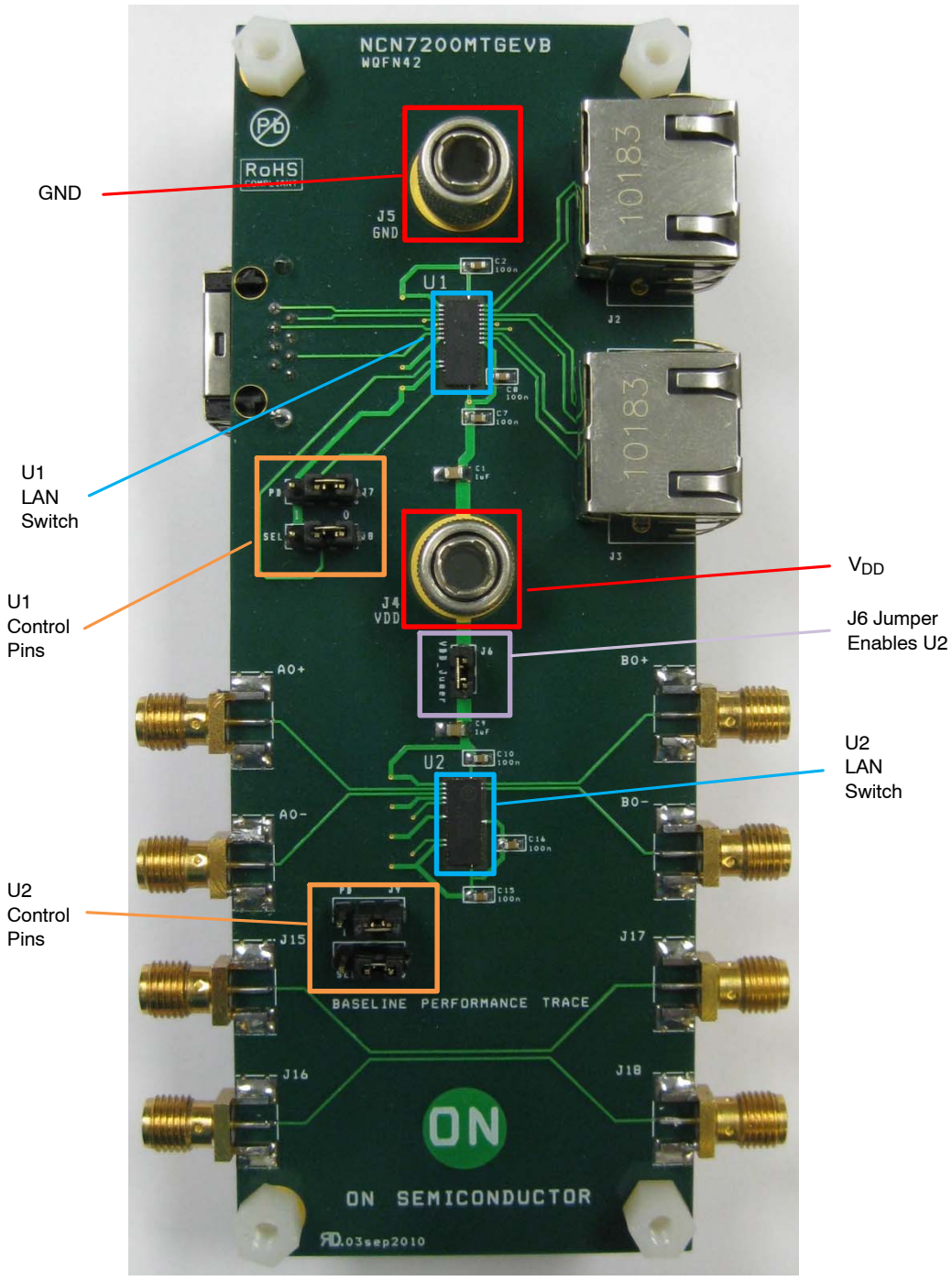

Figure 3. Key Features of the NCN7200 Evaluation Board

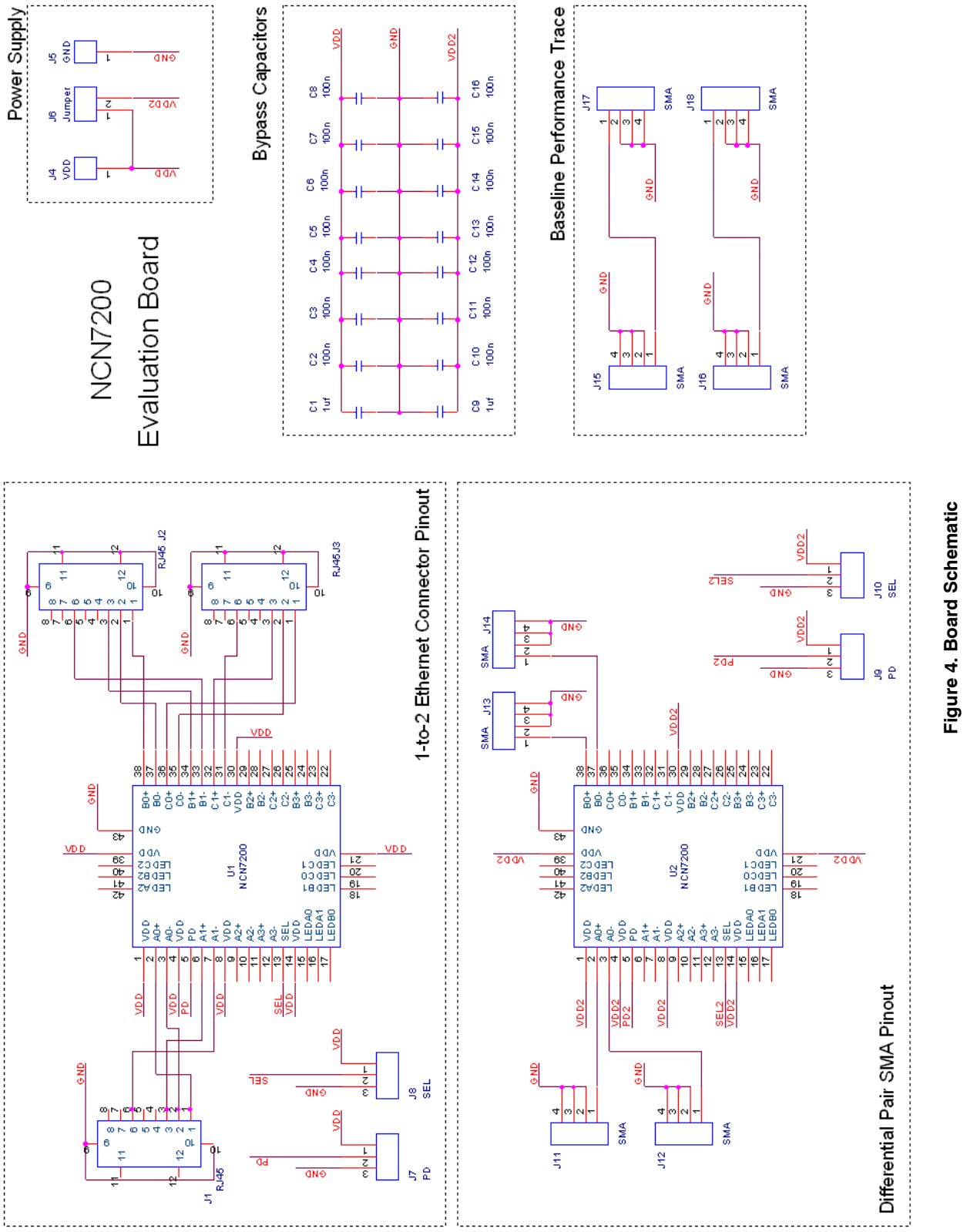

Figure 4. Board Schematic

BILL OF MATERIALS

The bill of materials is shown in Table 3. All components used are entirely lead-free and RoHS compliant.

Table 3. Bill of Materials

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
U1, U2	2	NCN7200 Gigabit Ethernet LAN Switch	n/a	n/a	WQFN42	ON Semiconductor	NCN7200MTTWG
J1, J2, J3	3	Conn Mod Jack 8Pos	n/a	n/a	RJ45	Tyco Electronics	1-406541-1
J4, J5	2	Banana Connector	n/a	n/a	7mm Hole	Johnson Components	111-2223-001
J6	1	2-Pin Header	n/a	n/a	Header2	Tyco Electronics	5-826629-0
J7, J8, J9, J10	4	3-Pin Header	n/a	n/a	Header3	Tyco Electronics	5-826629-0
J11, J12, J13, J14, J15, J16, J17, J18	8	SMA Jack - PCB End Launch	n/a	n/a	SMA	Emerson Network Power Connectivity	142-0711-821
C1, C9	2	Ceramic Capacitor SMD	1uF	10%	0805	Murata	GRM155R60J105
C2, C3, C4, C5, C6, C7, C8, C10, C11, C12, C13,C14, C15, C16	14	Ceramic Capacitor SMD	.01uF	10%	0603	AVX	06031C103KAT2A
F1, F2, F3, F4	4	Nylon Standoff Hex, 6-32THR, .500”L	n/a	n/a	HOLE	Keystone Electronics	1903C
F1, F2, F3, F4	4	Nylon Standoff Hex M/F, 6-32, .250”L	n/a	n/a	HOLE	Keystone Electronics	4814

PCB DESIGN

The evaluation board layout is shown in Figure 5. In the figure, traces in the top layer are magenta, while traces on the bottom layer are cyan. The board also has two grounded inner layers that are used to control the characteristic impedance of the signal traces at 50 Ω to maintain signal integrity. The total PCB thickness is 1.62 mm with dimensions of 51 mm by 133 mm.

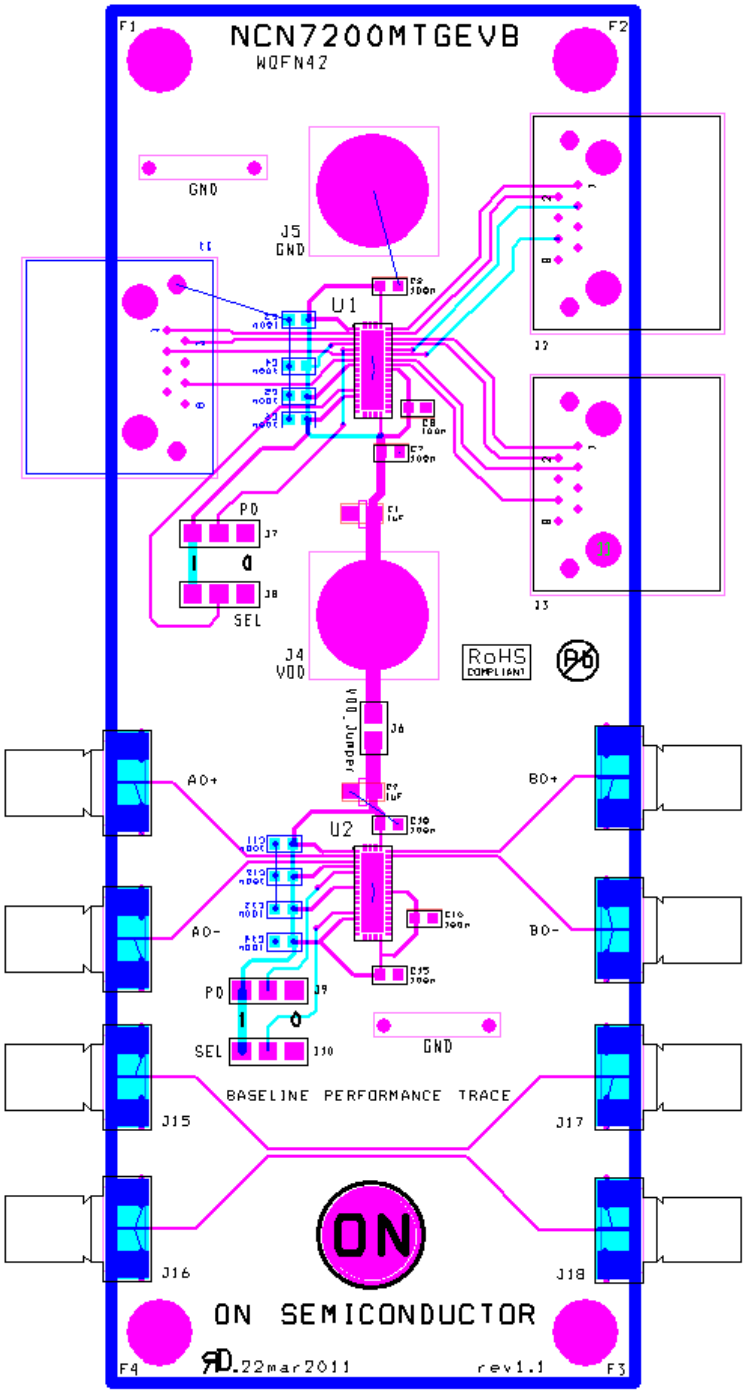

Figure 5. Evaluation Board Layout

ELECTRICAL LAYOUT CONSIDERATIONS

Implementing a high speed switch device requires careful PCB design to preserve signal integrity. The evaluation board serves as a layout example and can support the design engineers to preserve high speed performances.

Electrical layout guidelines:

- The bypass capacitor must be placed as close as possible to the V_{DD} input pin for noise immunity.
- The characteristic impedance of each segment must be 50 Ω single-ended and 100 Ω differential according to IEEE standard 802.3.
- The ground plane of the PCB will be used to determine the characteristic impedance of each line.
- All corresponding differential A+/− line segment pairs must be the same length.
- The use of vias to route these signals should be avoided when possible.
- The use of turns or bends to route these signals should be avoided when possible. When bends are needed, use 45° bends instead of 90° bends.

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