VNQ7050AJ-E

Quad channel high-side driver with CurrentSense analog feedback for automotive applications

Datasheet - production data

PowerSSO-16

GAPGCFT00327

Features

Max transient supply voltage	V_{CC}	40 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per Ch)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	27 A
Stand-by current (max)	I_{STBY}	0.5 µA

- Automotive qualified
- General
  - Quad channel smart high-side driver with CS analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
  - Analog feedback of load current with high precision proportional current mirror
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Sense enable/disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
  - Loss of ground and loss of V_{CC}
  - Reverse battery with external components
  - Electrostatic discharge protection

Applications

- All types of automotive resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps (up to P27W or SAE1156 or LED Real Combinations)

Description

The VNQ7050AJ-E is a quad channel high-side driver manufactured using ST proprietary VIPower® technology and housed in PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A sense enable pin allows OFF-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

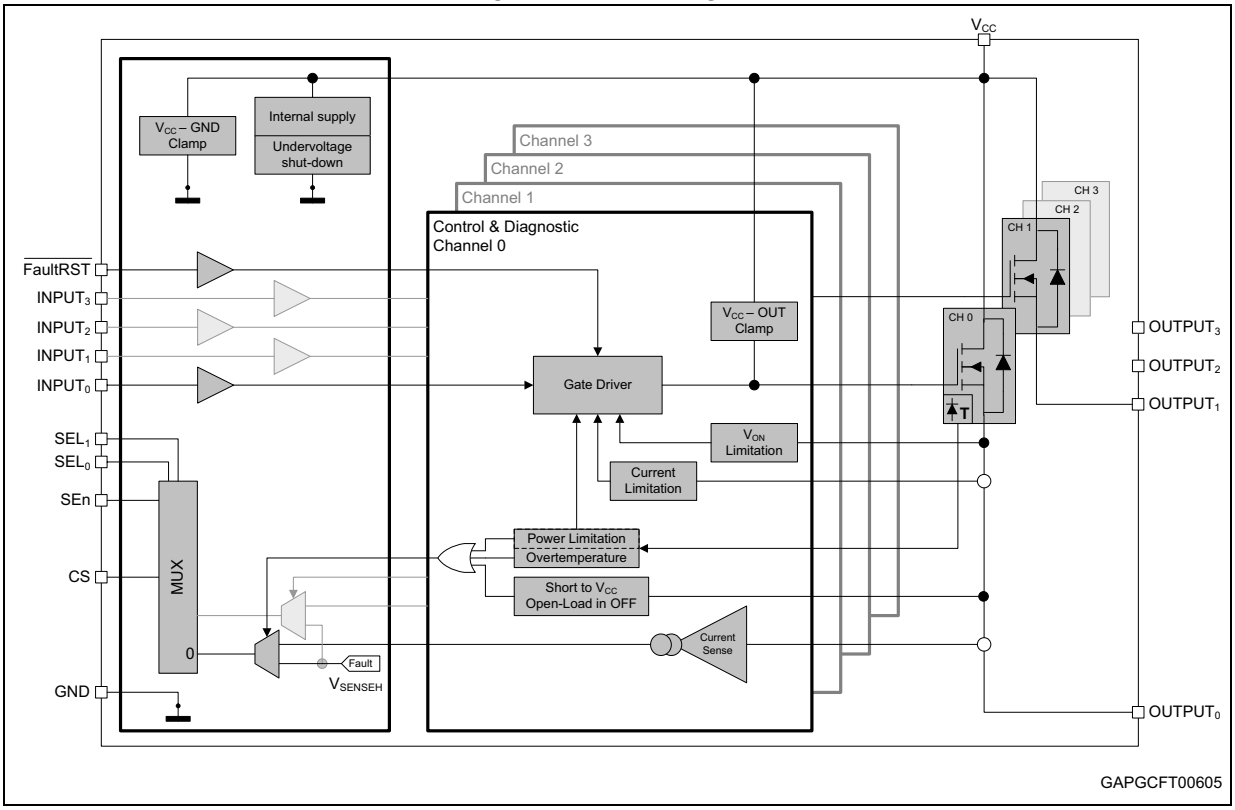


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection.
$OUTPUT_{0,1,2,3}$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
$INPUT_{0,1,2,3}$	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state.
CS	Analog current sense output pin delivers a current proportional to the load current.
SEn	Active high, compatible with 3 V and 5 V CMOS outputs input pin; it enables the CS diagnostic pin.
$SEL_{0,1}$	Active high, compatible with 3 V and 5 V CMOS outputs input pin; They address the CS multiplexer.
FaultRST	Active low, compatible with 3 V and 5 V CMOS outputs input pin; it unlatches the output in case of fault; If kept low, sets the outputs in auto-restart mode.

Figure 2. Configuration diagram (top view)

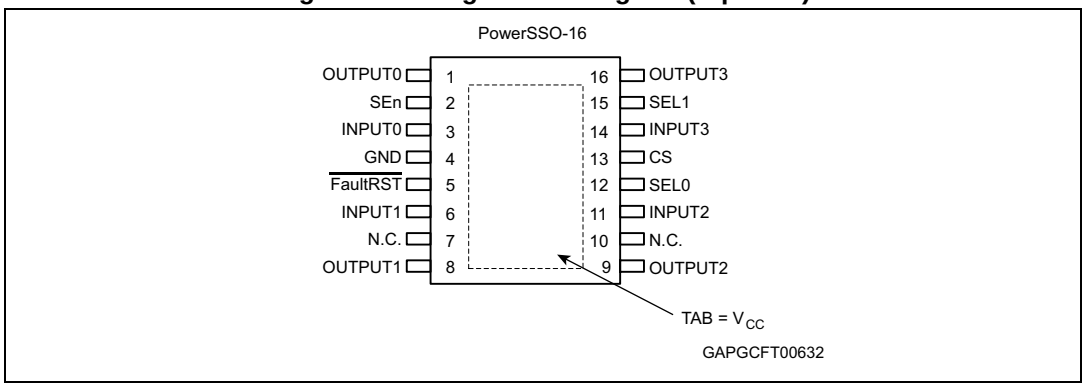


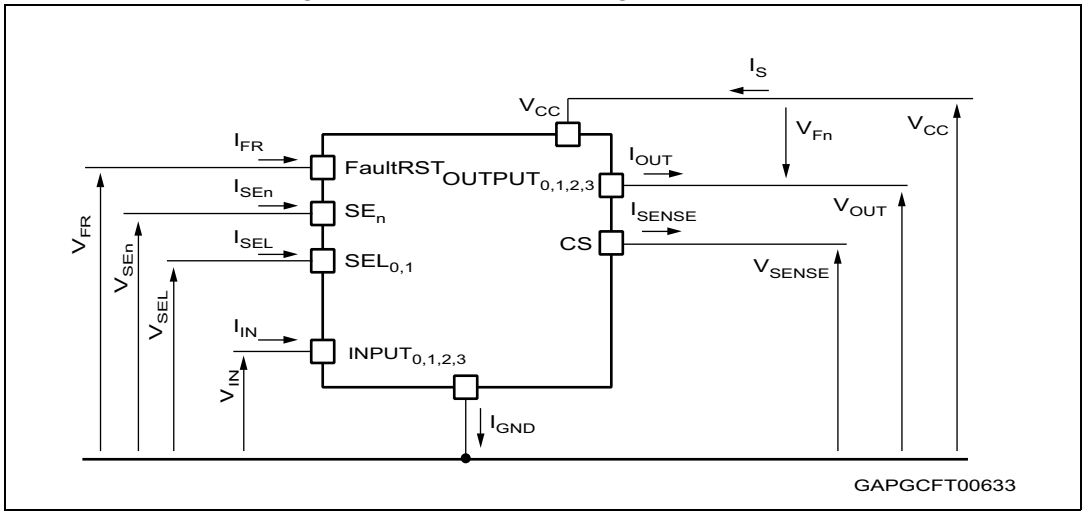
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CS	N.C.	Output	Input	SEn, SELx, FaultRST
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1 kΩ resistor	X	Not allowed	Through 15 kΩ resistor	Through 15 kΩ resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



Note: *$V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.*

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	38	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCPK}	Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; R_L = 4 Ω)	40	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	$OUTPUT_{0,1,2,3}$ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	16	
I_{IN}	$INPUT_{0,1,2,3}$ DC input current	-1 to 10	mA
I_{SEn}	SEn DC input current		
I_{SEL}	$SEL_{0,1}$ DC input current		
I_{FR}	FaultRST DC input current		
V_{FR}	FaultRST DC input voltage	7.5	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
I_{SENSE}	CS pin DC output current (V_{GND} = V_{CC} and V_{SENSE} < 0 V)	10	mA
	CS pin DC output current in reverse (V_{CC} < 0 V)	-20	
E_{MAX}	Maximum switching energy (single pulse) (T_{DEMAG} = 0.4 ms; T_{jstart} = 150°C)	30	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F) – $INPUT_{0,1,2,3}$ – CS – SEn, $SEL_{0,1}$, FaultRST – $OUTPUT_{0,1,2,3}$ – V_{CC}	 4000 2000 4000 4000 4000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}board}$	Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8)(1)(2)	6.3	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3)	57.3	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2)	23.5	

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB.
3. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace.

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown				4	
$V_{USDReset}$	Undervoltage shutdown reset				5	
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		
R_{ON}	On-state resistance(1)	I_{OUT} = 2 A; T_j = 25°C		50		mΩ
		I_{OUT} = 2 A; T_j = 150°C			100	
		I_{OUT} = 2 A; V_{CC} = 4 V; T_j = 25°C			75	
V_{clamp}	Clamp voltage	I_S = 20 mA; T_j = -40°C	38			V
		I_S = 20 mA; 25°C < T_j < 150°C	41	46	52	
I_{STBY}	Supply current in Standby at V_{CC} = 13 V(2)	V_{CC} = 13 V; $V_{IN} = V_{OUT} = V_{FR} = V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 25°C			0.5	µA
		V_{CC} = 13 V; $V_{IN} = V_{OUT} = V_{FR} = V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 85°C (3)			0.5	µA
		V_{CC} = 13 V; $V_{IN} = V_{OUT} = V_{FR} = V_{SEn}$ = 0 V; $V_{SEL0,1}$ = 0 V; T_j = 125°C			3	µA
t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V $V_{IN} = V_{OUT} = V_{FR} = V_{SEL0,1}$ = 0 V; V_{SEn} = 5 V to 0 V	60	300	550	µs
$I_{S(ON)}$	Supply current	V_{CC} = 13 V; $V_{SEn} = V_{FR} = V_{SEL0,1}$ = 0 V; $V_{IN0,1,2,3}$ = 5 V; $I_{OUT0,1,2,3}$ = 0 A		10	16	mA
$I_{GND(ON)}$	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; $V_{FR} = V_{SEL0,1}$ = 0 V; $V_{IN0,1,2,3}$ = 5 V; $I_{OUT0,1,2,3}$ = 1 A			20	mA
$I_{L(off)}$	Off-state output current at V_{CC} = 13 V(1)	$V_{IN} = V_{OUT}$ = 0 V; V_{CC} = 13 V; T_j = 25°C	0	0.01	0.5	µA
		$V_{IN} = V_{OUT}$ = 0 V; V_{CC} = 13 V; T_j = 125°C	0		3	
V_F	Output - V_{CC} diode voltage(1)	I_{OUT} = -2 A; T_j = 150°C			0.7	V

1. For each channel.
2. PowerMOS leakage included.
3. Parameter specified by design; not subject to production test.

Table 6. Switching (V_{CC} = 13 V; -40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(1)	Turn-on delay time at T_j = 25°C	R_L = 6.5 Ω	10	35	120	µs
$t_{d(off)}$(1)	Turn-off delay time at T_j = 25°C		10	45	100	
$(dV_{OUT}/dt)_{on}$(1)	Turn-on voltage slope at T_j = 25°C	R_L = 6.5 Ω	0.1	0.28	0.7	V/µs
$(dV_{OUT}/dt)_{off}$(1)	Turn-off voltage slope at T_j = 25°C		0.1	0.31	0.7	
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 6.5 Ω	—	0.26	0.35(2)	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 6.5 Ω	—	0.23	0.31(2)	mJ
t_{SKEW}(1)	Differential Pulse skew (t_{PHL} - t_{PLH})	R_L = 6.5 Ω	-40	10	60	µs

1. See *Figure 4: Switching times and Pulse skew*.
2. Parameter guaranteed by design and characterization, not subject to production test

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$INPUT_{0,1,2,3}$ characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
$\overline{FaultRST}$ characteristics						
V_{FRL}	Input low level voltage				0.9	V
I_{FRL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{FRH}	Input high level voltage		2.1			V
I_{FRH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{FR(hyst)}$	Input hysteresis voltage		0.2			V
V_{FRCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.5	V
		I_{IN} = -1 mA		-0.7		
$SEL_{0,1}$ characteristics (7 V < V_{CC} < 18 V)						
V_{SELL}	Input low level voltage				0.9	V
I_{SELL}	Low level input current	V_{IN} = 0.9 V	1			µA

Table 7. Logic Inputs (7 V < V_{CC} < 28 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SELH}	Input high level voltage		2.1			V
I_{SELH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEL(hyst)}$	Input hysteresis voltage		0.2			V
V_{SELCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V_{CC} < 18 V)						
V_{SEnL}	Input low level voltage				0.9	V
I_{SEnL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{SEnH}	Input high level voltage		2.1			V
I_{SEnH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{SEn(hyst)}$	Input hysteresis voltage		0.2			V
V_{SEnCL}	Input clamp voltage	I_{IN} = 1 mA	5.3		7.2	V
		I_{IN} = -1 mA		-0.7		

Table 8. Protections (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIMH}	DC short circuit current	V_{CC} = 13 V	21	27	38	A
		4 V < V_{CC} < 18 V(1)			38	
I_{LIML}	Short circuit current during thermal cycling	V_{CC} = 13 V; $T_R < T_j < T_{TSD}$		9		
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature(1)		T_{RS} + 1	T_{RS} + 7		
T_{RS}	Thermal reset of fault diagnostic indication	V_{FR} = 0 V; V_{SEn} = 5 V;	135			
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)(1)			7		
ΔT_{J_SD}	Dynamic temperature	T_j = -40°C; V_{CC} = 13 V		60		K
t_{LATCH_RST}	Fault reset time for output unlatch(1)	V_{FR} = 5 V to 0 V; V_{SEn} = 5 V – E.g. Ch_0 V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V	3	10	20	µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}= 2 A; L = 6 mH; T_j = -40°C	V_{CC} - 38			V
		I_{OUT}= 2 A; L = 6 mH; T_j = 25°C to 150°C	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.2 A		20		mV

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. CurrentSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CL}	Current sense clamp voltage	V_{SEn} = 0 V; I_{SENSE} = 1 mA	-17		-12	V
		V_{SEn} = 0 V; I_{SENSE} = -1 mA		7		
Current Sense characteristics						
K_{OL}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.01 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	425			
dK_{cal}/K_{cal} (1)(2)	Current sense ratio drift at calibration point	I_{OUT} = 0.01 A to 0.05 A; I_{cal} = 30 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_{LED}	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	530	1390	2120	
dK_{LED}/K_{LED} (1)(2)	Current sense ratio drift	I_{OUT} = 0.05 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-30		30	%
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	730	1280	1700	
dK_0/K_0 (1)(2)	Current sense ratio drift	I_{OUT} = 0.2 A; V_{SENSE} = 0.5 V; V_{SEn} = 5 V	-25		25	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 0.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	830	1180	1545	
dK_1/K_1 (1)(2)	Current sense ratio drift	I_{OUT} = 0.4 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-20		20	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	885	1120	1335	
dK_2/K_2 (1)(2)	Current sense ratio drift	I_{OUT} = 1.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-15		15	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 4.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	990	1110	1210	
dK_3/K_3 (1)(2)	Current sense ratio drift	I_{OUT} = 4.5 A; V_{SENSE} = 4 V; V_{SEn} = 5 V	-10		10	%

Table 9. CurrentSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	Current sense leakage current	Current sense disabled: V_{SEn} = 0 V;	0		0.5	µA
		Current sense disabled: -1 V < V_{SENSE} < 5 V(1)	-0.5		0.5	
		Current sense enabled: V_{SEn} = 5 V All channels ON; I_{OUTX} = 0 A; Ch_X diagnostic selected: – E.g. Ch_0: $V_{IN0,1,2,3}$ = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 0 A; $I_{OUT1,2,3}$ = 2 A	0		2	
		Current sense enabled: V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected: – E.g. Ch_0: V_{IN0} = 0 V; $V_{IN1,2,3}$ = 0 V; V_{SEL0} = 5V; V_{SEL1} = 0 V; $I_{OUT1,2,3}$ = 2 A	0		2	
V_{OUT_MSD}(1)	Output Voltage for Current sense shutdown	V_{SEn} = 5 V; R_{SENSE} = 2.7 kΩ – E.g. Ch_0: V_{IN0} = 5 V; V_{SEL0} = 0 V; V_{SEL1} = 0 V; I_{OUT0} = 2 A		5		V
V_{SENSE_SAT}	CS saturation voltage	V_{CC} = 7 V; R_{SENSE} = 2.7 KΩ; V_{SEn} = 5 V; V_{IN0} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 4.5 A; T_j = 150°C	5			V
I_{SENSE_SAT}(1)	CS saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	4			mA
I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V; V_{SENSE} = 4 V; V_{IN0} = 5 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; T_j = 150°C	4.8			A
OFF-state diagnostic						
V_{OL}	OFF-state open-load voltage detection threshold	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected – E.g: Ch_0 V_{IN0} = 0 V; $V_{SEL0,1}$ = 0 V	2	3	4	V
$I_{L(off2)}$	OFF-state output sink current	V_{IN} = 0 V; V_{OUT} = V_{OL}; T_j = -40°C to 125°C	-100		-15	µA

Table 9. CurrentSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see *Figure 6*)	V_{SEn} = 5 V; Ch_X ON to OFF transition; Ch_X diagnostic selected: – E.g: Ch_0 V_{IN0} = 5 V to 0 V; $V_{SEL0,1}$ = 0 V; V_{OUT0} = 4 V; I_{OUT0} = 0 A	100	350	700	µs
$t_{D\_OL\_V}$	Settling time for valid OFF-state open-load diagnostic indication from rising edge of SEn	$V_{IN0,1,2,3}$ = 0 V; V_{FR} = 0 V; $V_{SEL0,1}$ = 0 V; V_{OUT0} = 4 V; V_{SEn} = 0 V to 5 V			60	µs
t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	V_{SEn} = 5 V; Ch_X OFF; Ch_X diagnostic selected: – E.g: Ch_0 V_{IN0} = 0 V; $V_{SEL0,1}$ = 0 V; V_{OUT0} = 0 V to 4 V		5	30	µs
Fault diagnostic feedback (see *Table 10*)						
V_{SENSEH}	Current sense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 1 kΩ – E.g: Ch_0 in open load V_{IN0} = 0 V; V_{SEn} = 5 V; $V_{SEL0,1}$ = 0 V; I_{OUT0} = 0 A; V_{OUT0} = 4 V	5		6.6	V
I_{SENSEH}	Current sense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V	7	20	30	mA
Current sense timings (current sense mode - see *Figure 5*)						
$t_{DSENSE1H}$	Current sense settling time from rising edge of SEn	V_{IN} = 5 V; V_{SEn} = 0 V to 5 V; R_{SENSE} = 1 kΩ; R_L = 6.5 Ω			60	µs
$t_{DSENSE1L}$	Current sense disable delay time from falling edge of SEn	V_{SEn} = 5 V to 0 V; R_{SENSE} = 1 kΩ; R_L = 6.5 Ω		5	20	µs
$t_{DSENSE2H}$	Current sense settling time from rising edge of INPUT	V_{IN} = 0 V to 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 6.5 Ω		100	250	µs
$\Delta t_{DSENSE2H}$	Current sense settling time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	V_{IN} = 5 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; I_{SENSE} = 90 % of $I_{SENSEMAX}$; R_L = 6.5 Ω			100	µs
$t_{DSENSE2L}$	Current sense turn-off delay time from falling edge of INPUT	V_{IN} = 5 V to 0 V; V_{SEn} = 5 V; R_{SENSE} = 1 kΩ; R_L = 6.5 Ω		50	250	µs

1. Parameter defined by design. Not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Figure 4. Switching times and Pulse skew

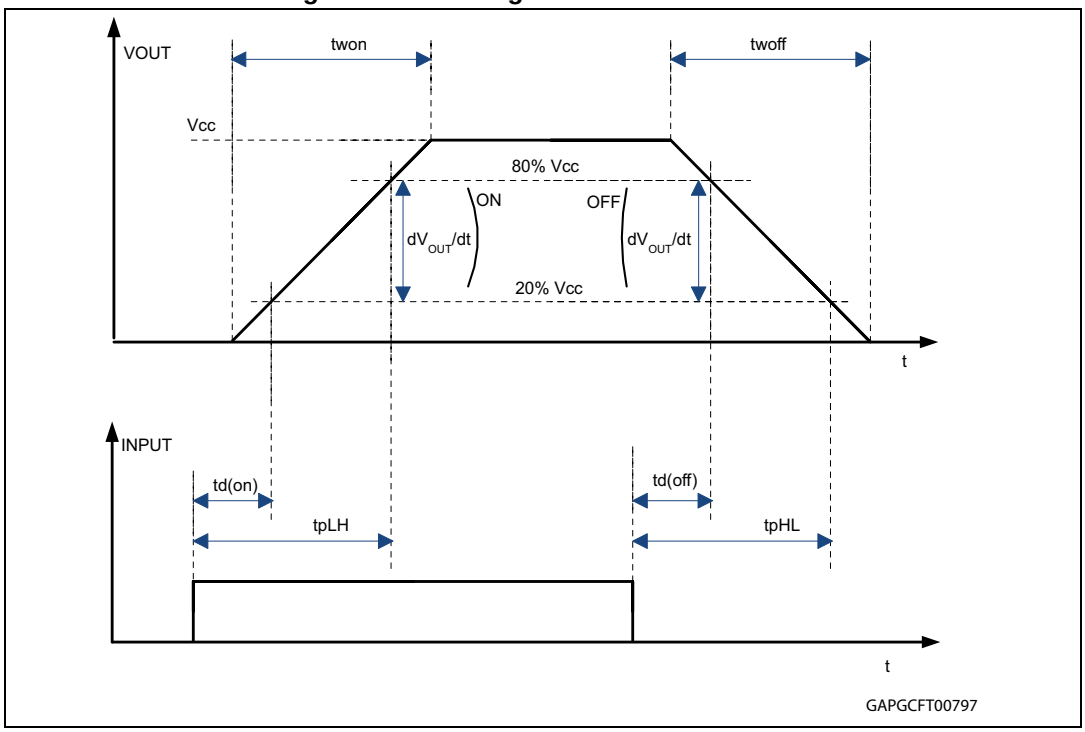


Figure 5. Current sense timings (current sense mode)

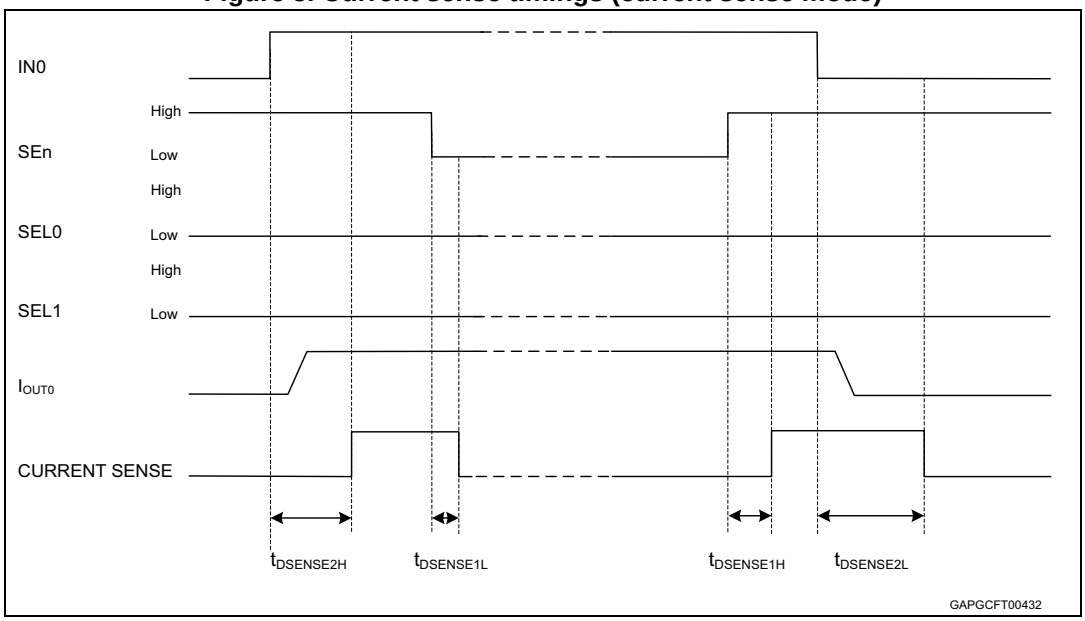


Figure 6. T_{DSKON}

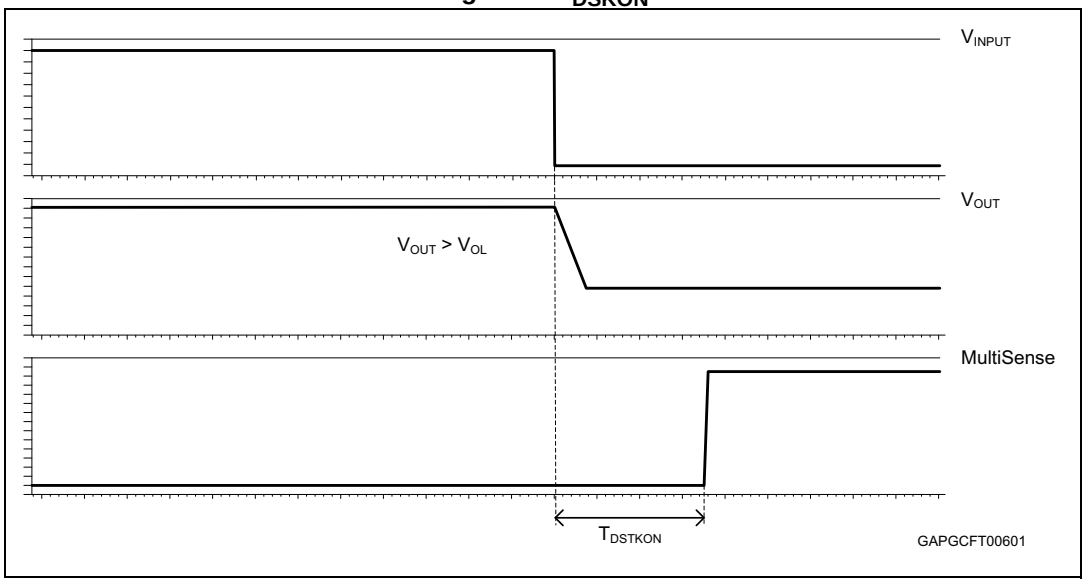


Table 10. Truth table

Mode	Conditions	IN_X	FR	SEn	SEL_X	OUT_X	Current sense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; T_j < 150°C	L	X	Refer to *Table 11*		L	Refer to *Table 11*	
		H	L			H		Outputs configured for auto-restart
		H	H			H		Outputs configured for Latch-off
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	X	Refer to *Table 11*		L	Refer to *Table 11*	
		H	L			H		Output cycles with temperature hysteresis
		H	H			L		Output latches-off
Under-voltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	X	L L	Hi-Z Hi-Z	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	Refer to *Table 11*		H	Refer to *Table 11*	
	Open-load	L	X			H		External pull-up
Negative output voltage	Inductive loads turn-off	L	X	Refer to *Table 11*		< 0 V	Refer to *Table 11*	

Table 11. Current sense multiplexer addressing

SEn	SEL_1	SEL_0	MUX channel	Current sense output			
				Nomal mode	Overload	OFF-state diag.(1)	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	Channel 1 diagnostic	I_{SENSE} = 1/K * I_{OUT1}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	L	Channel 2 diagnostic	I_{SENSE} = 1/K * I_{OUT2}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	H	Channel 3 diagnostic	I_{SENSE} = 1/K * I_{OUT3}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z

1. In case the output channel corresponding to the selected MUX channel is latched off while the relevant input is low, CS pin delivers feedback according to OFF-State diagnostic.
Example 1: FR = 1; IN_0 = 0; OUT_0 = L (latched); MUX channel = channel 0 diagnostic; CS = 0
Example 2: FR = 1; IN_0 = 0; OUT_0 = latched, $V_{OUT0} > V_{OL}$; MUX channel = channel 0 diagnostic; CS = V_{SENSEH}

2.4 Waveforms

Figure 7. Latch functionality - behavior in hard short circuit condition (T_{AMB} << T_{TSD})

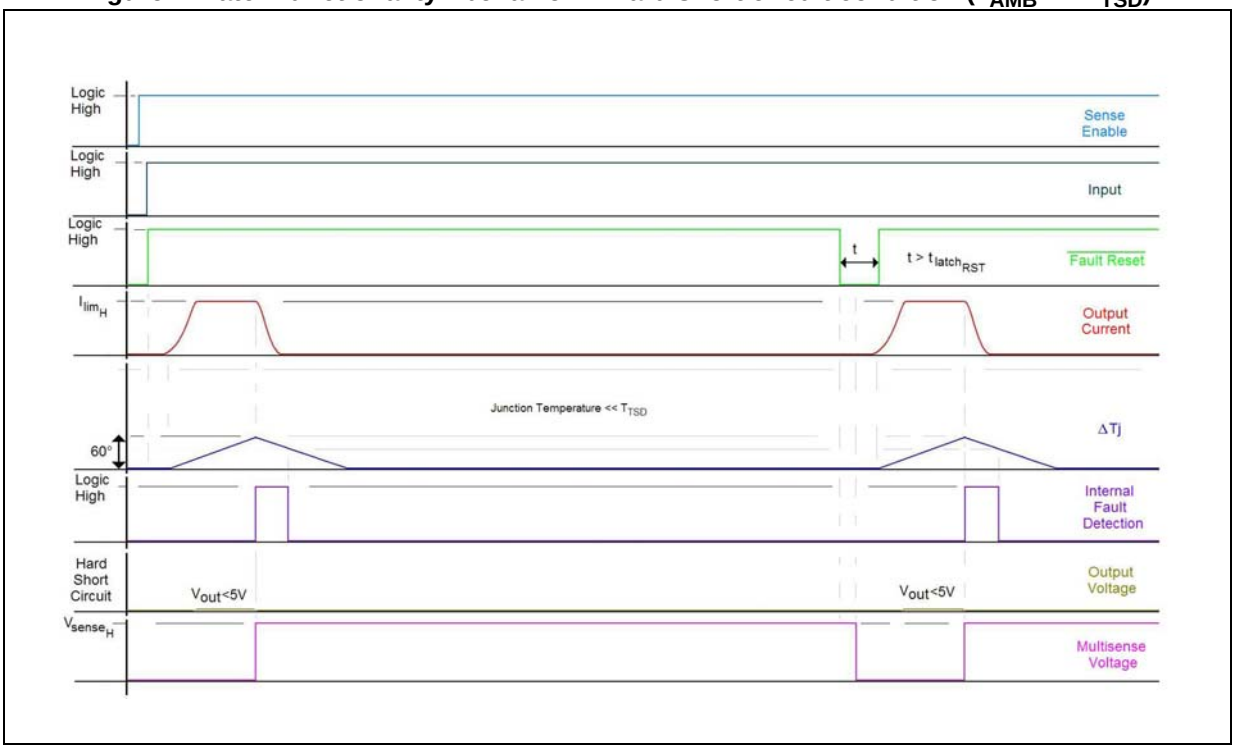


Figure 8. Latch functionality - behavior in hard short circuit condition

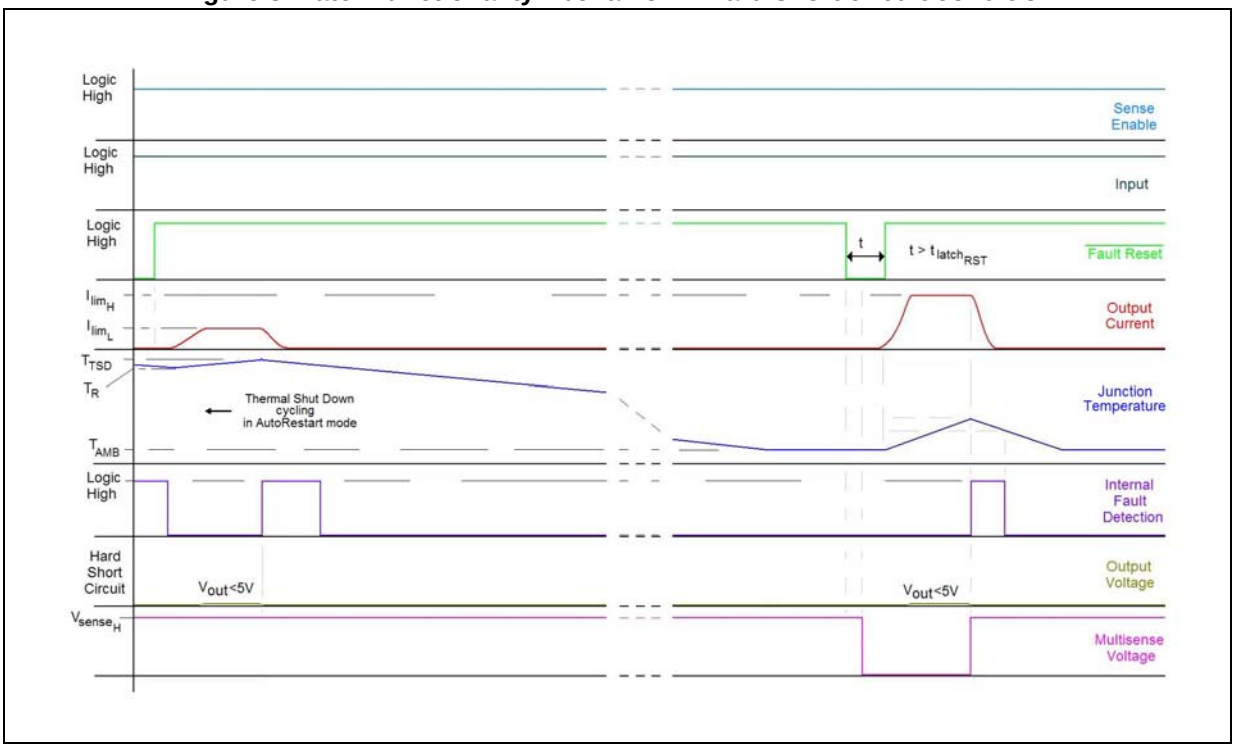


Figure 9. Latch functionality - behavior in hard short circuit condition (autorestart mode + latch off)

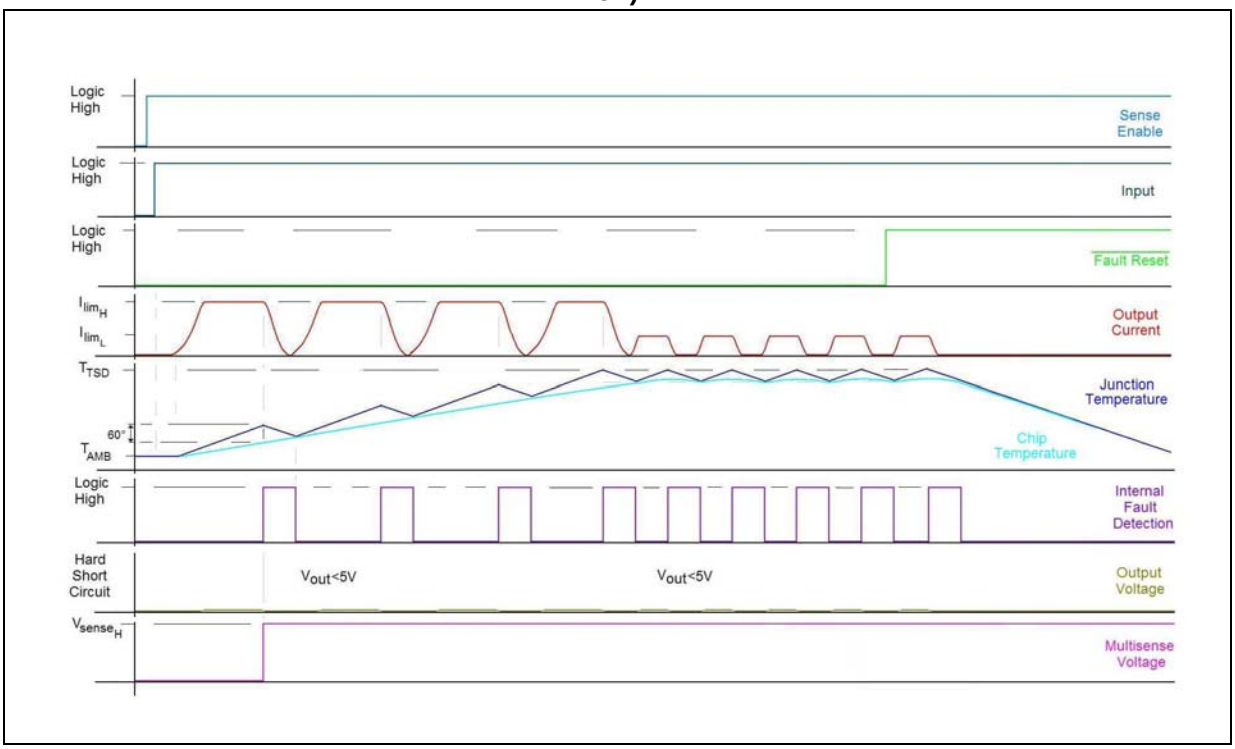


Figure 10. Standby mode activation

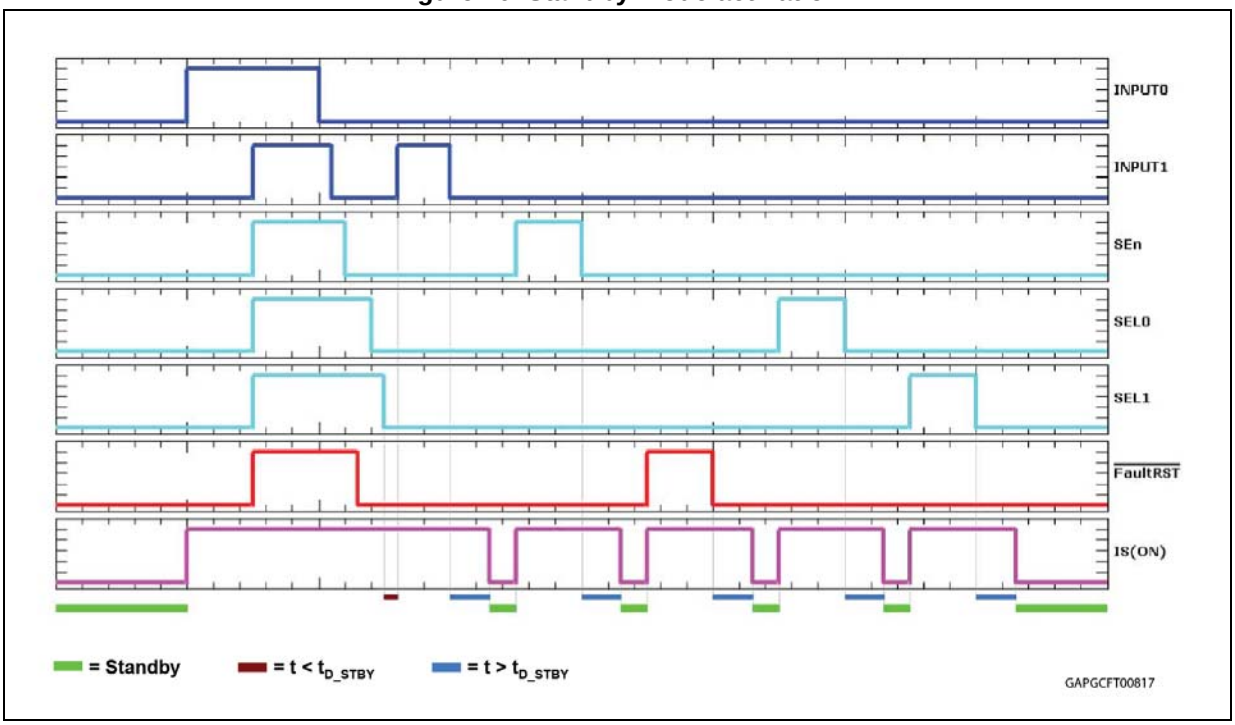
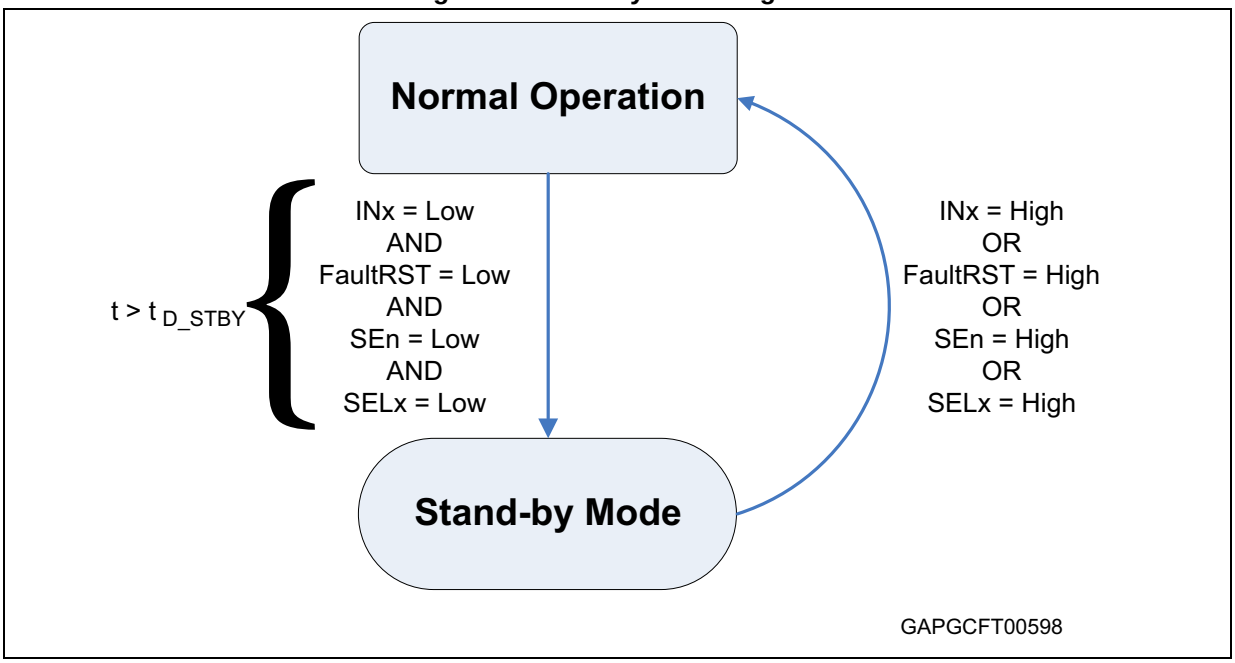
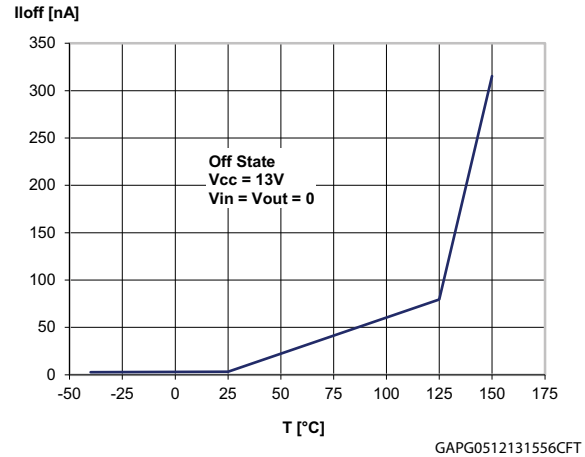


Figure 11. Standby state diagram



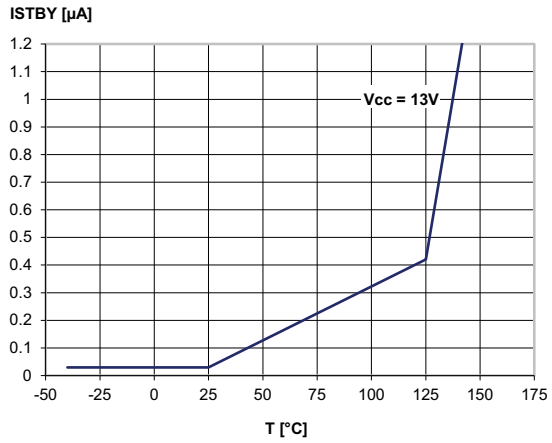
2.5 Electrical characteristics curves

Figure 12. OFF-state output current



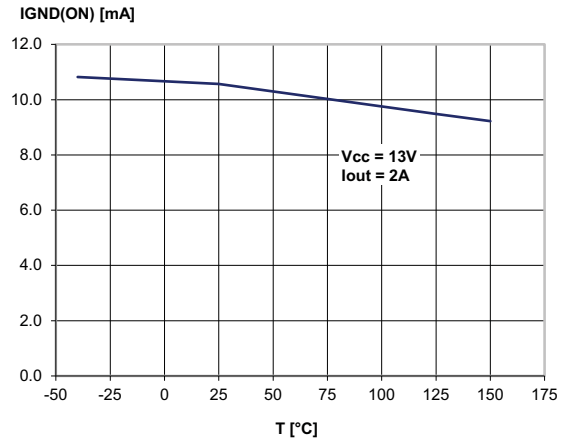
GAPG0512131556CFT

Figure 13. Standby current



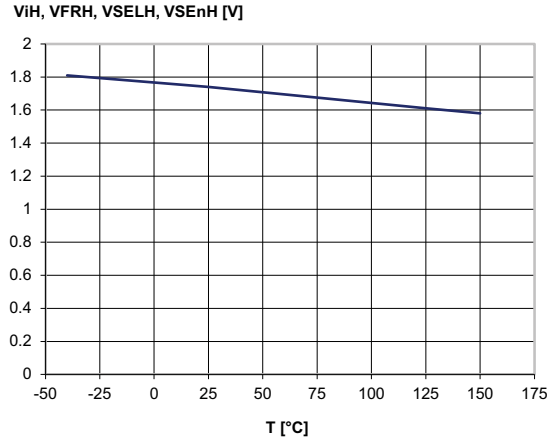
GAPG0512131558CFT

Figure 14. $I_{GND(ON)}$ vs I_{out}



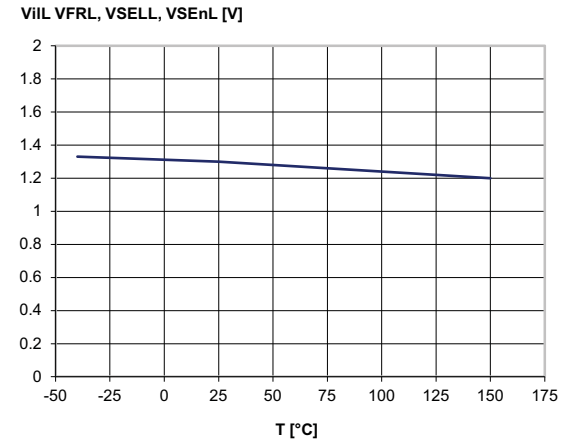
GAPG0512131559CFT

Figure 15. Logic Input high level voltage



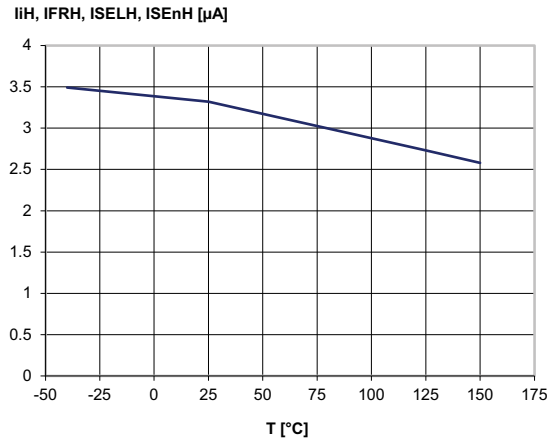
GAPG0512131602CFT

Figure 16. Logic Input low level voltage



GAPG0512131604CFT

Figure 17. High level logic input current



GAPG0512131606CFT

Figure 18. Low level logic input current

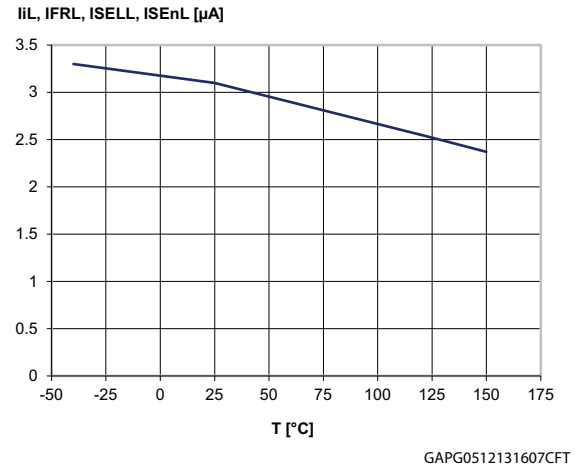


Figure 19. Logic Input hysteresis voltage

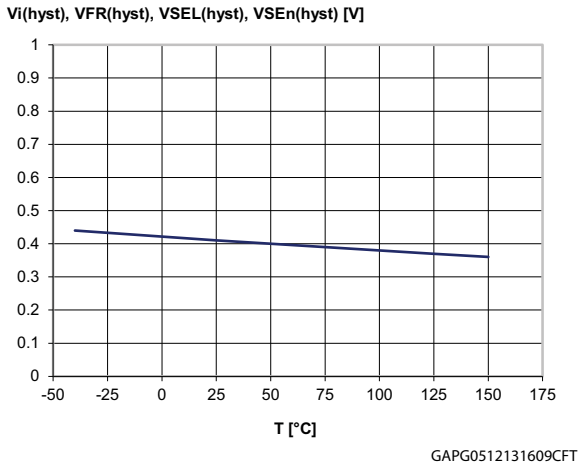


Figure 20. FaultRST Input clamp voltage

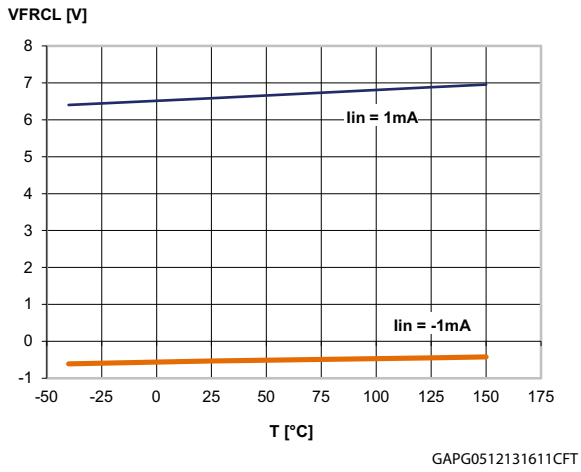


Figure 21. Undervoltage shutdown

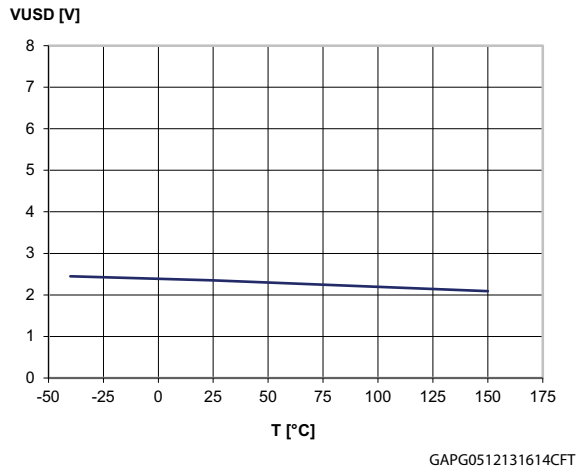


Figure 22. On-state resistance vs T_{case}

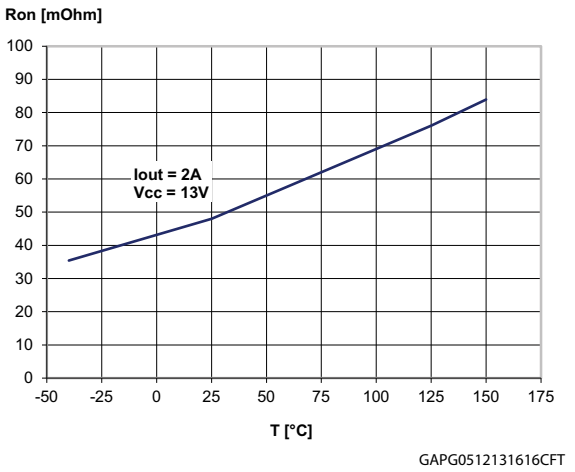


Figure 23. On-state resistance vs V_{CC}

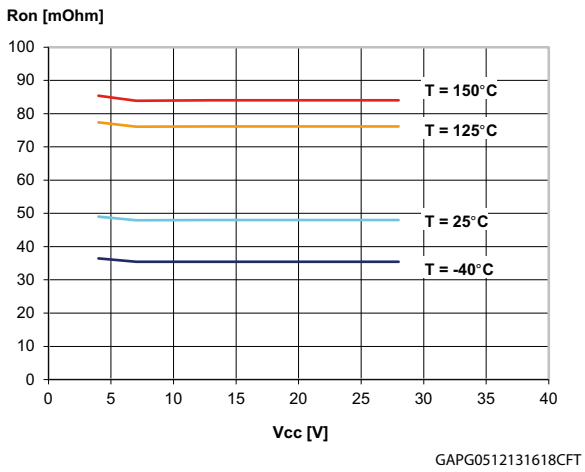


Figure 24. Turn-on voltage slope

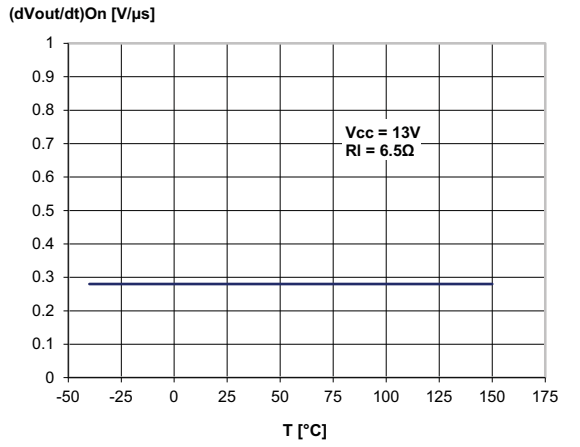


Figure 25. Turn-off voltage slope

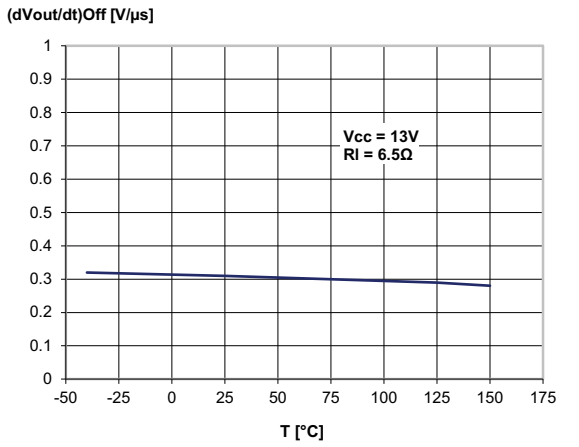


Figure 26. W_{on} vs T_{case}

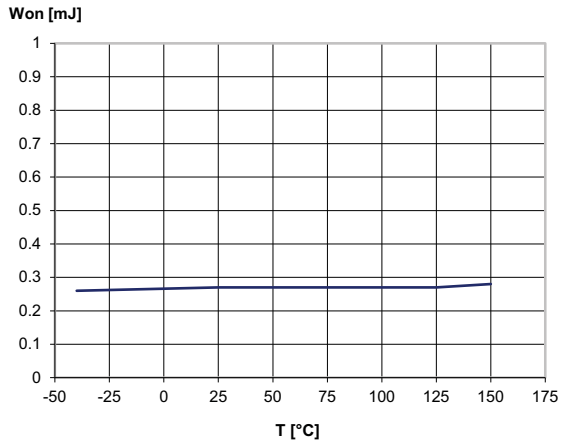


Figure 27. W_{off} vs T_{case}

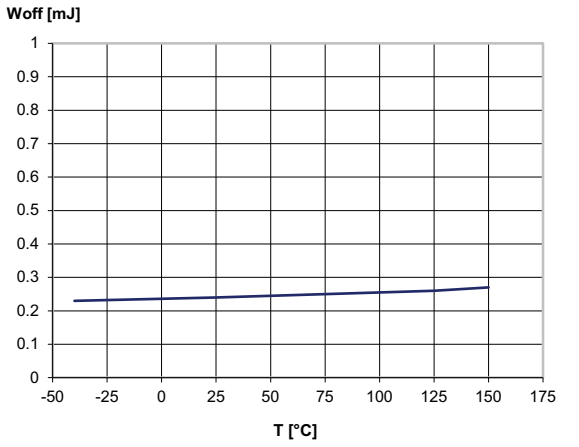


Figure 28. I_{LIMH} vs. T_{case}

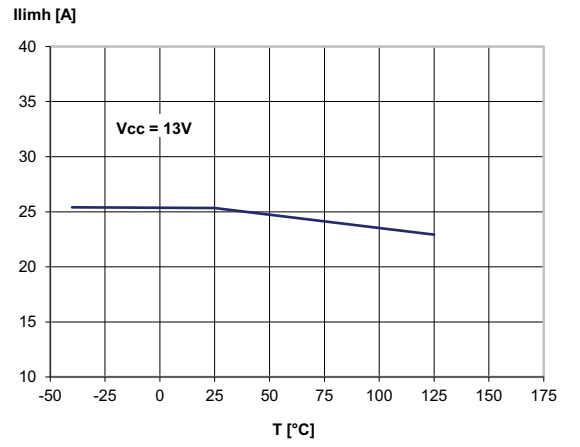


Figure 29. OFF-state open-load voltage detection threshold

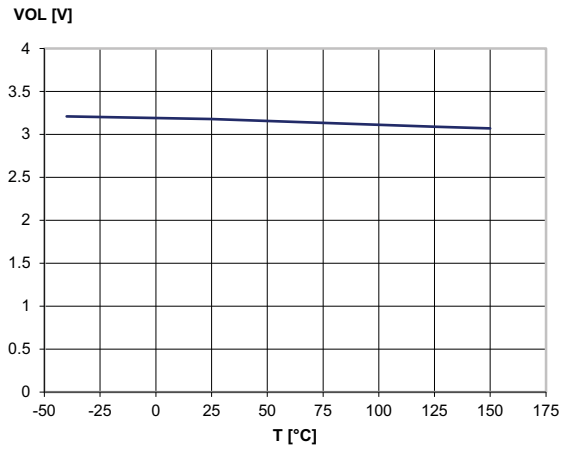


Figure 30. V_{sense} clamp vs. T_{case}

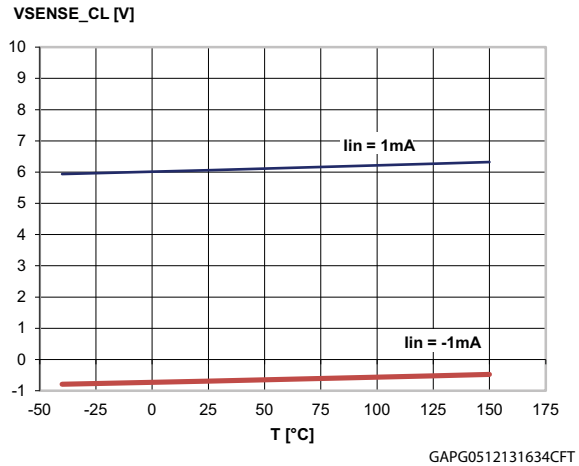
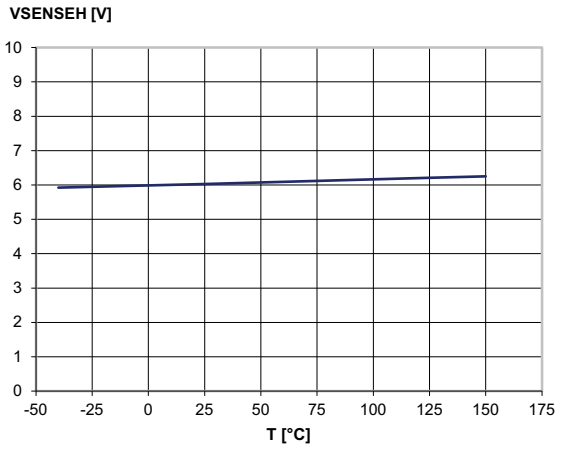


Figure 31. V_{senseh} vs. T_{case}



3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. According to the voltage level on the FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (FaultRST = Low) or remains off (FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (see *Table 8*, FaultRST = Low) or remains off (FaultRST = High).

3.3 Current limitation

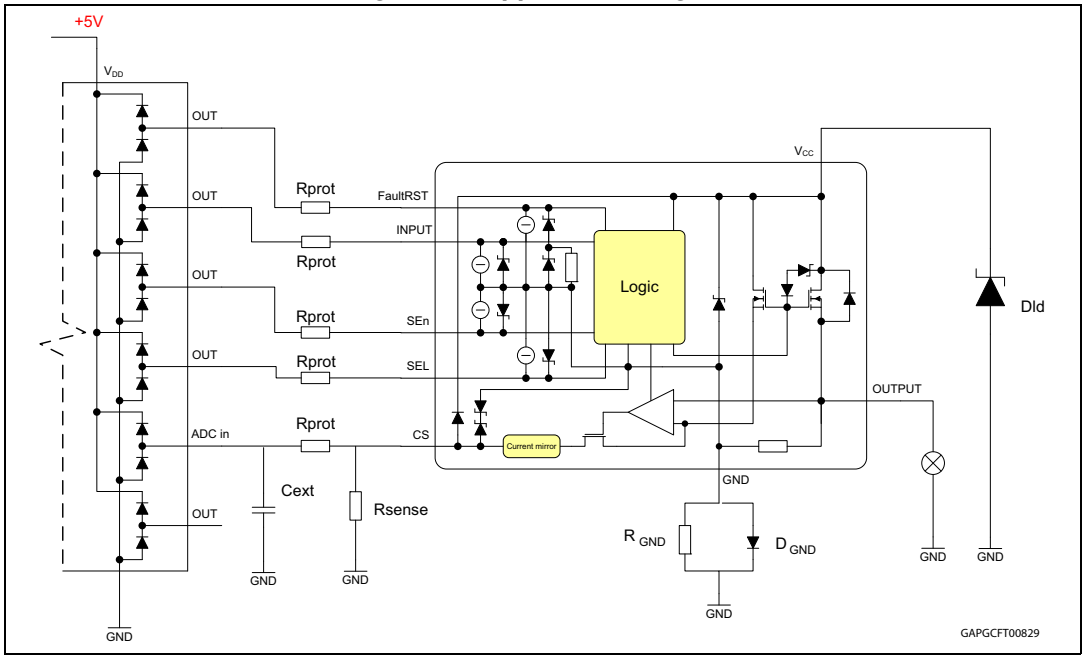
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG} (see *Table 8*), allowing the inductor energy to be dissipated without damaging the device.

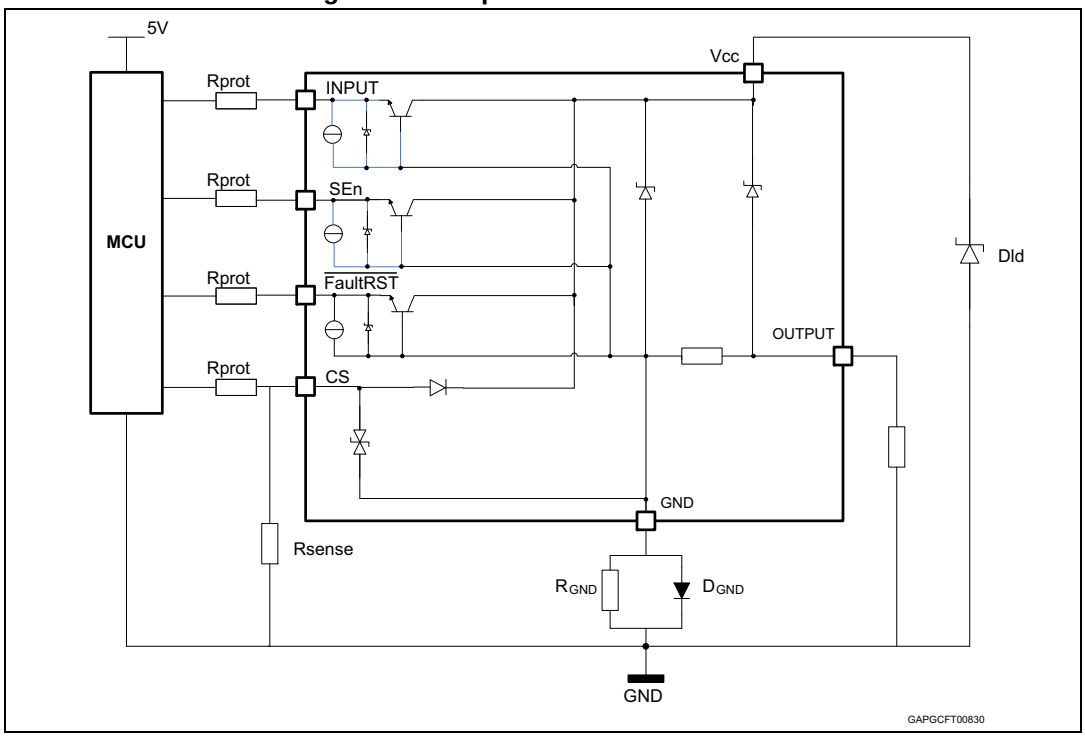
4 Application information

Figure 32. Application diagram



4.1 GND protection network against reverse battery

Figure 33. Simplified internal structure



4.1.1 Diode (D_{GND}) in the ground line

A resistor (typ. R_{GND} = 4.7 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 12*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through V_{CC} and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 12. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S(1)		min	max	
1	III	-112V	500 pulses	0,5 s		2ms, 10Ω
2a	III	+55V	500 pulses	0,2 s	5 s	50µs, 2Ω
3a	IV	-220V	1h	90 ms	100 ms	0.1µs, 50Ω
3b	IV	+150V	1h	90 ms	100 ms	0.1µs, 50Ω
4(2)	IV	-7V	1 pulse			100ms, 0.01Ω
Load dump according to ISO 16750-2:2010						
Test B(3)		40V	5 pulse	1 min		400ms, 2Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < T_j < 150°C).

4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins to latch-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak} = -150 V; $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

$$7.5\ k\Omega \leq R_{prot} \leq 140\ k\Omega.$$

Recommended values: R_{prot} = 15 kΩ

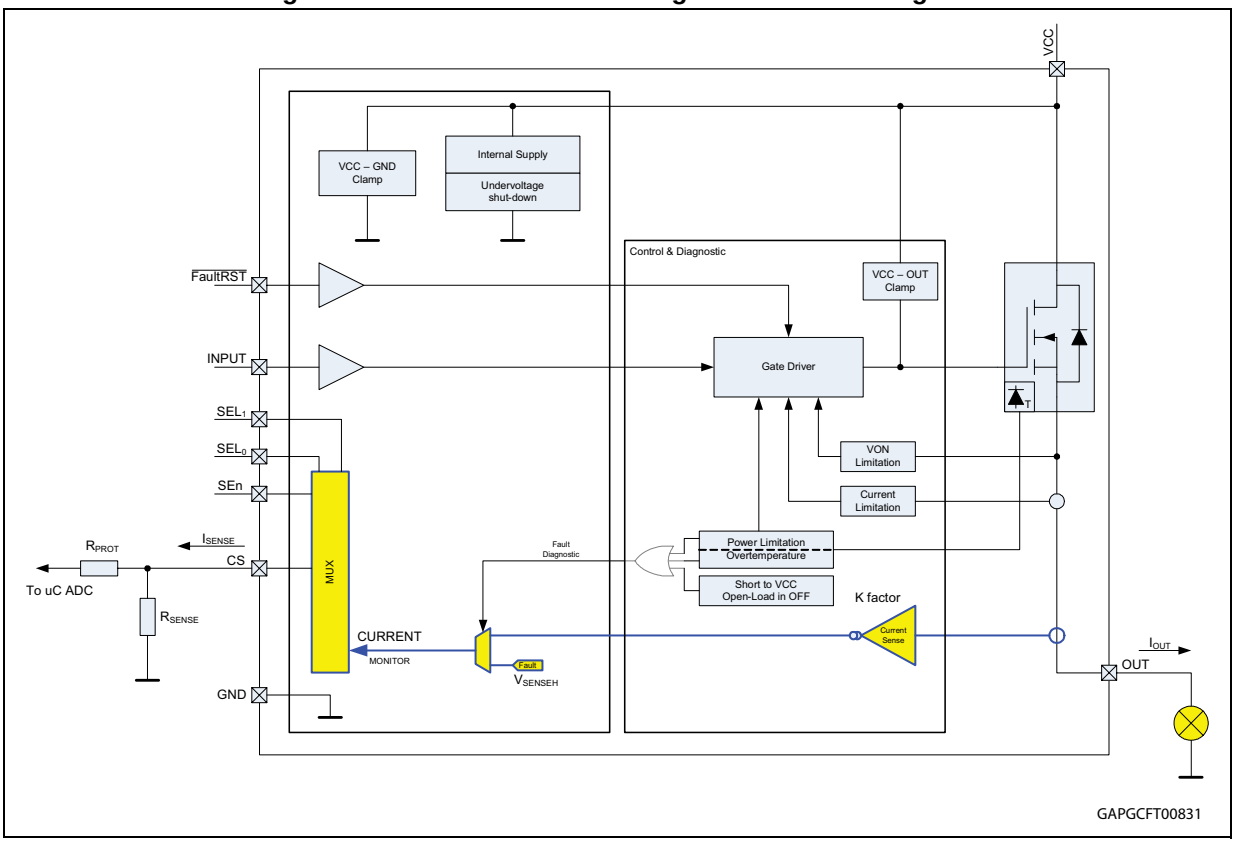
4.4 CS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

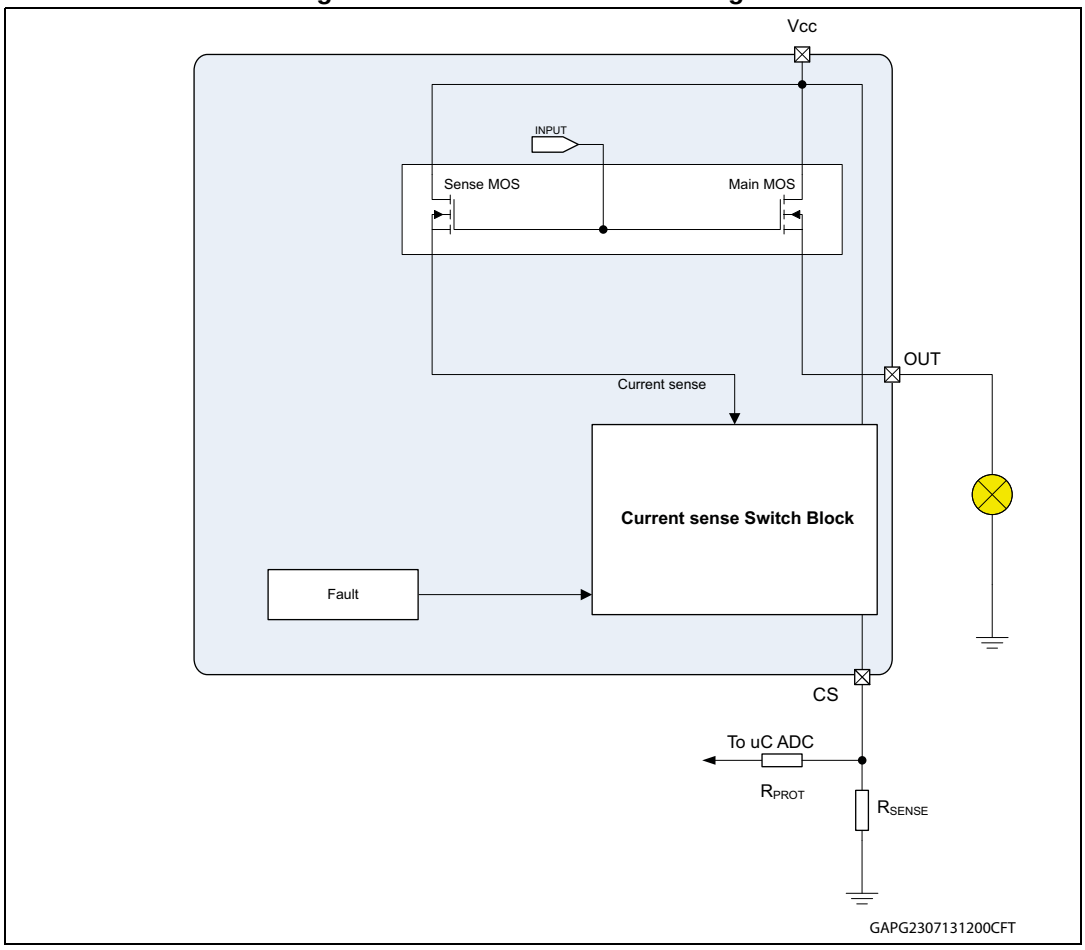
Those signals are routed through an analog multiplexer which is configured and controlled by means of SELx and SEn pins, according to the address map in *Table 11*.

Figure 34. Current sense and diagnostic – block diagram



4.4.1 Principle of Current sense signal generation

Figure 35. Current sense block diagram



Current sense

This output is capable to provide:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage V_{SENSEH}

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted to a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations

Current provided by CS output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

- V_{SENSE} is voltage measurable on R_{SENSE} resistor
- I_{SENSE} is current provided from CS pin in current output mode
- I_{OUT} is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of the overall circuitry the specifying ratio between I_{OUT} and I_{SENSE}.

Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CS pin which is switched to a “current limited” voltage source, V_{SENSEH} (see *Table 9*).

In any case, the current sourced by the CS in this condition is limited to I_{SENSEH} (see *Table 9*).

The typical behavior in case of overload or hard short circuit is shown in *Figure 7*, *Figure 8* and *Figure 9*.

Figure 36. Analogue HSD – open-load detection in off-state

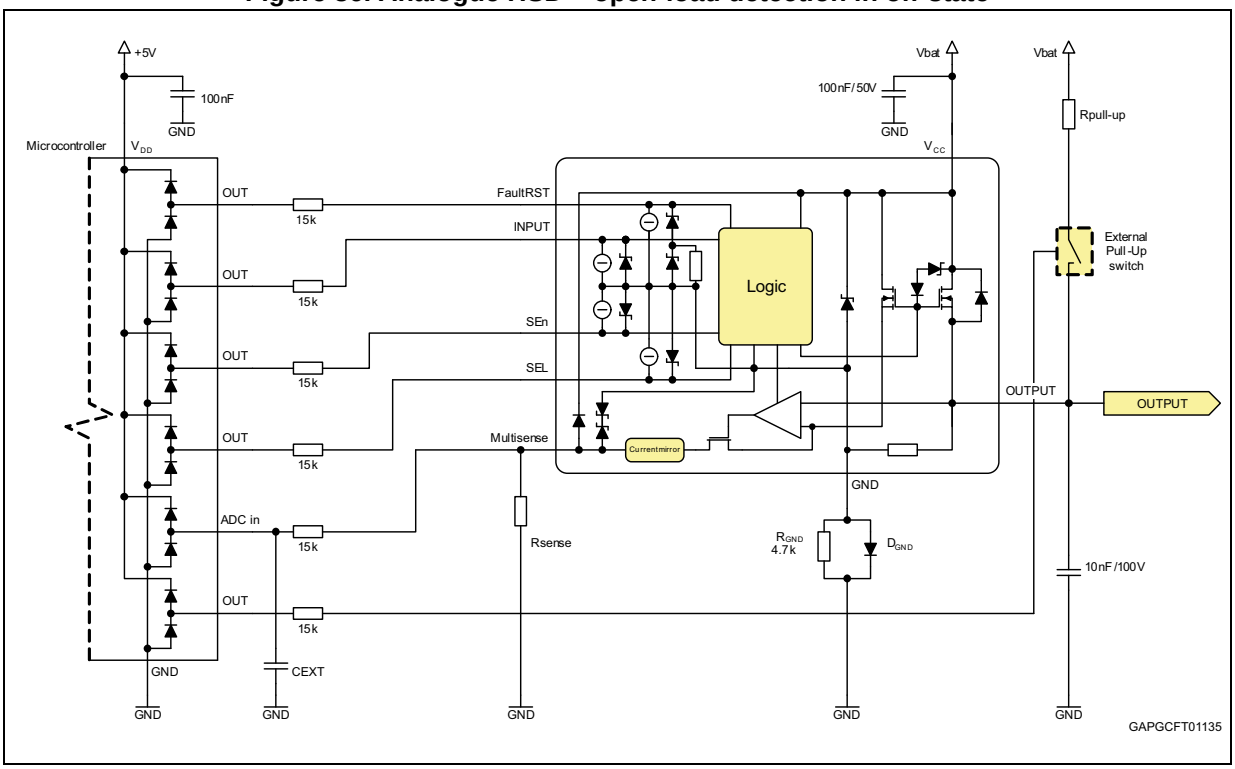


Figure 37. Open-load / short to V_{CC} condition

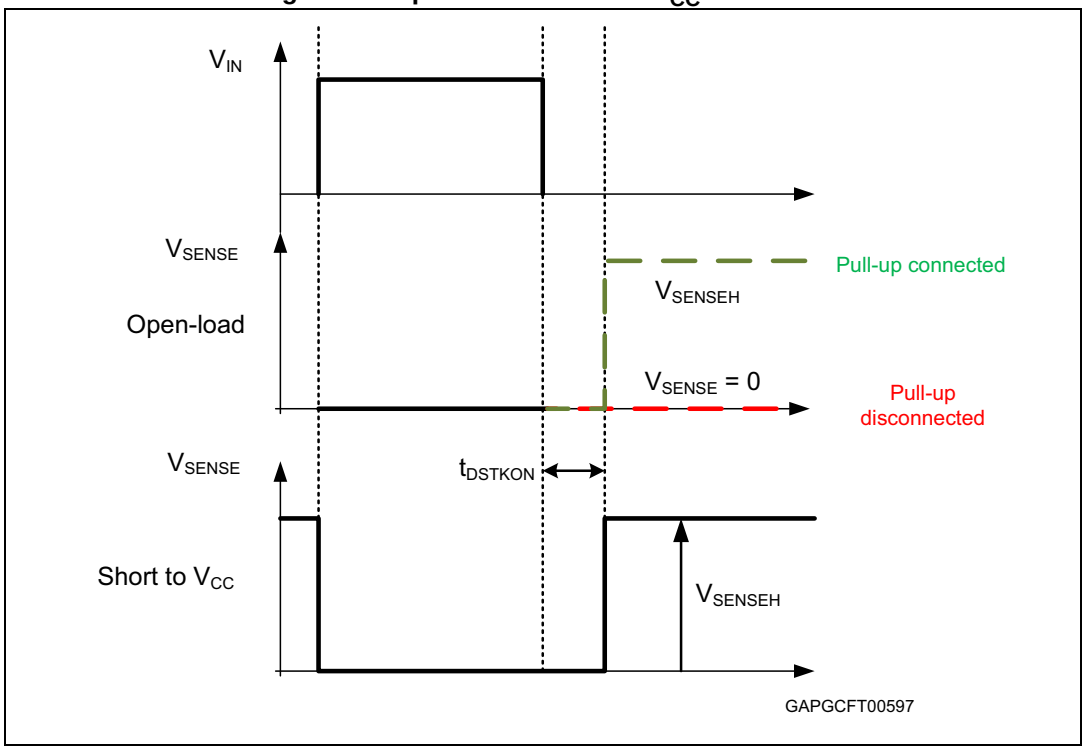


Table 13. Current Sense pin levels in off-state

Condition	Output	CS	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V_{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

4.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

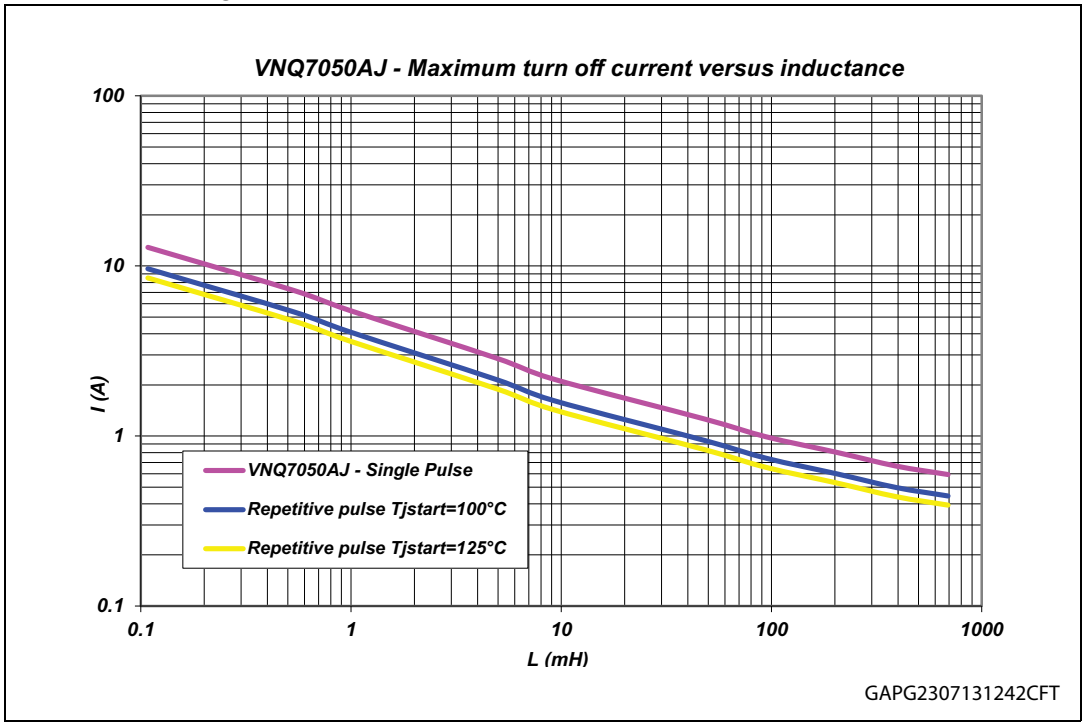
R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with to following equation:

Equation 2

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

4.5 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 38. Maximum turn off current versus inductance



Note: Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

5 Package and PCB thermal data

5.1 PowerSSO-16 thermal data

Figure 39. PowerSSO-16 on two-layers PCB (2s0p to JEDEC JESD 51-5)

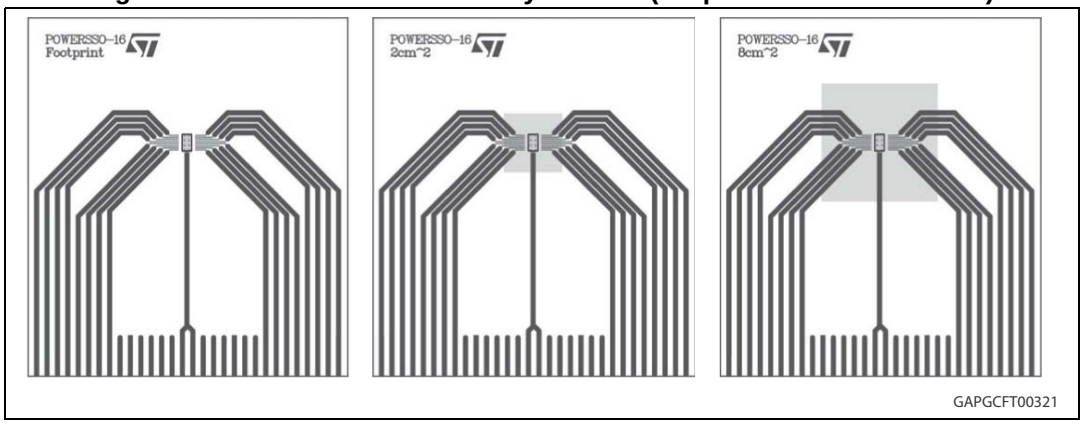


Figure 40. PowerSSO-16 on four-layers PCB (2s2p to JEDEC JESD 51-7)

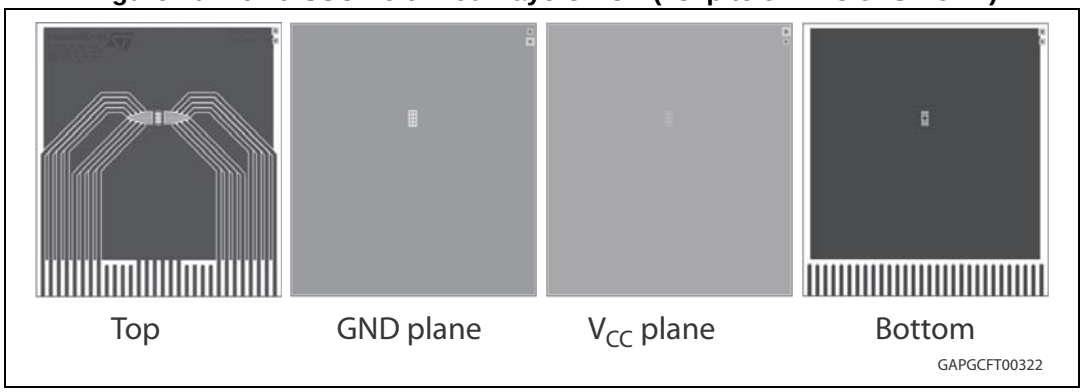


Table 14. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

Figure 41. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)

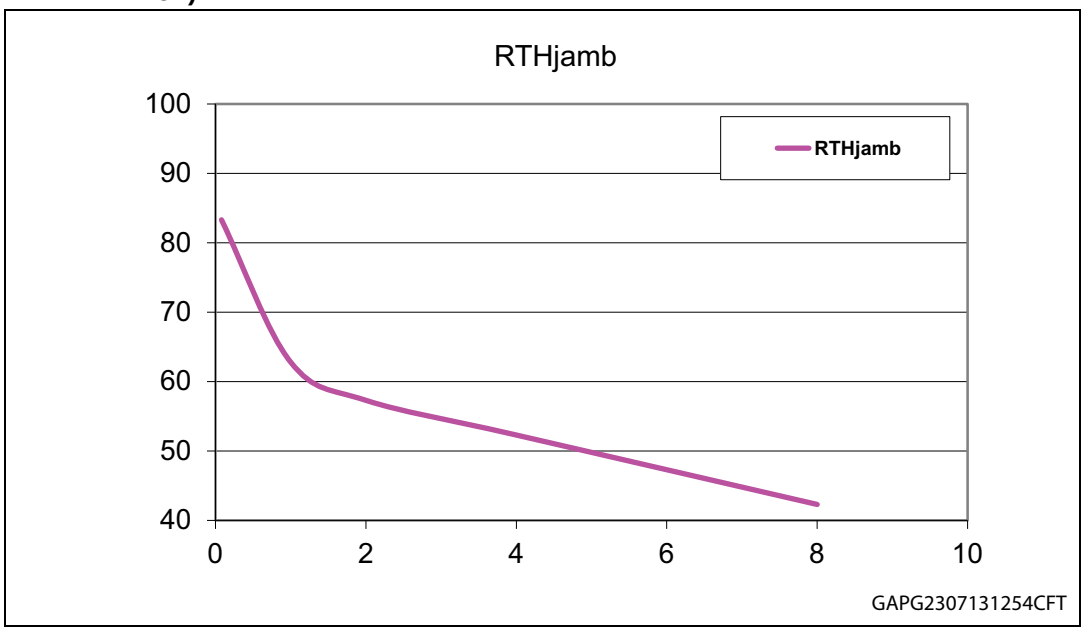
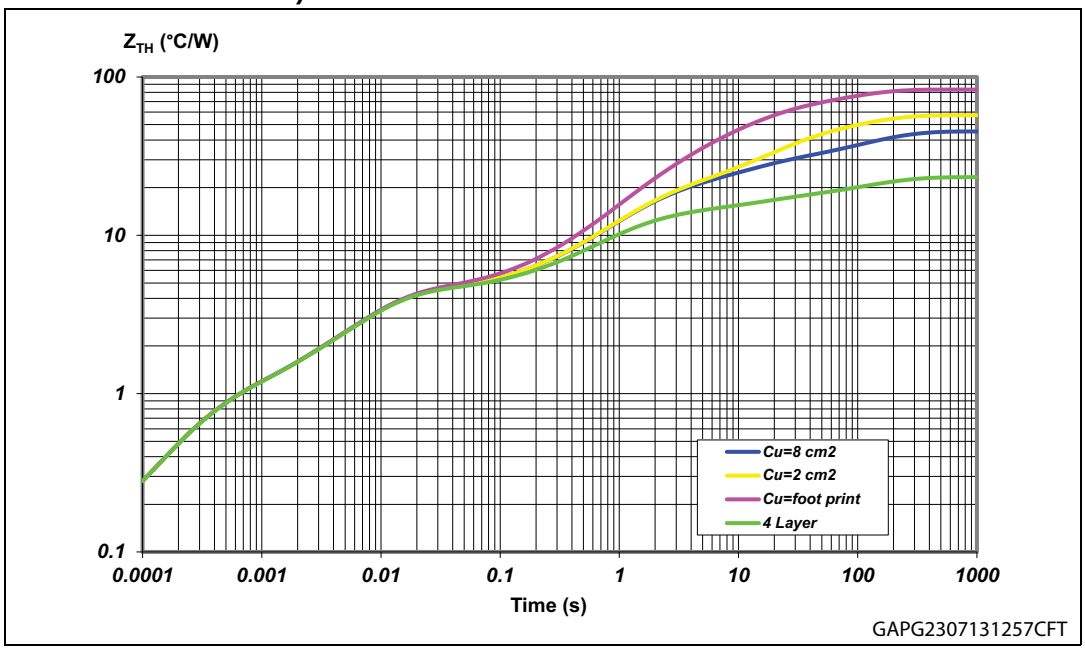


Figure 42. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)

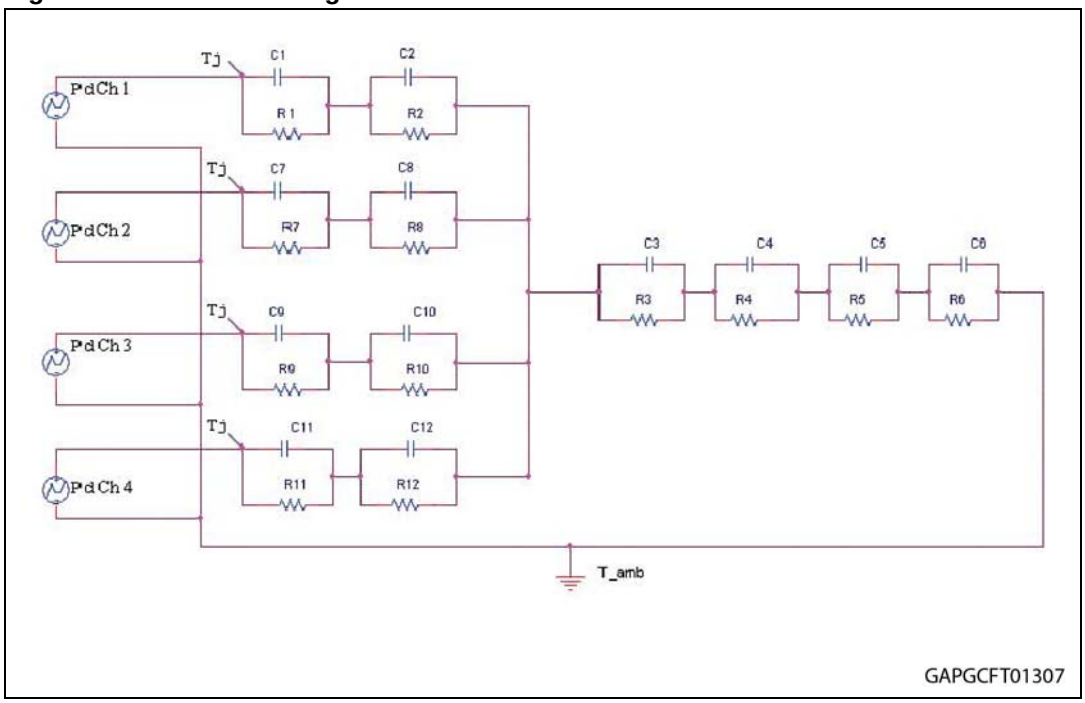


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

Figure 43. Thermal fitting model of a double-channel HSD in PowerSSO-16



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8	
R1 = R7 = R9 = R11 (°C/W)	0.8			
R2 = R8 = R10 = R12 (°C/W)	3.5			
R3 (°C/W)	7	7	7	7
R4 (°C/W)	16	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 = C7 = C9 = C11 (W.s/°C)	0.00035			
C2 = C8 = C10 = C12 (W.s/°C)	0.0023			
C3 (W.s/°C)	0.14			
C4 (W.s/°C)	0.2	0.3	0.3	0.4
C5 (W.s/°C)	0.4	1	1	4
C6 (W.s/°C)	3	5	7	18

6 Package information

6.1 ECOPACK®

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6.2 PowerSSO-16 package information

Figure 44. PowerSSO-16 package dimensions

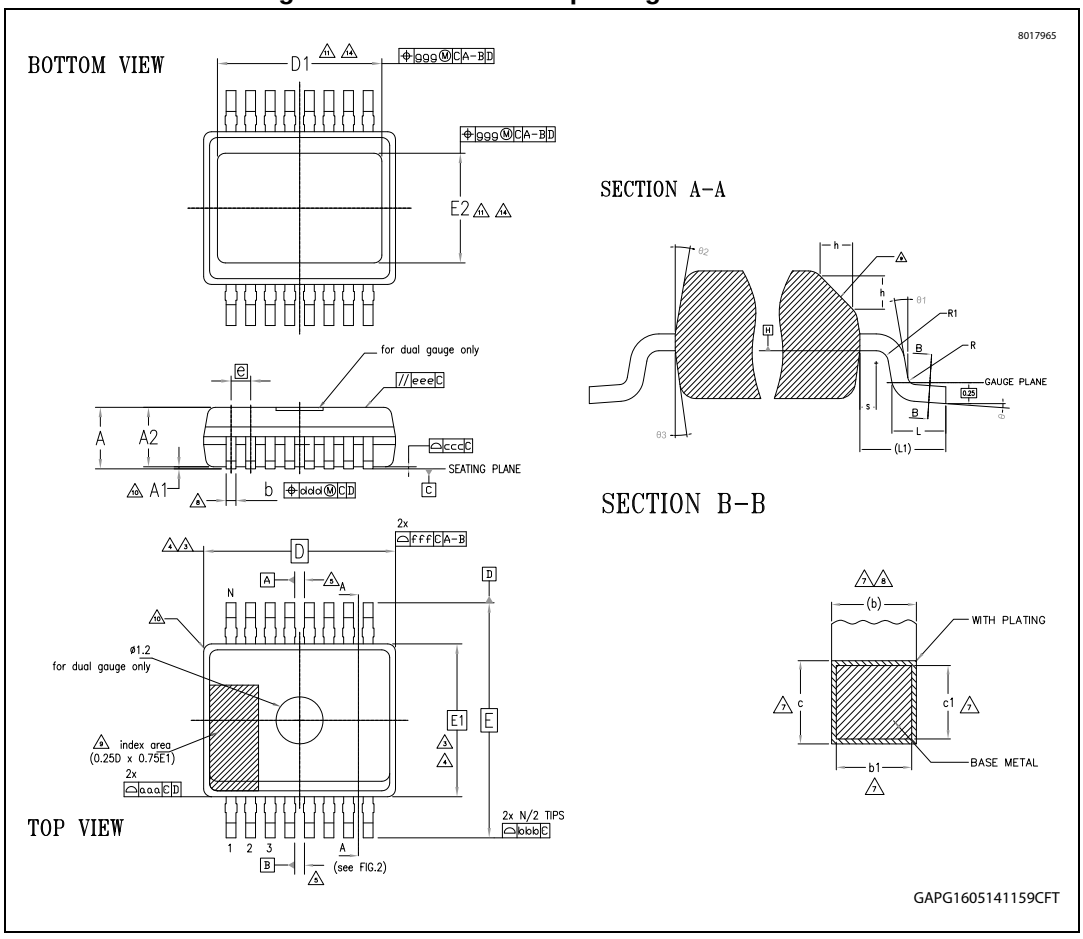

Table 16. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.90 BSC		
D1	3.60		4.20
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	1.90		2.50
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

7 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-16	VNQ7050AJ-E	VNQ7050AJTR-E

8 Revision history

Table 18. Document revision history

Date	Revision	Changes
03-Jun-2012	1	Initial release.
26-Jul-2012	2	Updated *Figure 2: Configuration diagram (top view)* *Table 3: Absolute maximum ratings*: – I_{SENSE}, E_{MAX}: updated parameters – V_{CC_ISC}: removed row – V_{ESD}: updated values Update *Table 4: Thermal data* *Table 5: Power section*: – V_{clamp}: added test conditions Update *Table 9: CurrentSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)* Updated *Figure 4: Switching times and Pulse skew* Removed *Figure : Pulse skew* Added *Figure 6: T_{DSKON}* Updated *Table 10: Truth table* *Table 11: Current sense multiplexer addressing*: added note Updated *Section 2.4: Waveforms* Added *Chapter 3: Protections* and *Chapter 4: Application information*
25-Jul-2013	3	Updated *Table 2: Suggested connections for unused and not connected pins* *Table 3: Absolute maximum ratings*: – V_{CCPK}: updated parameter – I_{SENSE}: updated value – E_{MAX}: updated parameter and value *Table 4: Thermal data*: – $R_{thj-amb}$: updated value *Table 5: Power section*: – $I_{GND(ON)}$: updated value Updated *Table 6: Switching (VCC = 13 V; -40°C < T_j < 150°C, unless otherwise specified)*, *Table 9: CurrentSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)* and *Table 11: Current sense multiplexer addressing* Removed *Table: Electrical transient requirements (part 1/3)*, *Table: Electrical transient requirements (part 2/3)* and *Table: Electrical transient requirements (part 3/3)* Updated *Section 3.1: Power limitation*, *Section 3.2: Thermal shutdown*, *Section 3.4: Negative voltage clamp* and *Section 4.1.1: Diode (DGND) in the ground line* Removed *Section: Load dump protection* Added *Section 4.2: Immunity against transient electrical disturbances*

Table 18. Document revision history (continued)

Date	Revision	Changes
25-Jul-2013	3 (continued)	Updated *Figure 35: Current sense block diagram* and *Figure 36: Analogue HSD – open-load detection in off-state* Updated *Table 13: Current Sense pin levels in off-state* Added *Section 4.5: Maximum demagnetization energy (V_{CC} = 16 V)* Updated *Chapter 5: Package and PCB thermal data* and *Chapter 6: Package information*
18-Sep-2013	4	Updated disclaimer.
09-Dec-2013	5	Updated *Features* list *Table 4: Thermal data*: – $R_{thj\text{-}board}$: updated value *Table 6: Switching (VCC = 13 V; -40°C < T_j < 150°C, unless otherwise specified)*: – $(dV_{OUT}/dt)_{on}$, $(dV_{OUT}/dt)_{off}$: updated values *Table 9: CurrentSense (7 V < V_{CC} < 18 V; -40°C < T_j < 150°C)*: – K_{OL}, K_{LED}, K_0, K_1, K_2, K_3: updated values – dK_{cal}/K_{cal}: add row Added *Section 2.5: Electrical characteristics curves*
09-Jun-2014	6	Updated *Section 6.2: PowerSSO-16 package information*
22-Oct-2014	7	Updated *Figure 16: PowerSSO-16 mechanical data*

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