

## N-channel 60 V, 21 mΩ typ., 7 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

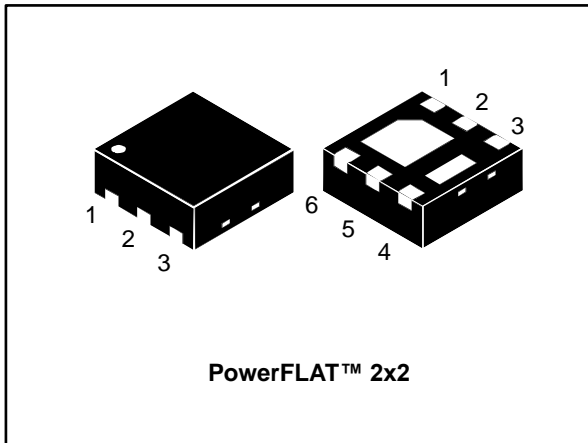


Figure 1: Internal schematic diagram

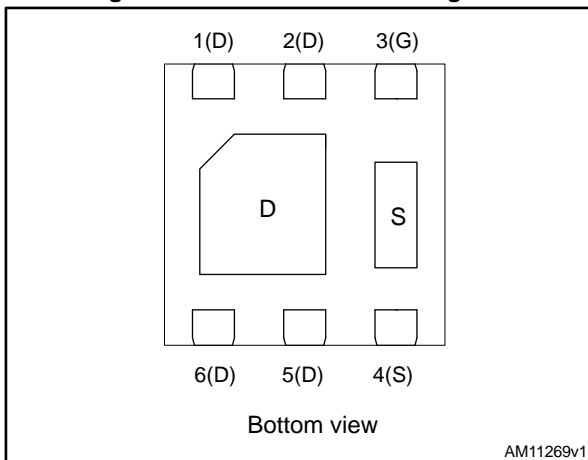


Table 1: Device summary

Order code	Marking	Package	Packing
STL7N6F7	ST7N	PowerFLAT™ 2x2	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL7N6F7	60 V	25 mΩ	7 A

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

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## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
	4.1 PowerFLAT 2x2 package information .....	10
<b>5</b>	<b>Revision history .....</b>	<b>12</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	7	A
$I_D$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	4.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.4	W
$T_J$	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	52	$^\circ\text{C/W}$

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

**Table 4: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	60			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V			1	μA
I <sub>GSS</sub>	Gate-body leakage current	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5A		21	25	mΩ

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 30 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	420	-	pF
C <sub>oss</sub>	Output capacitance		-	215	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	16	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 7 A	-	8	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 0 to 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	2.3	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	2.1	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 3.5A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	7.85	-	ns
t <sub>r</sub>	Rise time		-	3.25	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	12.1	-	ns
t <sub>f</sub>	Fall time		-	3.95	-	ns

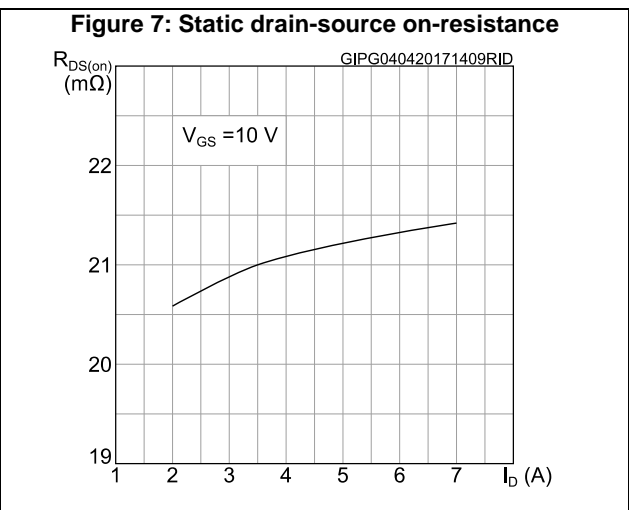
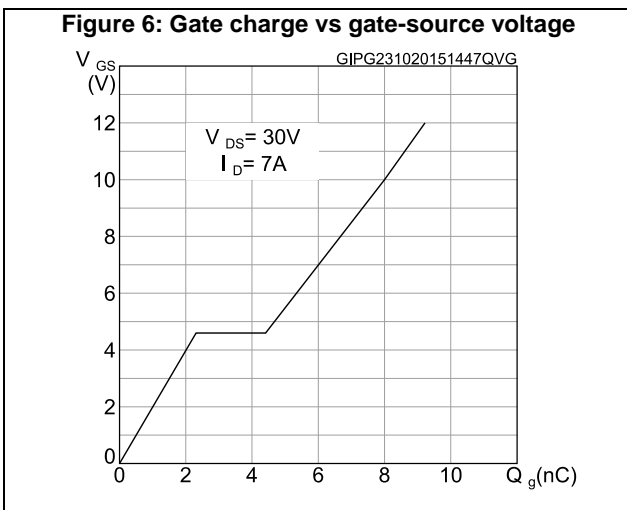
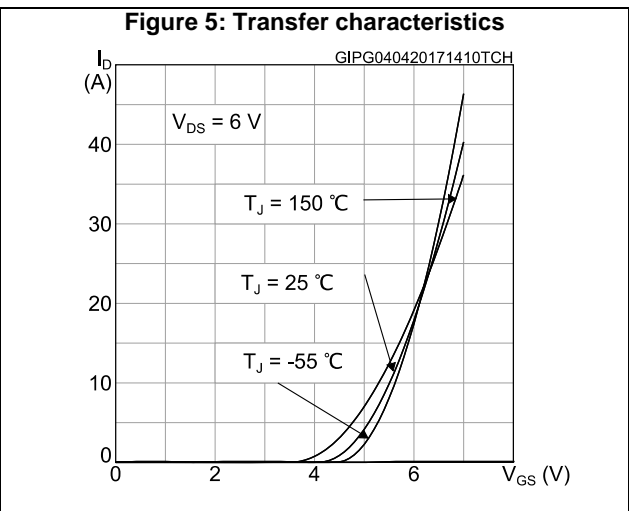
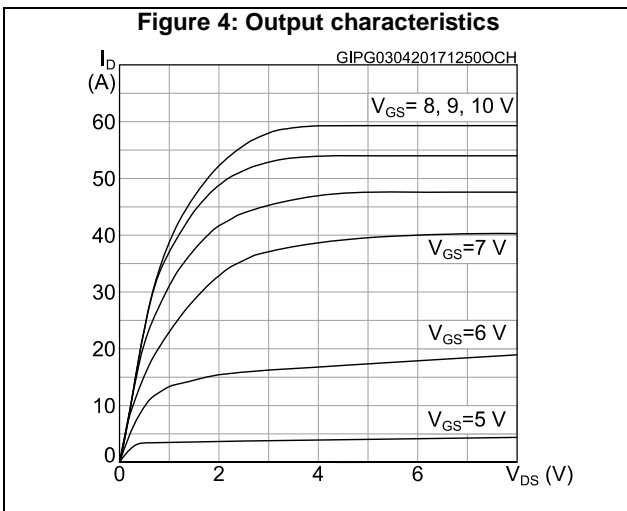
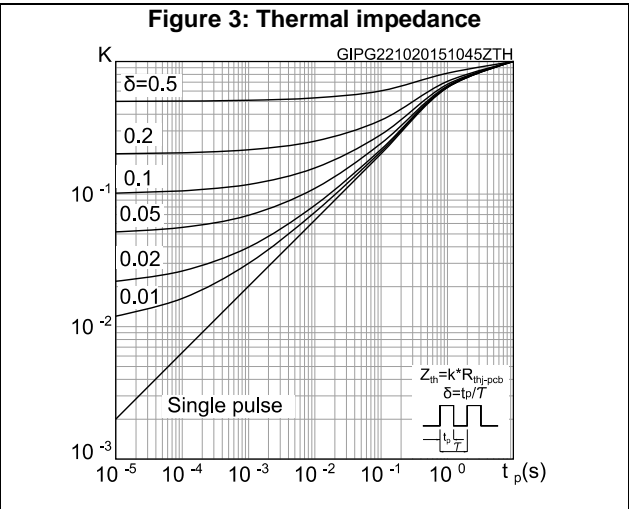
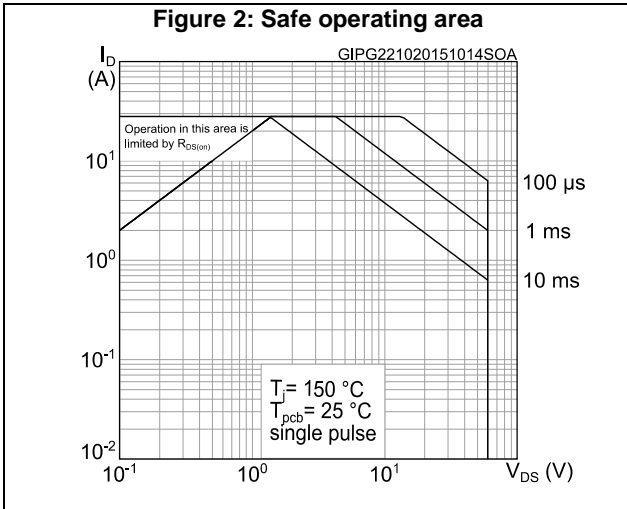
Table 7: Source-drain diode

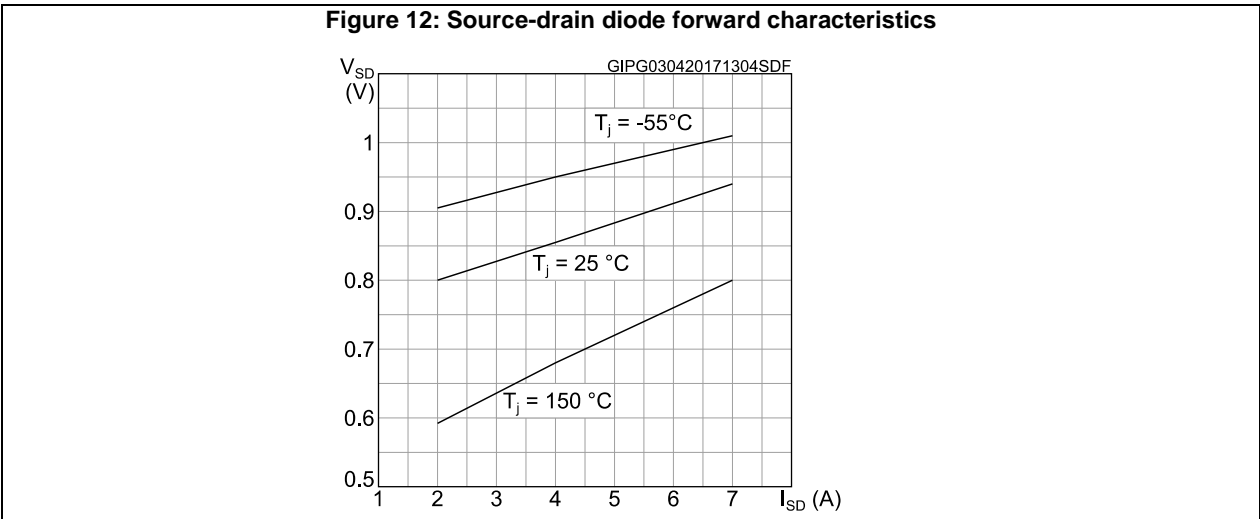
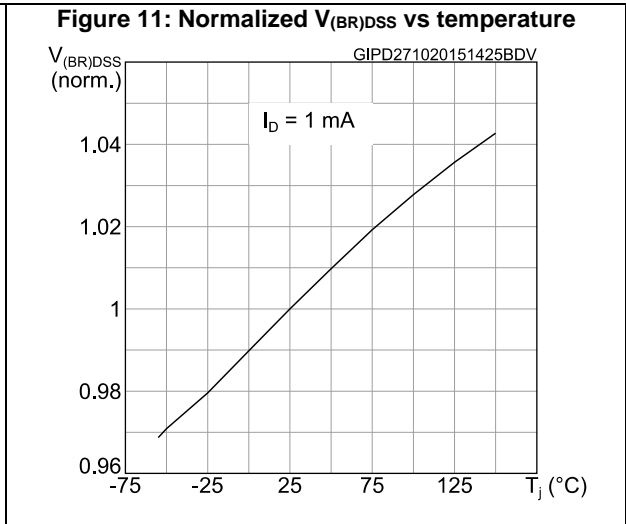
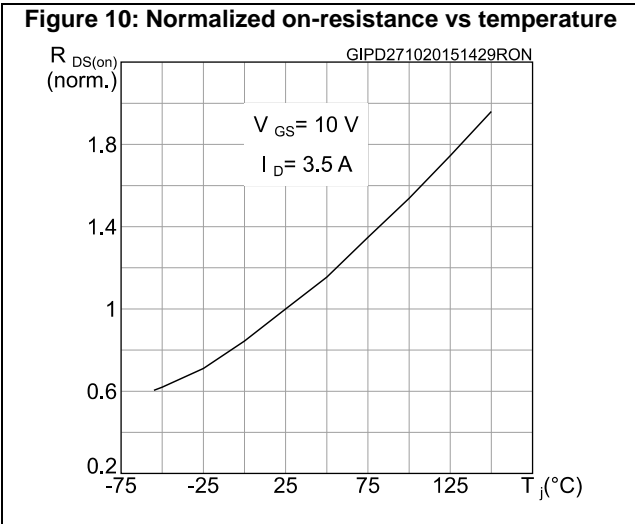
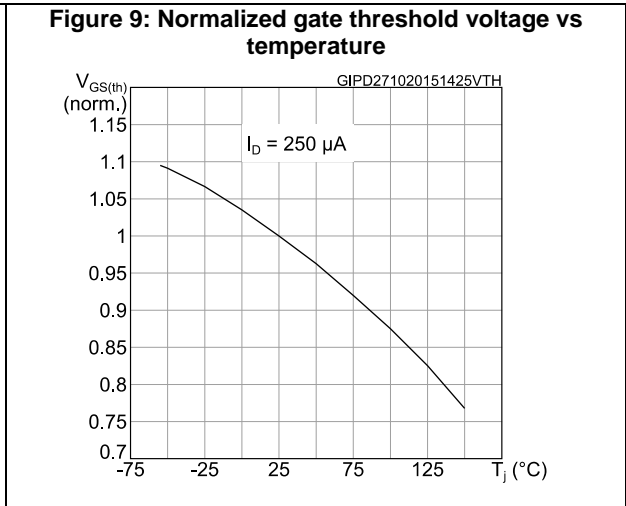
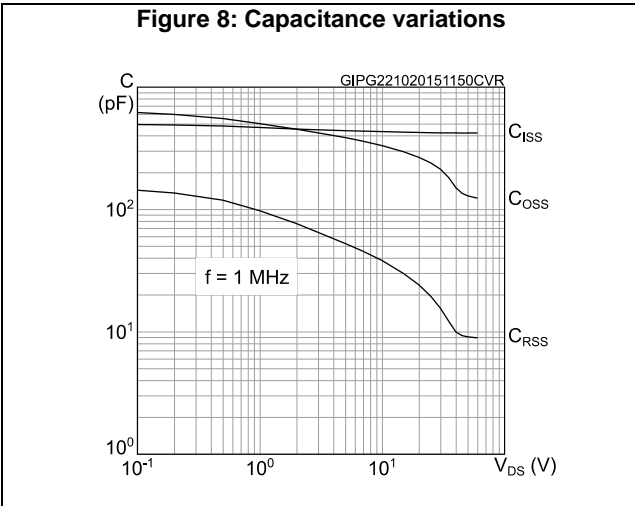
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_D = 7 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 48 \text{ V}$ (see <a href="#">Figure 15</a> : "Test circuit for inductive load switching and diode recovery times")	-	17.1		ns
$Q_{rr}$	Reverse recovery charge		-	6.67		nC
$I_{RRM}$	Reverse recovery current		-	0.8		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)





### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



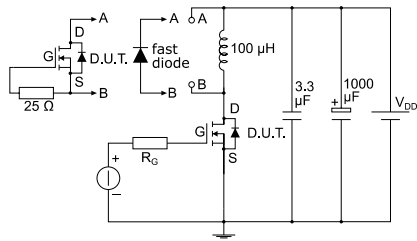
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**Figure 14: Test circuit for gate charge behavior**



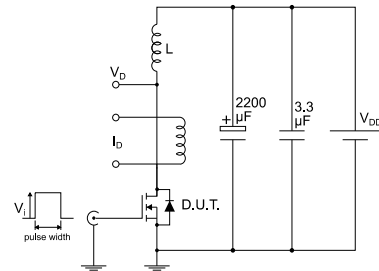
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



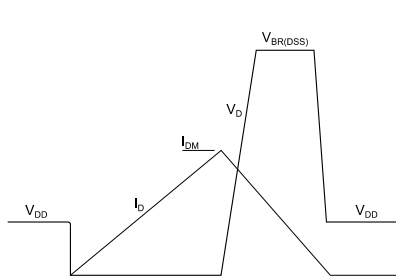
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**Figure 16: Unclamped inductive load test circuit**



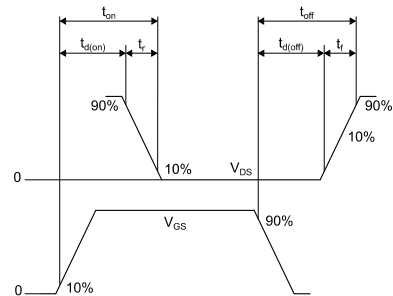
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT 2x2 package information

Figure 19: PowerFLAT™ 2x2 package outline

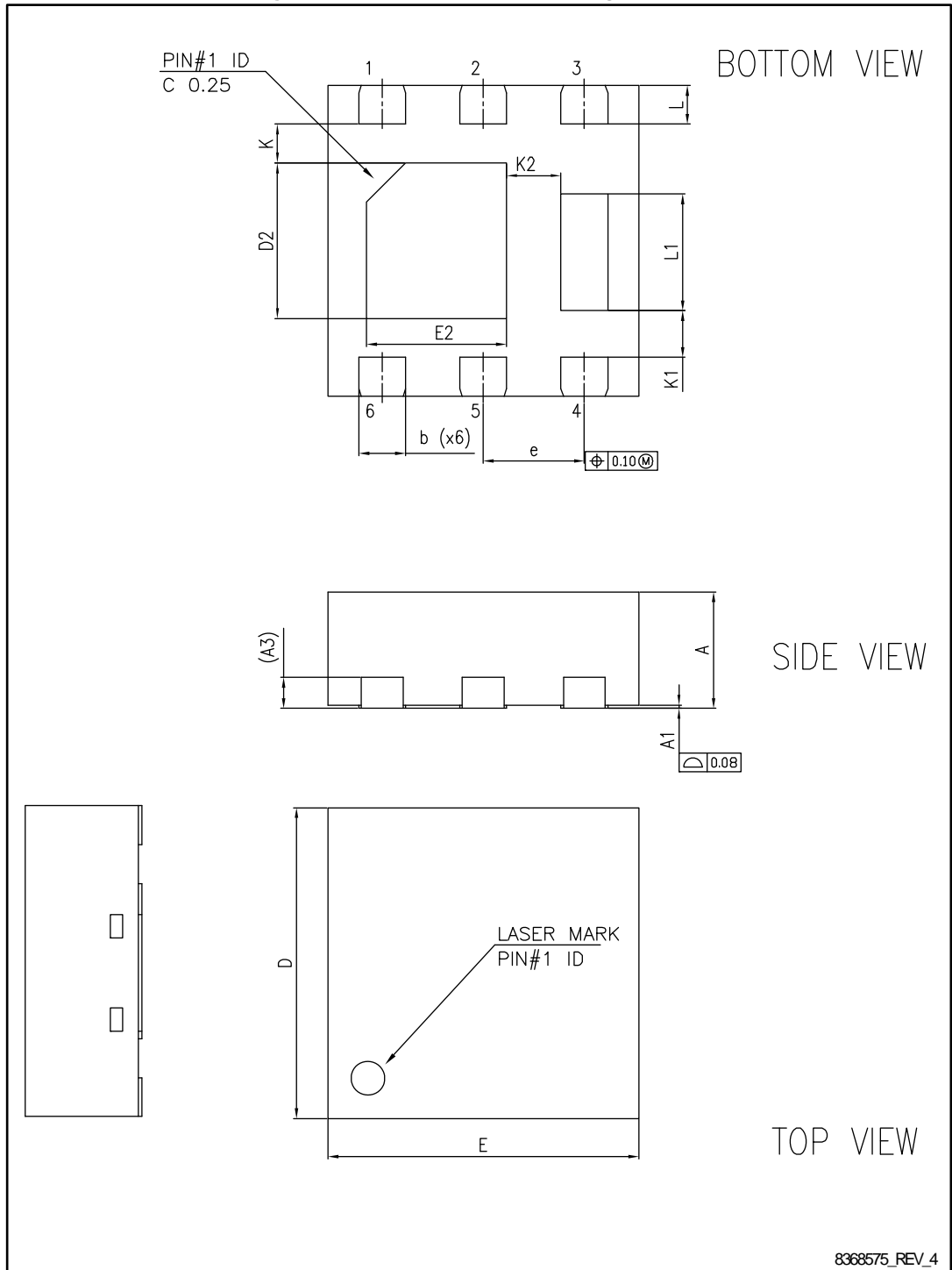
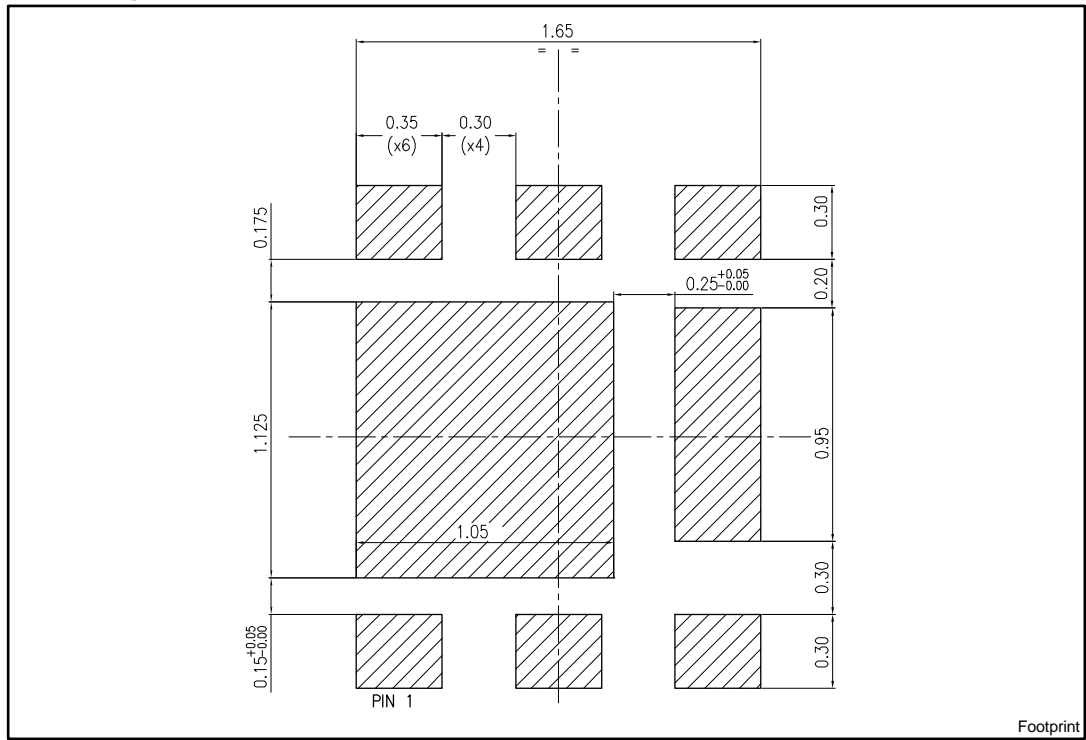


Table 8: PowerFLAT™ 2x2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 20: PowerFLAT™ 2x2 recommended footprint (dimensions are in mm)



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
27-Aug-2015	1	First release.
22-Oct-2015	2	Updated title and features in cover page Updated Table 4: "On /off states", Table 5: "Dynamic" and Table 6: "Switching times". Added Section 4.1: "Electrical characteristics (curves)"
03-Apr-2017	3	Modified title and features table on cover page Modified <i>Table 4: "On /off states"</i> Modified <i>Figure 4: "Output characteristics"</i> , <i>Figure 5: "Transfer characteristics"</i> , <i>Figure 7: "Static drain-source on-resistance"</i> and <i>Figure 12: "Source-drain diode forward characteristics"</i> Minor text changes.

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