AOZ8905

Ultra-Low Capacitance TVS Diode Array

General Description

The AOZ8905 is a transient voltage suppressor array designed to protect high speed data lines such as HDMI, USB 2.0, MDDI, SATA, and Gigabit Ethernet from damaging ESD events.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The AOZ8905 provides a typical line to line capacitance of 0.35pF and low insertion loss up to 3GHz providing greater signal integrity making it ideally suited for HDMI 1.3 or USB 2.0 applications, such as Digital TVs, DVD players, Computing, set-top boxes and MDDI applications in mobile computing devices.

The AOZ8905 comes in RoHS compliant and halogen free SOT23-6L package and is rated -40°C to +85°C junction temperature range.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - ±15kV (air discharge) and ±8kV (contact discharge)
  - IEC61000-4-4 (EFT) 40A (5/50nS)
  - IEC61000-4-5 (Lightning) 2.5A (8/20µS)
  - Human Body Model (HBM) ±15kV
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance between I/O lines: 0.35pF
- Low clamping voltage
- Low operating voltage: 5.0V

Applications

- HDMI, USB 2.0, MDDI, SATA ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers

Green Product

Typical Application

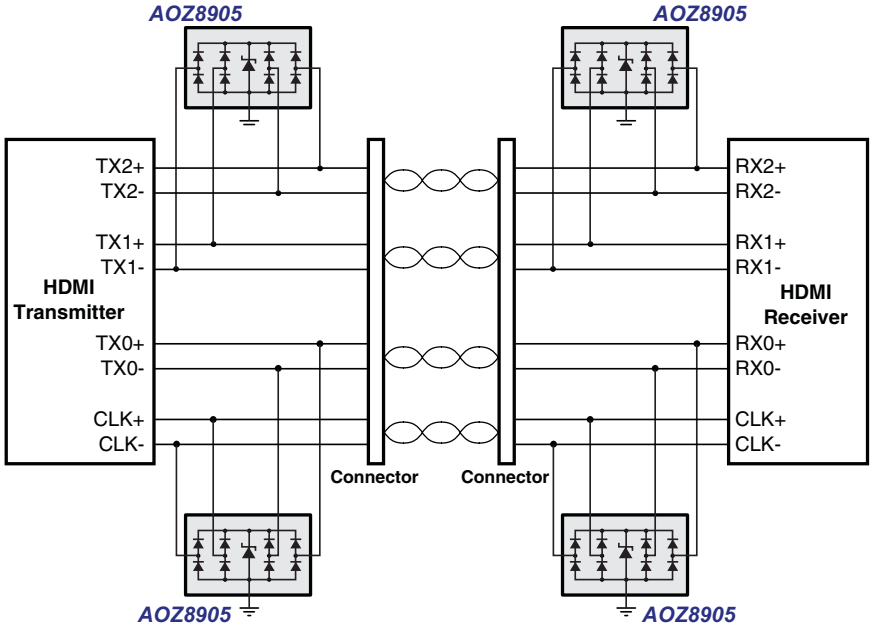


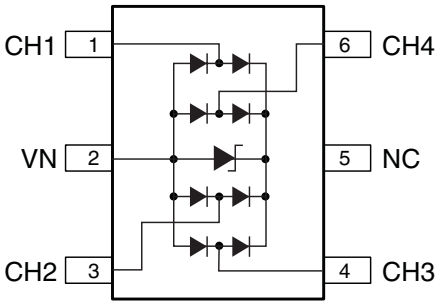
Figure 1. HDMI Ports

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8905CI	-40°C to +85°C	SOT23-6L	RoHS Compliant Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



SOT23-6
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, contact(1)	±8kV
ESD Rating per IEC61000-4-2, air(1)	±15kV
ESD Rating per Human Body Model(2)	±15kV

Notes:
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

T_A = 25°C unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

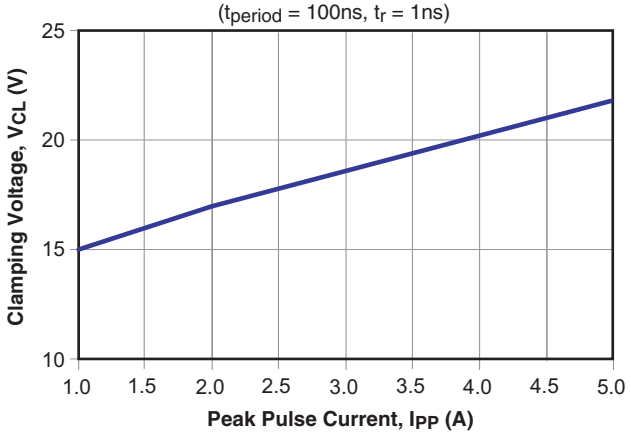
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between I/O and VN[3]			5.0	V
V_{BR}	Reverse Breakdown Voltage	I_T = 1mA, between I/O and VN[4]	6.0			V
I_R	Reverse Leakage Current	V_{RWM} = 5V, between I/O and VN			1	µA
V_F	Diode Forward Voltage	I_F = 15mA	0.70	0.85	1	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 1A, tp = 100ns, any I/O pin to Ground[5]			 15.0 -3.5	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5A, tp = 100ns, any I/O pin to Ground[5]			 22.0 -6.0	 V V
	Channel Clamp Voltage Any I/O Pin to Ground	I_{PP} = 1A, tp = 8/20µs			 15.5	 V
C_j	Channel Input Capacitance	V_R = 0V, f = 1MHz, between I/O pins		0.35	0.40	pF
		V_R = 0V, f = 1MHz, any I/O pin to Ground		0.70	0.80	pF

Notes:

3. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at the pulse test current I_T.
5. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

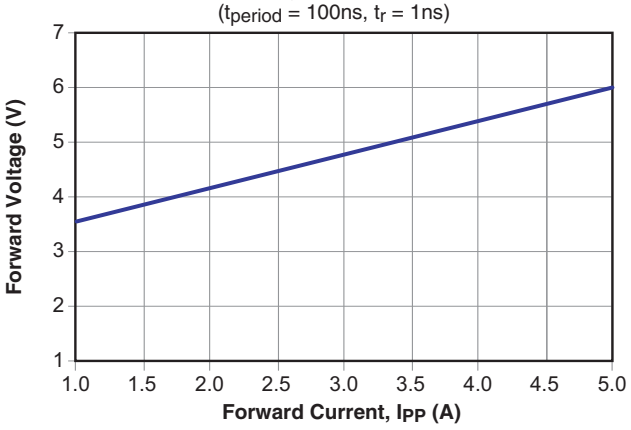
Typical Performance Characteristics

Clamping Voltage vs. Peak Pulse Current
(t_{period} = 100ns, t_r = 1ns)

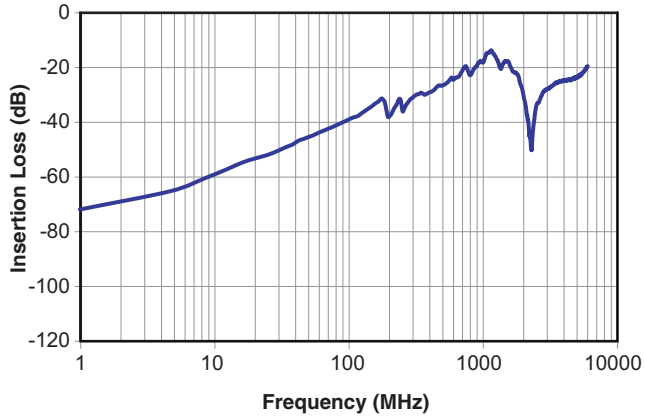


I/O – Gnd Insertion Loss (S21) vs. Frequency

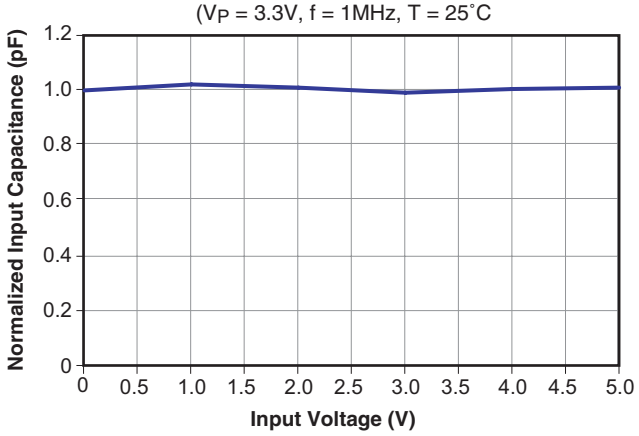
Forward Voltage vs. Forward Current
(t_{period} = 100ns, t_r = 1ns)



Analog Crosstalk (I/O–I/O) vs. Frequency



Typical Variation of C_{IN} vs. V_R)
(V_P = 3.3V, f = 1MHz, T = 25˚C



TDR for HDMI 1.3

The AOZ8905 TDR test results indicates the minimal effect the low capacitance has on the HDMI 1.3 TDR measurements. Below are the graphs from the TDR measurements. The two graphs show the before and after results of the TDR of each of the differential data line (Clock, D0, D1, D2) of the HDMI when the AOZ8905 was populated onto the PCB.

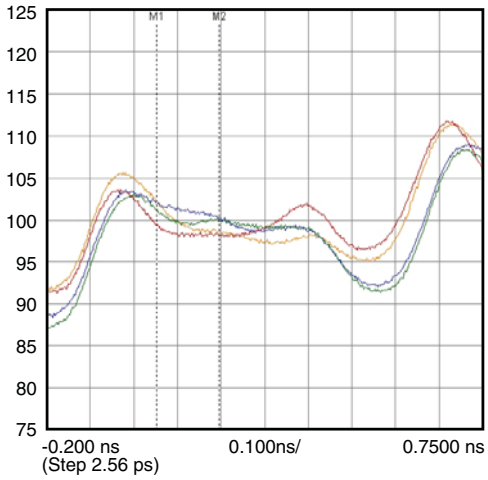


Figure 2. Ideal Stripe-Line

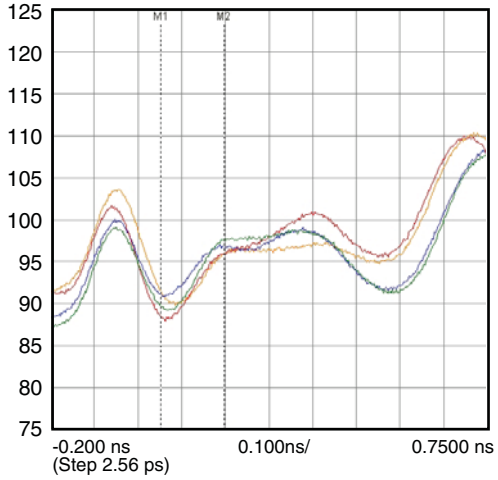


Figure 3. With AOZ8905 Device on the Board

(TDR Measurement with 200pS Rise Time Using AOS Evaluation Board)

High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8905 devices should be located as close as possible to the noise source. The placement of the AOZ8905 devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8905 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8905 device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8905 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8905 is designed for the ease of PCB layout by allowing the traces to run underneath the device. The pinout of the AOZ8905 is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI) or USB 3.0 design with minimal diversion of the signal lines that may add more parasitic inductance.

Based on the AOZ8905 SOT23-6 package design, a very straight forward layout can be achieved. To give the TDR an extra level of margin the traces may be compensated to have a nominal impedance of 90Ω throughout the differential pair. To make the design perfect the added capacitance of the device will have to be compensated by the use of “Skinny Traces”. The skinny traces are a narrow stripe line acting to lower the parasitic capacitance on the differential stripe line. The differential impedance of the USB 3.0 transmission line becomes well centered to 90Ω. A layout EM field simulator is recommended before fabrication to insure a perfect stripe line. With careful layout and placement of the device, the AOZ8905 can protect the USB 3.0 data line effectively and safely and meet the ESD immunity requirements of the IEC61000-4-2, level 4, ±15kV air discharge, ±8kV contact discharge.

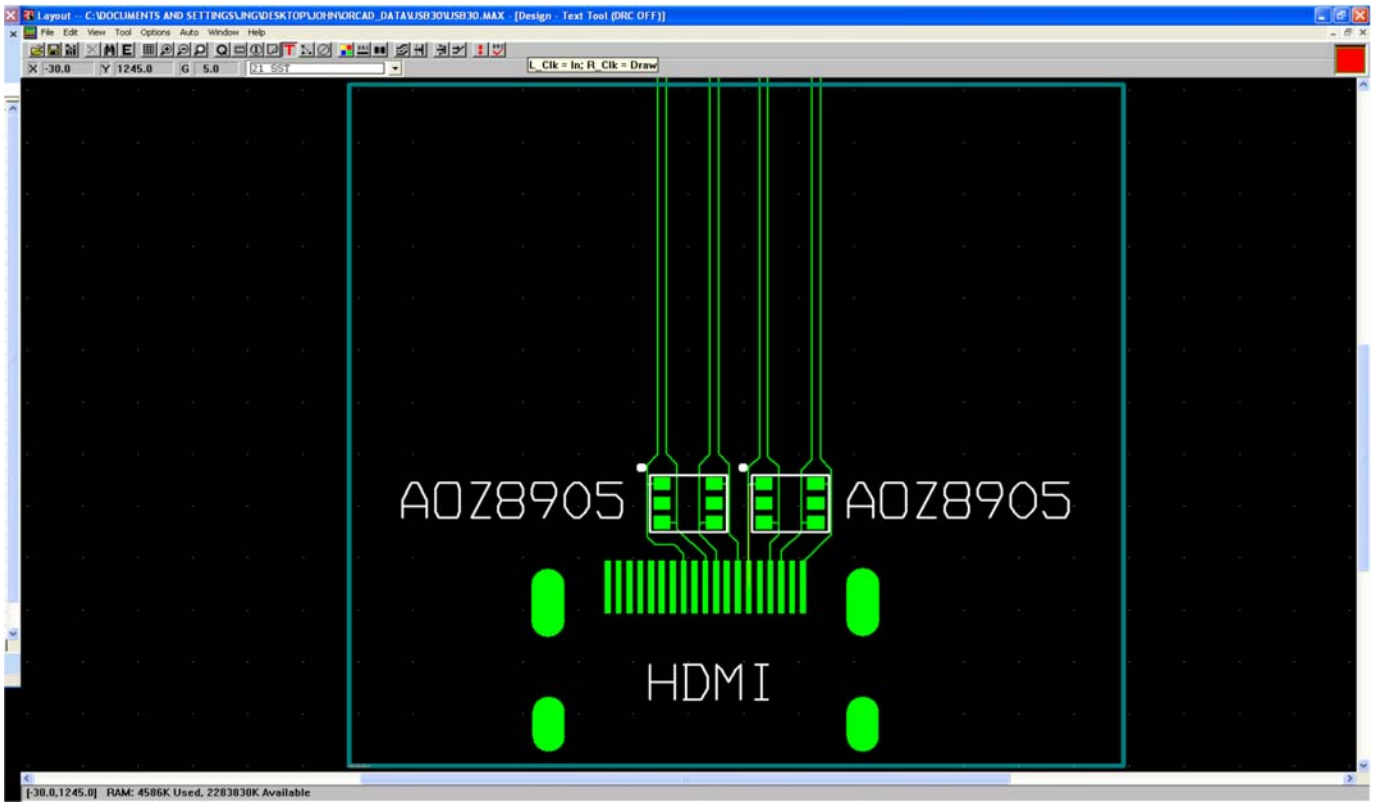
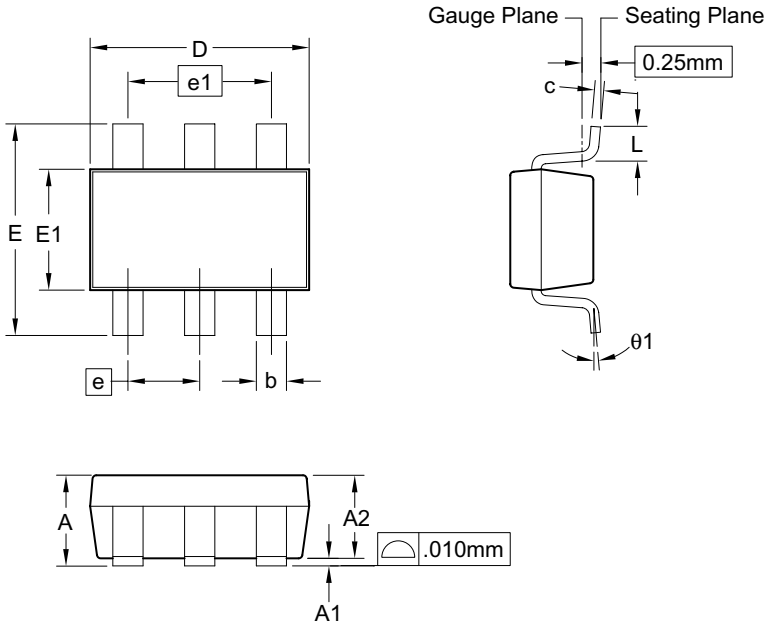


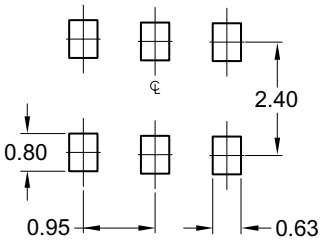
Figure 4. HDMI PCB Layout with Compensated Traces

Number of Layers	4
Copper Trace Thickness	1.4 mils
Dielectric Constant, ε_r	4.6
Overall Board Thickness	62 mils
Dielectric Thickness Between Top and Ground Layer	10 mils

Package Dimensions, SOT23-6L



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.90	—	1.25
A1	0.00	—	0.15
A2	0.80	1.10	1.20
b	0.30	0.40	0.50
c	0.08	0.13	0.20
D	2.70	2.90	3.10
E	2.50	2.80	3.10
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	—	0.60
θ1	0°	—	8°

Dimensions in inches

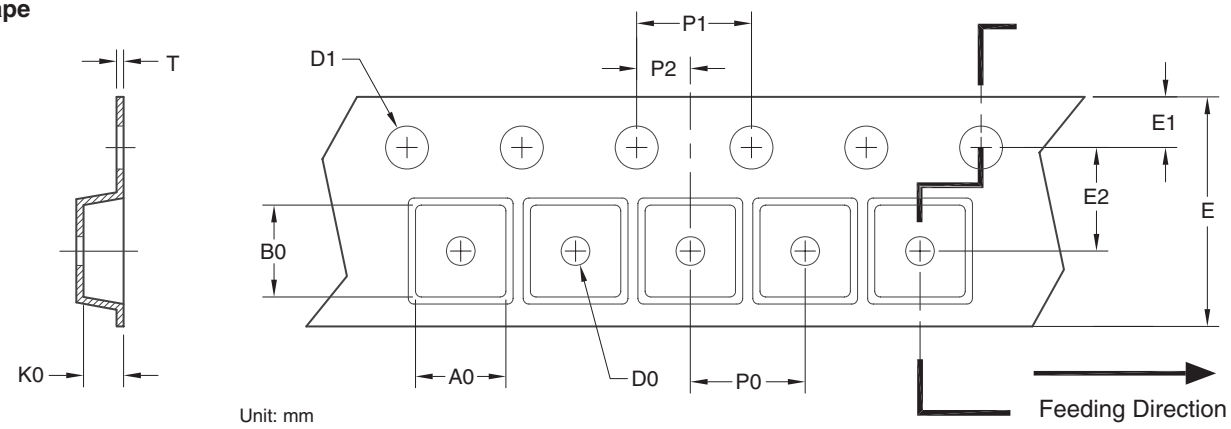
Symbols	Min.	Nom.	Max.
A	0.035	—	0.049
A1	0.00	—	0.006
A2	0.031	0.043	0.047
b	0.012	0.016	0.020
c	0.003	0.005	0.008
D	0.106	0.114	0.122
E	0.098	0.110	0.122
E1	0.059	0.063	0.067
e	0.037 BSC		
e1	0.075 BSC		
L	0.012	—	0.024
θ1	0°	—	8°

Notes:

1. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils each.
2. Dimension “L” is measured in gauge plane.
3. Tolerance ±0.100mm (4 mil) unless otherwise specified.
4. Followed from JEDEC MO-178C & MO-193C.
6. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SOT23-6L

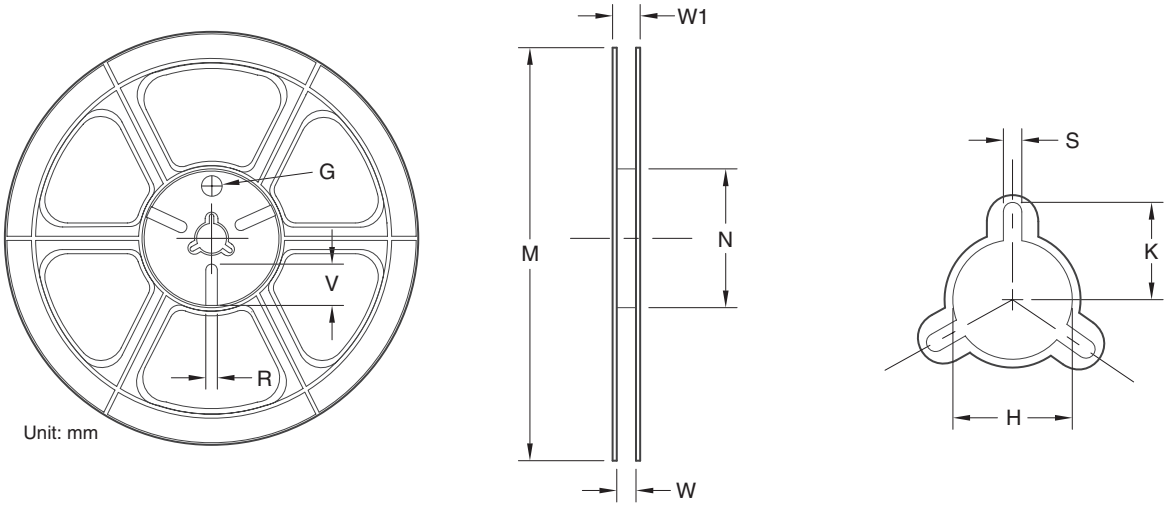
Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOT-23 (8mm)	3.15 ±0.10	3.20 ±0.10	1.40 ±0.10	1.00 Min.	1.50 ±0.10	8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.25 ±0.05

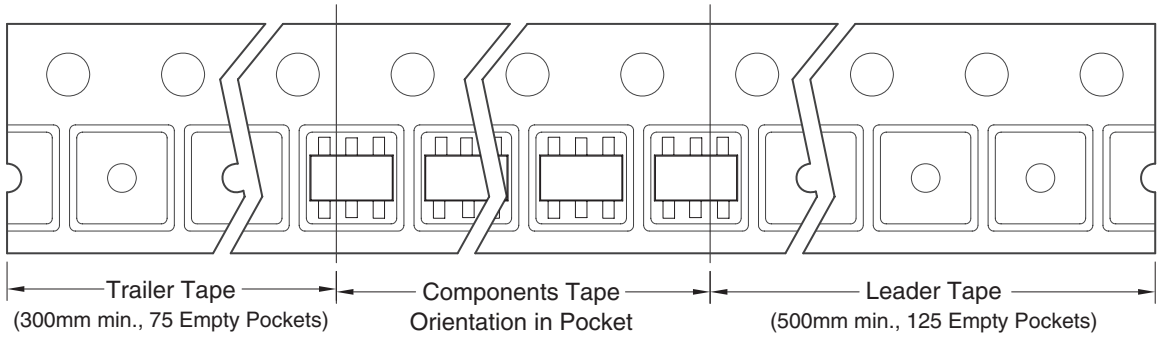
Reel



Unit: mm

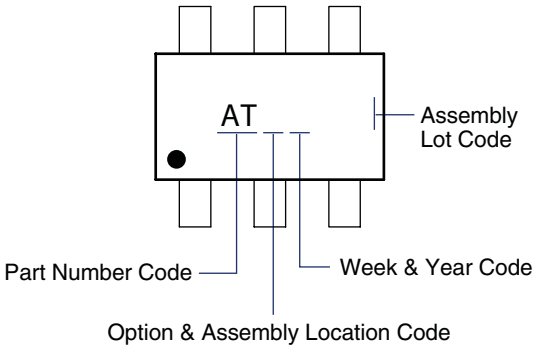
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
8mm	ø180	ø180.00 ±0.50	ø60.50	9.00 ±0.30	11.40 ±1.00	ø13.00 +0.50 / -0.20	10.60	2.00 ±0.50	ø9.00	5.00	18.00

Leader/Trailer and Orientation



Package Marking

AOZ8905CI
(SOT-23)



Revision History

Revision	Revised Item
Rev. 1.0	Initial release
Rev. 1.1	TDR and Layout Guidelines added