W83L786NR
W83L786NG
Nuvoton
H/W Monitoring IC

W83L786NR

Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	P.13	10/15/04	0.6	N/A	Pin 10: from Vram_SEN to VTIN1 Pin 11: from Vcore_SEN to D- Pin 13: from Vref to Vcore_SEN Pin 14: from D- to Vram_SEN Pin 15: from D1+ to Vref
2	P.14, P.18, P.51, P.55	11/15/04	0.7	N/A	Add pin function description, functional description, electrical characteristics and top marking explanation
3	P.1, P.3, P.5, P.9	07/04/05	0.8	N/A	Correct temp. sensor measurement method
4	N.A.	03/31/06	0.9	N/A	Add Pb-free package version; remove application circuit
5					

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1. GENERAL DESCRIPTION

W83L786NR/NG is an evolving product of W83L785R -- Nuvoton's most popular hardware monitoring IC, and intelligent fan controlling IC. Specifically designed for the graphic cards and barebone /mini systems, W83L786NR/NG can be used to monitor several critical hardware parameters of the system, including voltages, fan speeds, and temperatures, which are very important for the system to work stably and properly.

W83L786NR/NG can monitor up to 3 analog voltage inputs, 2 fan tachometer inputs, and 2 remote temperature sensors. One of the temperature inputs is connected to CPU/GPU thermal diode sensor, and the other remote temperature sensor could be performed by either thermal diode or thermistor. Power-on fan_set configuration offers the function to choose one of the four duty cycles, 100%, 81%, 62%, 43%, as initial fan speed. 2 sets of PWM (Pulse Width Modulation) / DC (Direct Current) fan output for SMART FAN^{TM} control – "Thermal Cruise^{TM}" mode and "SMART FAN^{TM} II "mode. Under "Thermal Cruise^{TM} "mode, temperatures of GPU and the system can be maintained within specific programmable ranges under the hardware control. Under "SMART FAN^{TM} II" mode, the fan could be operated at the lowest possible speed for minimum acoustic noise, and the dynamic intelligent fan management could create the most quiet system environment and stable working performance. An 8-bit analog-to-digital converter (ADC) is built inside W83L786NR/NG. As for warning mechanism, W83L786NR/NG provides four pure hardware event pins for independent warning signals: VOLTAGE_FAULT#, FAN_FAULT#, TEMP_FAULT#, and INT#. All threshold values could be set for system protection without any timing delay. One bit power-on address selection is used to decide the address of the W83L786NR/NG over I^{2}C serial bus interface. W83L786NR/NG also provides up to 7 optional multifunctional GPIO. W83L786NR/NG is powered by 3.3V.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper / preset range. The application software could be Nuvoton's Hardware Doctor^{TM}, Intel^{TM} LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable interrupts. For the spacing saving consideration of the Graphic cards and Notebook system, W83L786NR/NG is 20-pin SSOP package.

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2. FEATURES

2.1 Monitoring Items

2.1.1 Temperature
- Measure the temperature with high accuracy.
- One thermal diode sensor (current mode) connected to CPU/GPU and one remote sensor either by thermal diode (current mode) or thermistor.
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items.

2.1.2 Voltage
- 3 voltage sensor inputs.
  --- Typically for Vcore, RAM, etc.

2.1.3 Fan
- 3D/2D application being used and transferring fan set to the most appropriate fan speed control.
- Fan set: power on configuration for fan speed at four rotation rate levels at 43%, 62%, 81%, and 100% duty cycle.
- Two DC/PWM fan output control.
- SMART FAN™ function compliant.

2.2 Actions Enabling
- Total up to 2 sets of fan speed monitoring and controlling.
- Issue FAN_FAULT#, VOLTAGE_FAULT#, TEMP_FAULT#, and INT# signals to activate system protection.
- Warning signal pop-up in application software.

2.3 General
- Interface: I²C / SMBus control.
- 1 bit I²C address selection.
- Up to 7 GPIOs.
- Nuvoton hardware monitoring application software (Hardware Doctor™) support Windows 95 / 98 / 2000 / XP and Windows NT 4.0 / 5.0.
- 3.3V V_{CC} operation.

2.4 Package
- 20-pin SSOP (209mil).

3. KEY SPECIFICATIONS

- Voltage monitoring accuracy $\pm 3\%$ (typ.)
- Monitoring temperature range and accuracy $0°C$ to $+160°C$; $\pm 3°C$ (max.)
- Supply voltage $3.3V \pm 10\%$
- Operating supply current 2 mA (typ.)
- Power down supply current 10 uA (typ.)
- ADC resolution 8 Bits

4. BLOCK DIAGRAM

5. PIN CONFIGURATION

FAN_FAULT/GPIO1	1	20	VOLTAGE_FAULT#/GPIO7
TEMP_FAULT#/GPIO2	2	19	INT#
SCL	3	18	PWM/DC_OUT2/GPIO6
SDA	4	17	PWM/DC_OUT1
Vcc	5	16	GND
ADDR/GPO3	6	15	*VREF*
FAN_SET/GPO4	7	14	*V$_{RAM}$_SEN*
FANIN1	8	13	*V$_{CORE}$_SEN*
FANIN2/GPIO5	9	12	*D+*
VTIN1	10	11	*D-*

W83L786NR
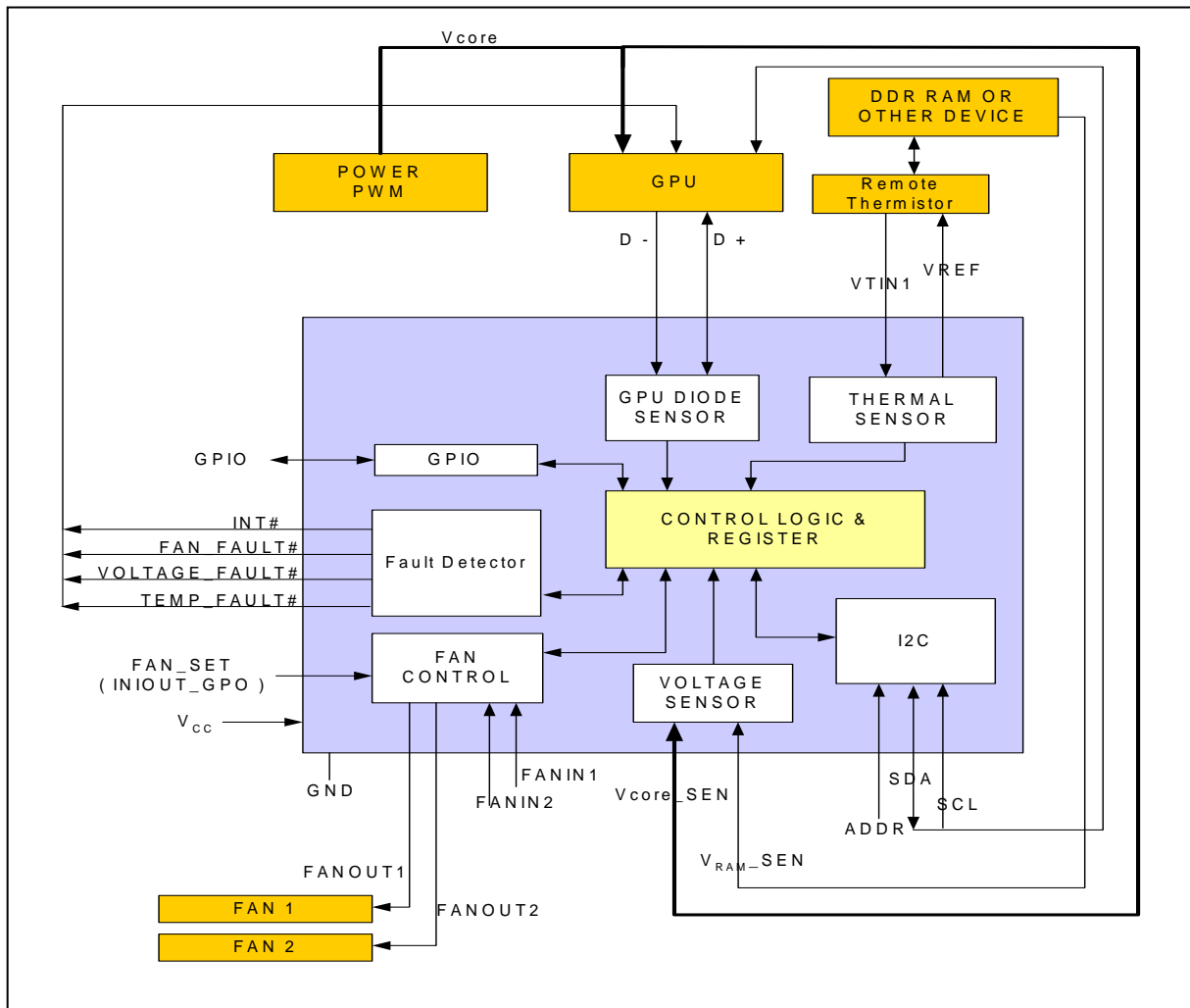
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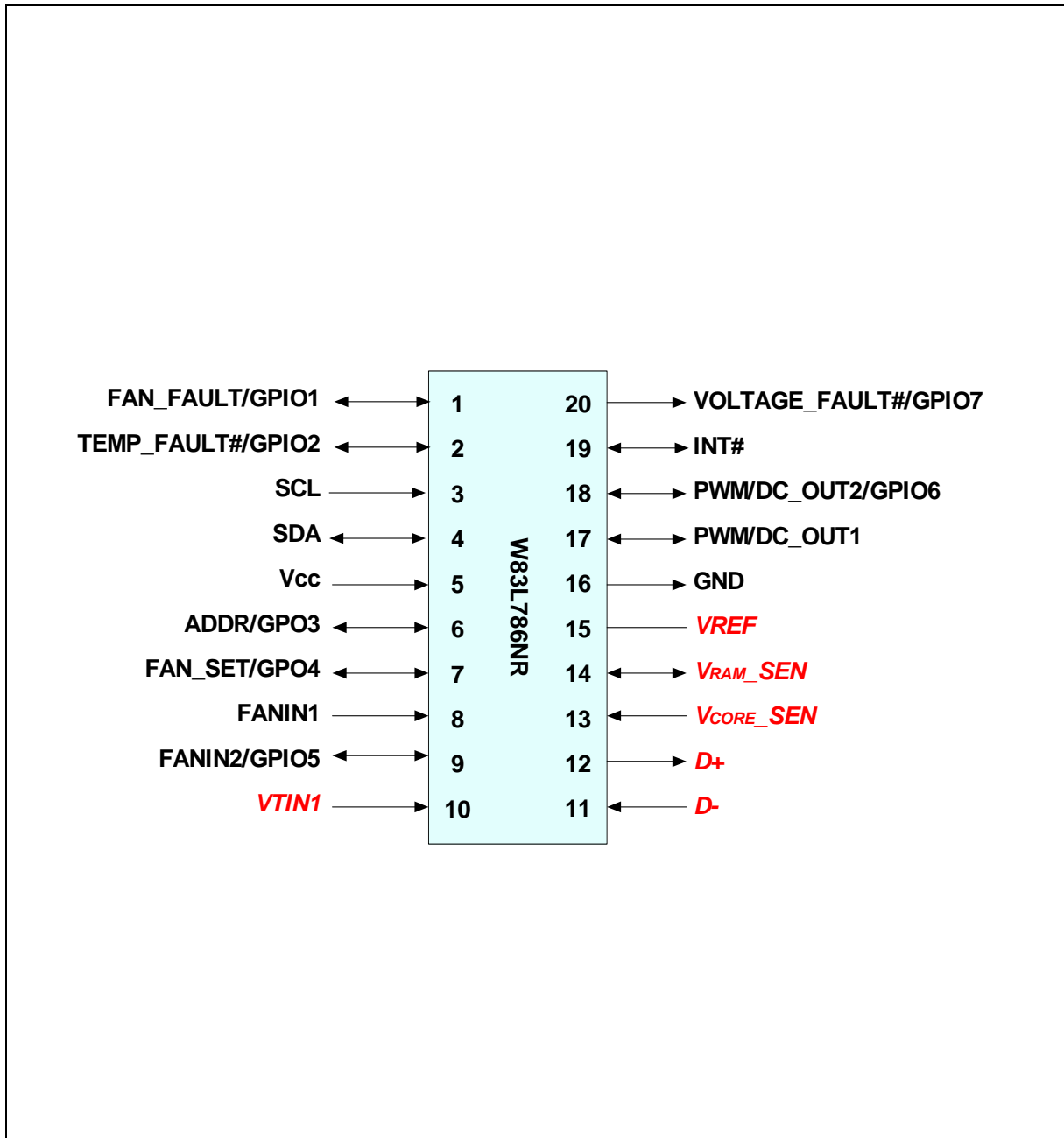
6. PIN DESCRIPTION

PIN TYPE	PIN ATTRIBUTE
I/O$_{12t}$	TTL level bi-directional pin with 12 mA source-sink capability
I/O$_{12ts}$	TTL level and schmitt trigger with 12 mA source-sink capability
I/O$_{8ts}$	TTL level and schmitt trigger with 8 mA source-sink capability
I/O$_{6ts}$	TTL level and schmitt trigger with 6 mA source-sink capability
I/OD$_{12ts}$	TTL level and schmitt trigger open drain output with 12 mA sink capability
OUT$_{12}$	Output pin with 12 mA source-sink capability
OD$_{12}$	Open-drain output pin with 12 mA sink capability
AOUT	Output pin (Analog)
IN$_t$	TTL level input pin
IN$_{ts}$	TTL level input pin and schmitt trigger
AIN	Input pin(Analog)

PIN NAME	NO	PIN TYPE	DESCRIPTION
FAN_FAULT#	1	OD$_{12}$	Active-Low output. This pin will be a logic LOW when the fan1 or fan2 is abnormally stopped. (Default)
GPIO1		I/OD$_{12TS}$	General purpose I/O function. This multi-functional pin is programmable.
TEMP_FAULT#	2	OD$_{12}$	Active-Low output. This pin will be a logic LOW when the temperature of the system or CPU exceeds its limit. (Default)
GPIO2		I/OD$_{12TS}$	General purpose I/O function. This multi-functional pin is programmable.
SCL	3	IN$_{ts}$	Digital Input. SMBus serial clock input. Requires SMBus pull-up.
SDA	4	I/OD$_{12}$	Digital I/O (Open drain). SMBus bidirectional serial data. Requires SMBus pull-up.
Vcc	5	POWER	Power supply input.

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PIN NAME	NO	PIN TYPE	DESCRIPTION
ADDR	6	IN_{TS}/OUT_{12}	Determines the SMBus device address.
GPO3			General purpose Output function. This multi-functional pin is programmable.
FAN_SET	7	AIN	Determines the FAN initial speed. Power on configuration for fan speed at four rotation rate levels at 43%, 62%, 81%, and 100%.
GPO4		OUT_{12}	General purpose Output function. This multi-functional pin is programmable.
FANIN1	8	IN_{TS}	0V to +3.3V amplitude fan tachometer input. (Default)
FANIN2	9	IN_{TS}	0V to +3.3V amplitude fan tachometer input. (Default)
GPIO5		OUT_{12TS}	General purpose I/O function. This multi-functional pin is programmable.
VTIN1	10	AIN	Analog Input. Connect to either diode sensor (current mode) or thermistor. Anode to VTIN1 if VTIN1 is connected to diode sensor (current mode).
D-	11	AIN	Thermistor 2 terminal input (Default) / Cathode to CPU Thermal Diode. Also cathode to VTIN1 if VTIN1 is connected to diode sensor (current mode). **Please connect this pin to the ground, see page 15, figure 5.**
D+	12	AIN	Thermistor 1 terminal input (Default) / Anode to CPU Thermal Diode.
V_{CORE}_SEN	13	AIN	Analog Input. Monitors CPU core voltage (0V-3V).
V_{RAM}_SEN	14	AIN	Analog Input. Monitors RAM's voltage.
VREF	15	AOUT	Reference voltage.

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PIN NAME	NO	PIN TYPE	DESCRIPTION
GND	16	GROUND	Ground pin for the W83L786NR
PWM / DC OUT1	17	OD_{12}	Fan speed control output. This pin is default DC output level. It can be programmed as PWM output.
PWM / DC OUT2	18	OD_{12}	Fan speed control output. This pin is default DC output level. It can be programmed as PWM output.
GPIO6		I/OD_{12TS}	General purpose I/O function. This multi-functional pin is programmable.
INT#	19	OD_{12}	System Interrupt.
VOLTAGE_FAULT#	20	OD_{12}	Active-Low output. This pin will be a logic LOW when the voltage exceeds its high/low limit. (Default)
GPIO7		I/OD_{12TS}	General purpose I/O function. This multi-functional pin is programmable..

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7. FUNCTIONAL DESCRIPTION

7.1 General Description

The W83L786NR/NG provides 3 analog voltage inputs, 2 fan speed inputs and outputs which support both PWM (Pulse Width Modulation) fan control and DC (Direct Current) fan control, all of them being implemented with SMART FAN™ I and SMART FAN™ II, and 2 sets of thermal inputs for CPU/GPU thermal diode sensor or remote temperature sensor. W83L786NR/NG is I^2C / SMBus interface compatible. Furthermore, the Watch Dog Timer will monitor every function and store the values to registers for comparison with preset ranges. If the monitored value exceeds the limit value, the interrupt status will be set to 1 and W83L786NR/NG will issue interrupt signals such as INT# and IRQ if not masked. W83L786NR/NG also provides software and hardware Watch Dog Timer to avoid system hang on.

7.2 Access Interface

The W83L786NR/NG provides I^2C Serial Bus for microprocessor to read/write internal registers, and the I^2C address default value is 01011110b (Pin 6 pull high). If Pin 6 pulls low, the I^2C address value is 01011100b.

7.3 The First Serial Bus Access Timing

(a) Serial bus writes to internal address register followed by the data byte

Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte
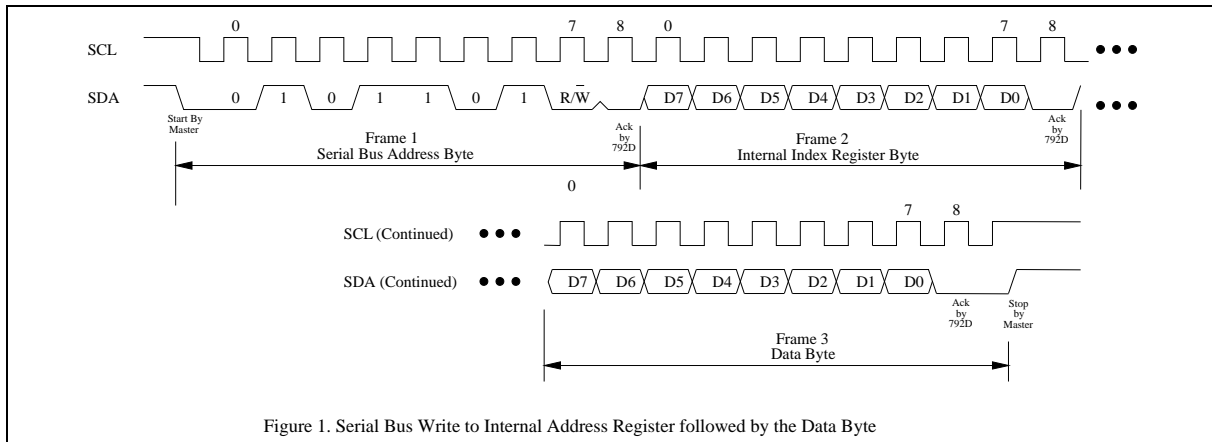
(b) Serial bus read from a register

Figure 2. Serial Bus Read from Internal Address Register
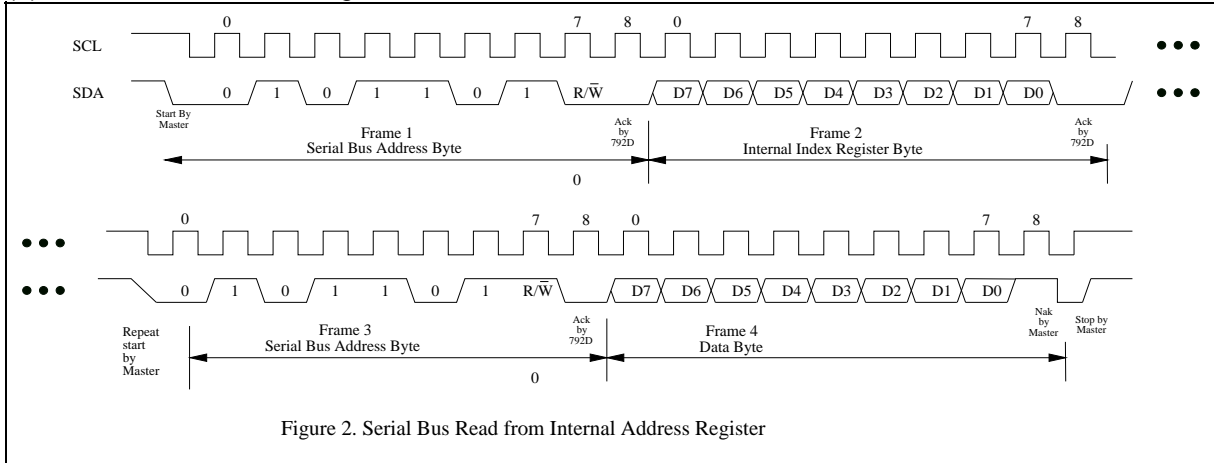
7.4   Analog Inputs

The maximum input voltage of the analog pin is 2.048V because the 8-bit ADC has the 8mV LSB. Actually, the application of the voltage monitoring would most often be connected to power suppliers. The input voltage lower than 2.048V could directly connect to the analog inputs. The inputs voltage higher than 2.048V should be reduced by external resistors so as to meet the input range. This is shown in Figure 3.

Figure 3

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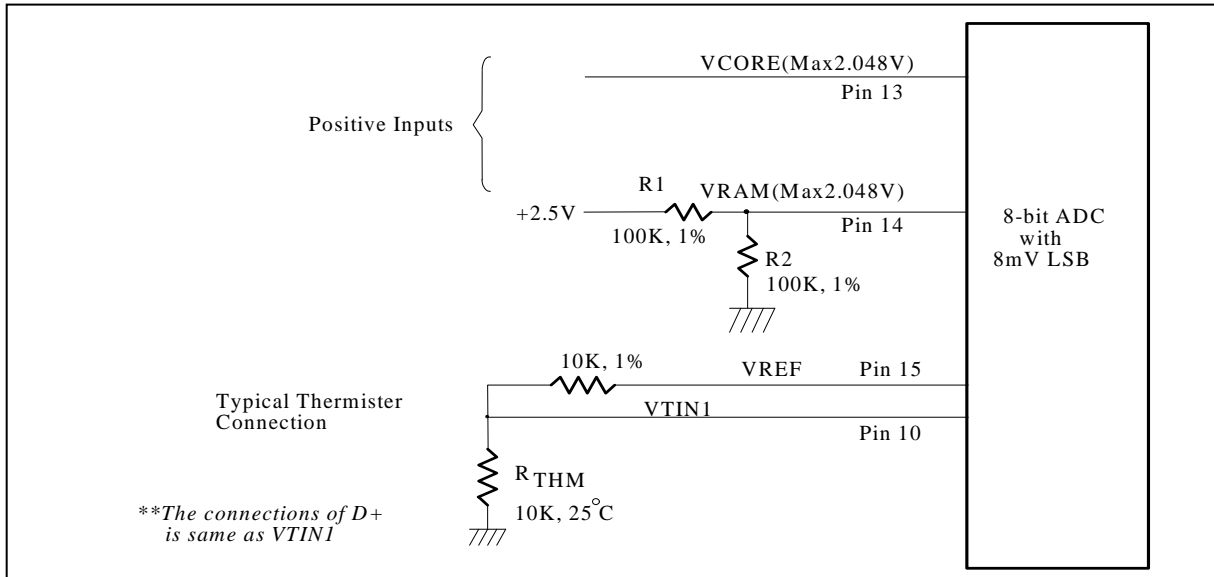
7.4.1   Voltage Input can not be over 2.048V

The input voltage Vcore, and Vram can be expressed as following equation:

$$VRAM = V_{+2.5V} \times \frac{R_2}{R_1 + R_2}$$.   V$_{+2.5V}$ is +2.5V inputs.

The value of R1 and R2 can be selected to 100K Ohms and 100K Ohms, respectively, when the input voltage is 2.5V. The node voltage of VRAM can be subject to less than 2.048V for the maximum input range of the 8-bit ADC. The pin 5 is connected to the power supply V$_{CC}$ with +3.3V. There are two functions in this pin with 3.3V: the first function is to supply internal analog power of the W83L786NR/NG and the second function is to connect this pin to internal serial resistors to monitor the +3.3V voltage. The values of two serial resistors are 20K ohms and 40K ohms so that input voltage to ADC is 1.1V which is less than 2.048V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{20K\Omega}{20K\Omega + 40K\Omega} \cong 1.1V$$

where VCC is set to 3.3V.

7.4.2   Voltage Fault (VOLTAGE_FAULT #)

W83L786NR/NG provides a good protection for voltage. Set Pin 20 (VOLTAGE_FAULT#) to monitor voltage. When Vcore (Pin13), Vram (Pin14), or VCC (Pin5) voltage exceeds high or low voltage limit in VR2B ~ VR34, Pin 20 VOLTAGE_FAULT# will be asserted (Figure 4).
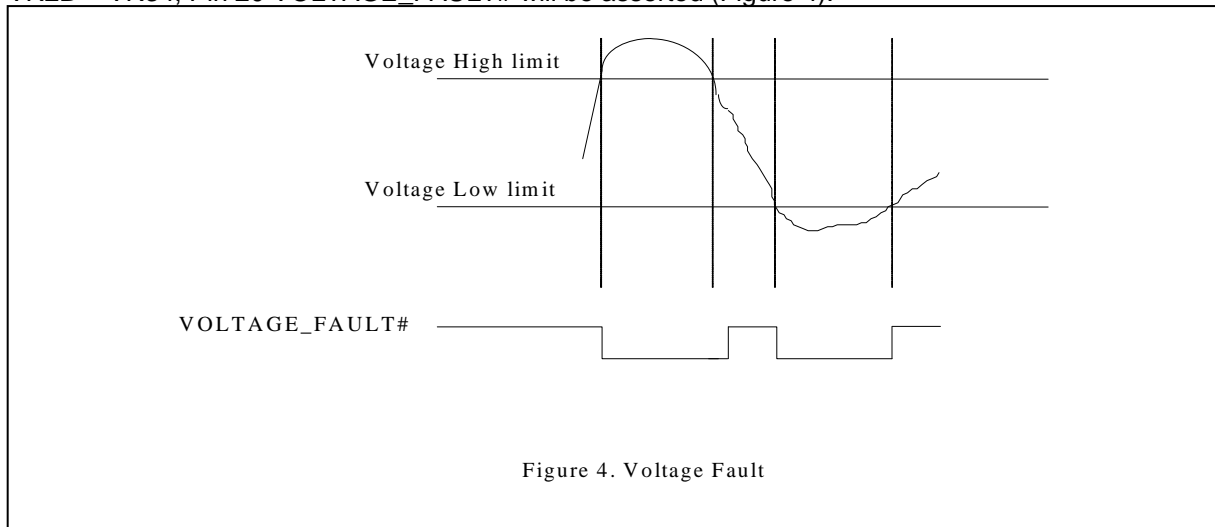
Figure 4. Voltage Fault

7.5   Temperature Measurement Machine

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The temperature data format is 8-bit unsigned for thermal sensor. The 8-bit temperature data can be obtained by reading the VR [25h] or VR [26h]. The format of the temperature data is shown in Table 1.

TEMPERATURE	8-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX
+160°C	1010,0000	A0h
+25°C	0001,1001	19h
+2°C	0000,0010	02h
+1°C	0000,0001	01h
+0°C	0000,0000	00h

Table 1

7.5.1 Monitor Temperature from Thermistor

The W83L786NR/NG can connect one thermistor and one thermal diode sensor to measure two different environment temperatures. The specification of thermistor should be considered to (1) β value is 3435 K, and (2) resistor value is 10K ohms at 25°C. In the Figure 3, the themistor is connected by a serial resistor with 10K Ohms, and then connect to V_{REF} (pin 15).

7.5.2 Monitor Temperature from Thermal Diode

The W83L786NR/NG can alternate the thermistor to thermal diode interface and the circuit connection is shown as Figure 5. The pin of D- is connected to power supply ground (GND) and the pin D+ is connected to pin D+ or VTIN1 in the W83L786NR/NG. The bypass capacitor C=2200pF should be added to filter the high frequency noise.

Figure 5

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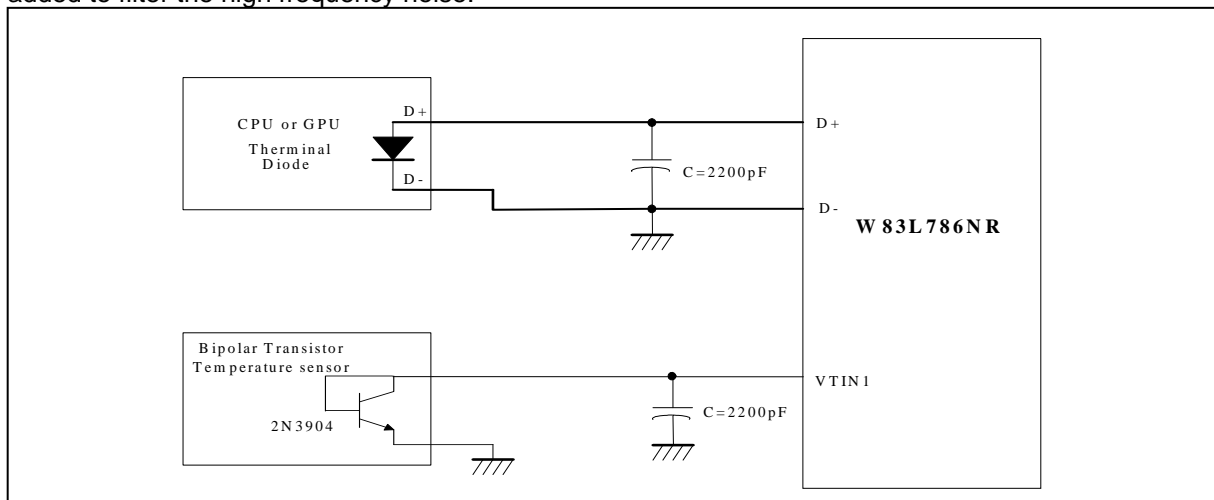
7.5.3   Temperature Fault (TEMP_FAULT #)

W83L786NR/NG provides a good protection for temperature fault. Set Pin 2 (TEMP_FAULT#) to monitor temperature. When D+-D- (Pin12, 11), or VTIN1 (Pin10) temperature exceeds temperature fault limit in VR35 or VR37, Pin 2 TEMP_FAULT# will be asserted (Figure 6).

Figure 6. TEMP_FAULT
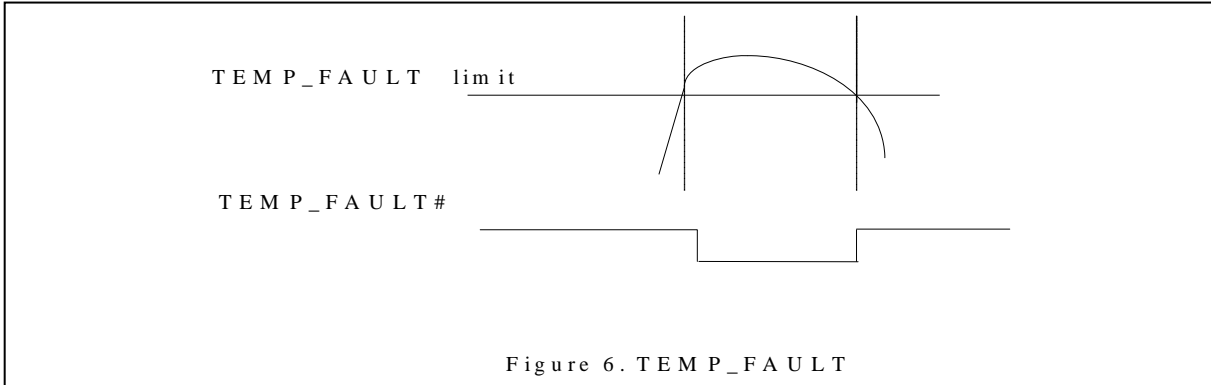
7.6   FAN Speed Count and FAN Speed Control

7.6.1   Fan Speed Count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over V_{CC}. If the input signals from the tachometer outputs are over the V_{CC}, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown in Figure 7.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register VR28 or VR29, and the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR54.bit0~2, bit4~6 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. Table 2 is an example for the relation of divisor, RPM, and count.

DIVISOR	NOMINAL RPM	TIME PER	COUNTS	70% RPM	TIME FOR 70%

		REVOLUTION			
1	8800	6.82 ms	*153*	6160	9.74 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

Table 2

Figure 7-1. Fan with Tach Pull-Up to +12V, or Totern-Pole Output and Register Attenuator

Figure 7-2. Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

Figure 7-3. Fan with Tach Pull-Up to +5V, or Totern-Pole Output and Register Attenuator

Figure 7-4. Fan with Tach Pull-Up to +5V, or Totem-Pole Putput and Zener Clamp

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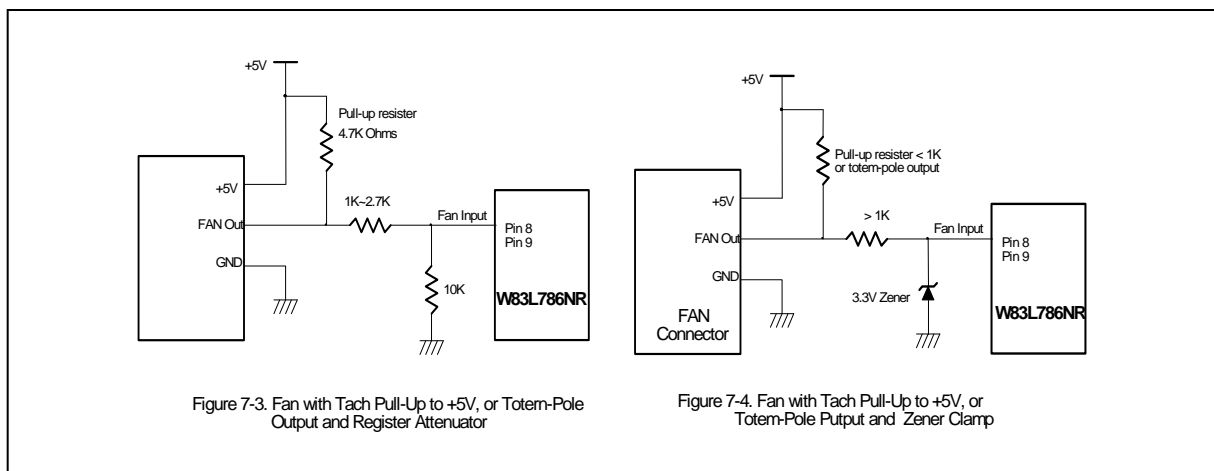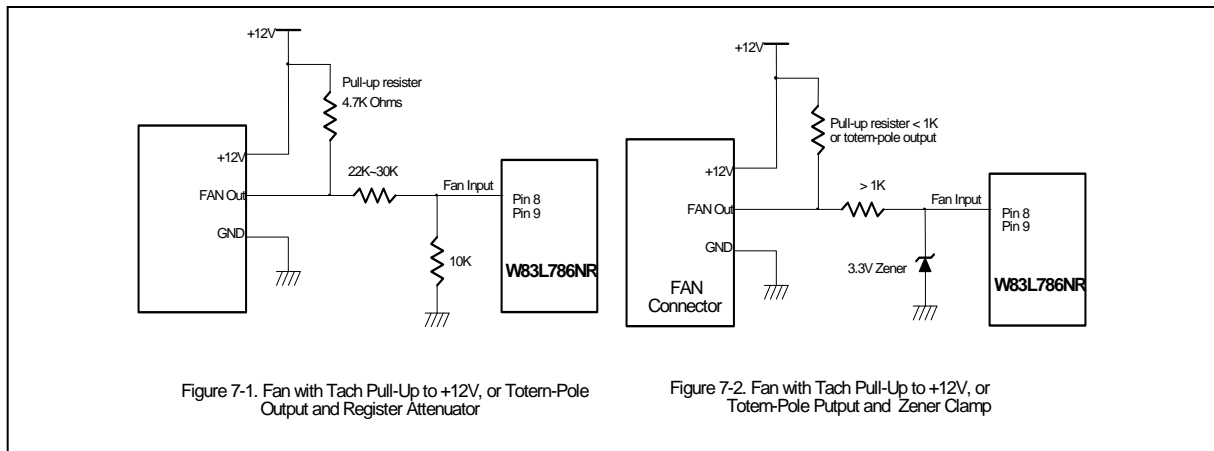
7.6.2   Fan Speed Control

The W83L786NR/NG provides two sets for PWM/DC fan speed control. The duty cycle of PWM or the output voltage of DC can be programmed by a 4-bit register. There are four mode to control fan speed which are set by programming CR80 [3:2] and CR [5:4], and default are FAN_SET mode.

7.6.2.1. Default Fan Speed Setting

There is a pin to set the default value for fan speed control by adjusting external serial resistors. After power up, the default value will be stored in CR90 (FAN_SET mode). The figure and table are shown below.
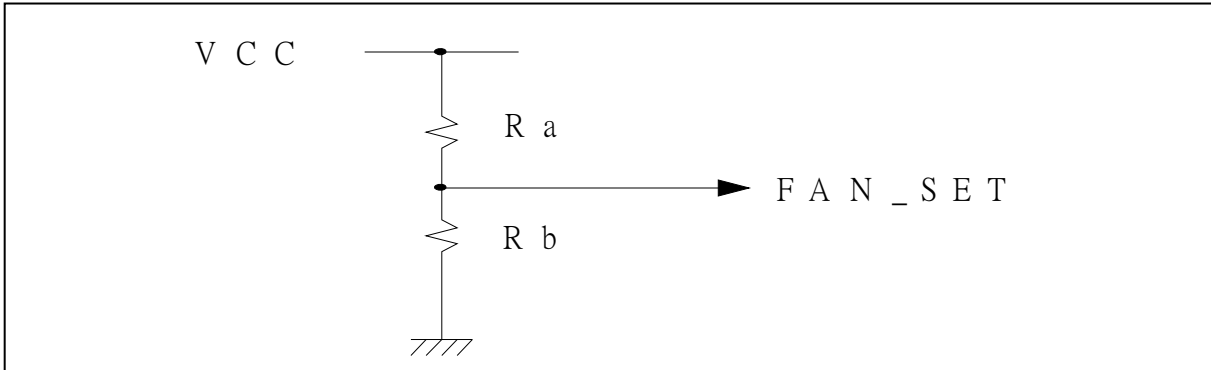
SECTION	FAN SPEED RATE	RA	RB
3	100%	9.1K	×
2	81%	4.7K	9.1K
1	62%	9.1K	4.7K
0	43%	×	9.1K

Figure 8 OFFSET Setting

7.6.2.2. PWM Mode

$$Duty - cycle(\%) = \frac{Programmed\ 4 - bit\ Register\ Value}{16} \times 100\%$$
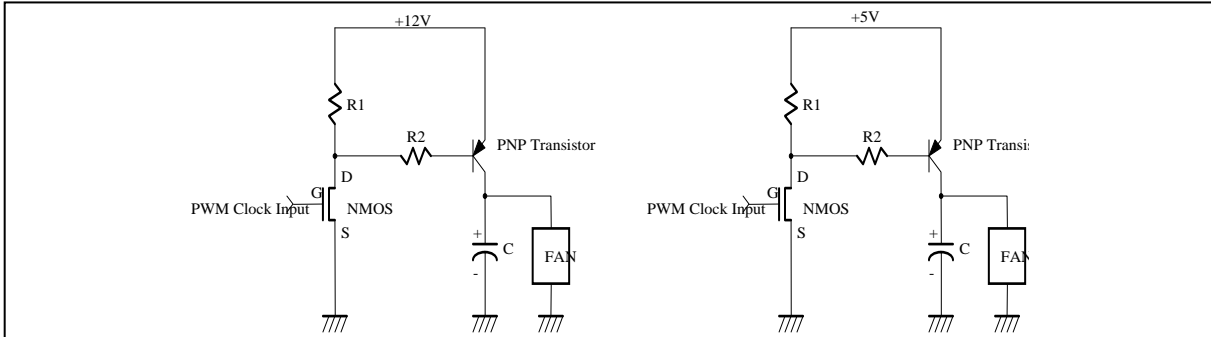
Figure 9

7.6.2.3. DC Mode

W83L786NR/NG has a 4-bit DAC, which produces 0 to 3.3 voltages DC output that provides maximum 2 sets for fan speed control. The analog output can be programmed in the CR 81, and CR 87 (manual mode). The expression of output voltage can be represented as follows,

$$\text{OUTPUT Voltage} = \text{VCC} \times \frac{\text{Programmed 4 - bit Register Value}}{16}$$

The application circuit is shown as follows,
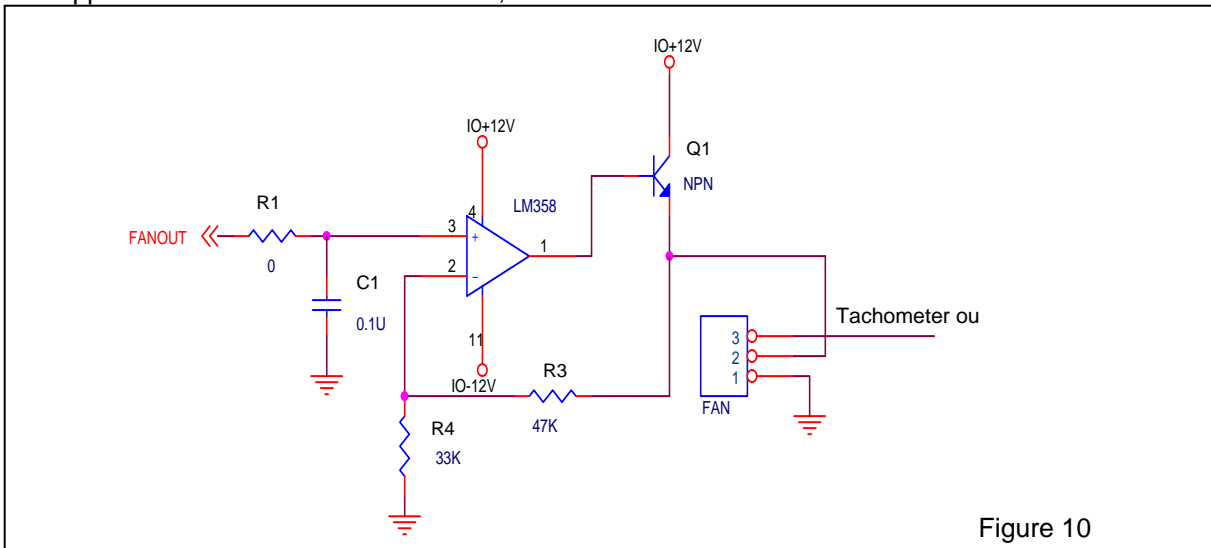
Figure 10

Be careful when choosing the OP-AMP and the transistor. The OP-AMP is used for amplify the 5V range of the DC output up to 12V. The transistor should has a suitable β value to avoid its base current pulling down the OP-AMP 's output and gain the common current to operate the fan at fully speed. (For more cost and effort efficient solution please refer to W83391TS/QS – the DC fan pre-driver that could provide up to 24V gate voltage for external N-channel MOSFET driving)

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7.6.3 SMART FANTM I Control

W83L786NR/NG supports two sets SMART FAN^{TM} I function and mapping to D+,D- (PWM/DC_OUT1), VTIN1 (PWM/DC_OUT2) . If CR80 [3:2] or CR80 [5:4] set to 2'b10, Fan1 or Fan2 will enable SMART FAN^{TM} I function.

At this mode, W83L786NR/NG provides the SMART FAN^{TM} system to automatically control fan speed to keep the temperatures of CPU and the system within specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS and the fan speed will be lowered as long as the current temperature remains below the setting value. Once the temperature exceeds the high limit (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its full speed but the temperature still exceeds the high limit (ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but still above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target range (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset stop value until the temperature exceeds the low limit.

Figure 11-1, 11-2 gives an illustration of Thermal Cruise Mode.
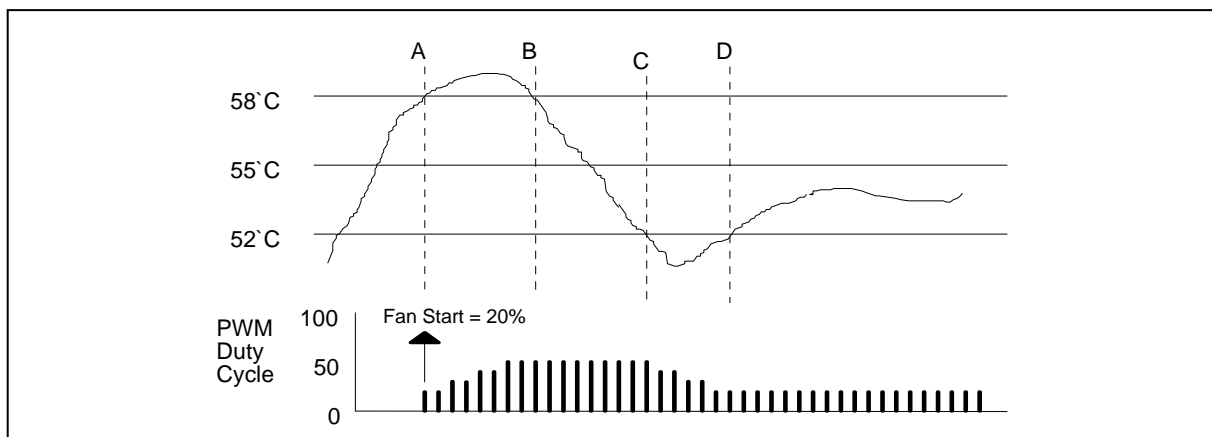
Figure 11-1
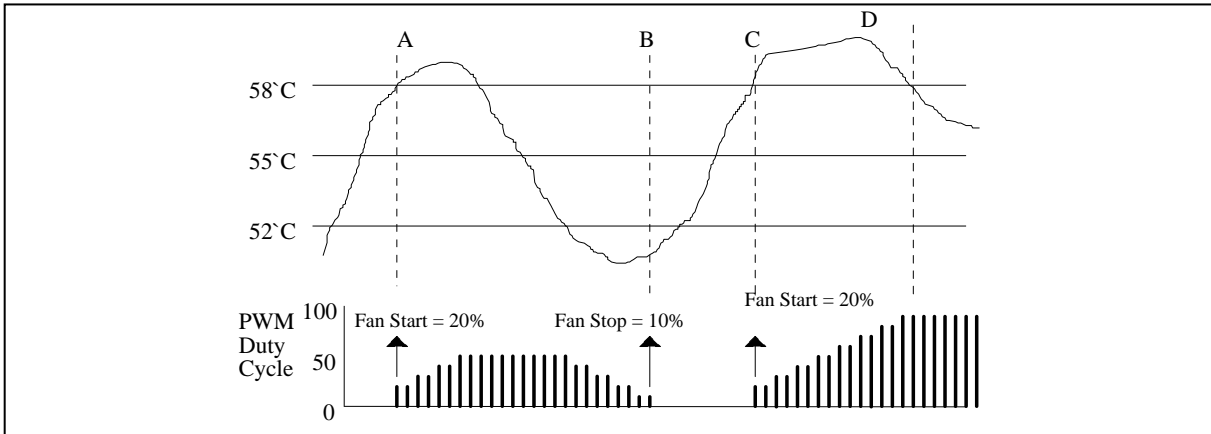
Figure 11-2

Of course, SMART FAN^{TM} control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

7.6.4 SMART FANTM II Control

W83786NR/NG provides 4 temperature points each can automatically control PWM or DC fan mode. Each temperature maps different fan out level, the relationship is shown as follows:
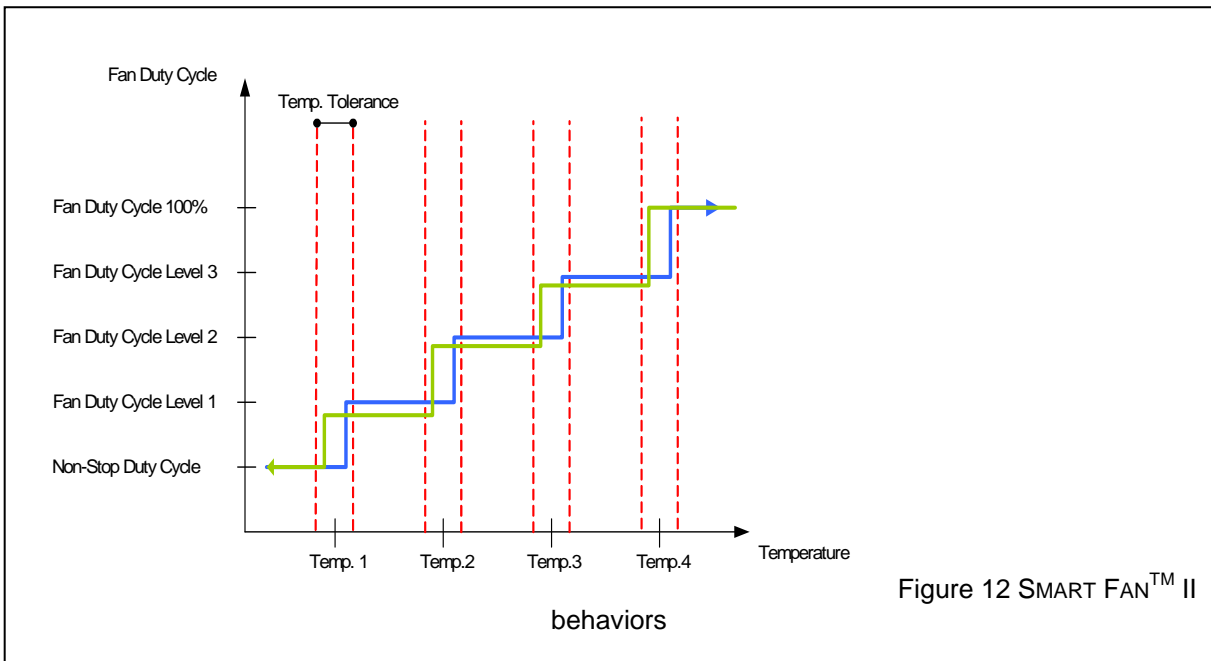
Figure 12 SMART FAN^{TM} II behaviors

The SMART FAN^{TM} II, a new innovation of Nuvoton, is specifically designed to operate fans at the lowest possible speed so as to minimize acoustic noise. As the figure shown above, it is clear that SMART FAN^{TM} II describes a relationship between Fan PWM Duty Cycle/DC Level and temperature. Users can program CR [80h] to enable SMART FAN^{TM} II mode. SMART FAN^{TM} II registers allow users to define suitable fan output levels to improve acoustic noise, power consumption and reliability issues regarding to specific fan.

Each fan has 4 duty cycle registers and 4 temperature point registers to setup the relation between fan output and temperature. Tolerance registers CR [8Dh] is used to postpone the response of fan output and avoid fan output throttles at each temperature point because fan throttling might produce some undesired noise.

The mechanism of SMART FAN^{TM} II is described as follows:

(1) At first, the fan speed operates at Non-Stop Duty Cycle, and keeps constant while temperature rises. When rising temperature hits critical Temp.1, fan speed remains unchanged. If the temperature keeps on rising and finally hits the upper edge of Temp. Tolerance of Temp.1, it triggers the fan speed change mechanism and fan speed jumps from Non-Stop Duty Cycle to Fan Duty Cycle Level 1.

(2) Fan speed remains constant at Fan Duty Cycle Level 1 even though the monitored temperature hits Temp.2.

(3) Fan speed will directly jump from Fan Duty Cycle Level 1 to Fan Duty Cycle Level 2 while the monitored temperature hits the upper edge of Temp. Tolerance of Temp.2.

(4) Same mechanism happens between Temp.3 and Temp.4.

(5) If the monitored temperature between Temp.3 and Temp.4, for example, begins to fall, the fan will keep its speed at Fan Duty Cycle Level 3, which is a constant.

(6) If the monitored temperature keeps on falling, the fan speed still remains the same unless the temperature hits the lower edge of Temp. Tolerance of Temp.3.

(7) Once the monitored temperature hits the lower edge of Temp. Tolerance of Temp.3, the fan speed reduces directly from Fan Duty Cycle Level 3 to Fan Duty Cycle Level 2, and keeps the same speed until the temperature hits the next lower edge of Temp. Tolerance.

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REGISTER	D+, D- – FAN1	VTIN1 – FAN2	
Non-Stop Duty Cycle	CR[81h] b3:b0	CR[87h] b3:b0	
Duty Level 1	CR[81h] b7:b4	CR[87h] b7:b4	
Duty Level 2	CR[82h] b3:b0	CR[88h] b3:b0	
Duty Level 3	CR[82h] b7:b4	CR[88h] b7:b4	
Temp Point 1	CR[83h] b7:b0	CR[89h] b7:b0	
Temp Point 2	CR[84h] b7:b0	CR[8Ah] b7:b0	
Temp Point 3	CR[85h] b7:b0	CR[8Bh] b7:b0	
Temp Point 4	CR[86h] b7:b0	CR[8Ch] b7:b0	
Tolerance	CR[8Dh] b3:b0	CR[8Dh] b7:b4	

7.6.5 Fan Fault (FAN_FAULT #)

W83L786NR/NG provides a good protection for fan speed. Set Pin 1 (FAN_FAULT#) to monitor fan speed. When FANIN1 (Pin8) or FANIN2 (Pin9) exceeds fan count high limit in VR3B or VR3C. Pin1 FAN_FAULT# will be asserted (Figure 13).

Figure 13. FAN_FAULT
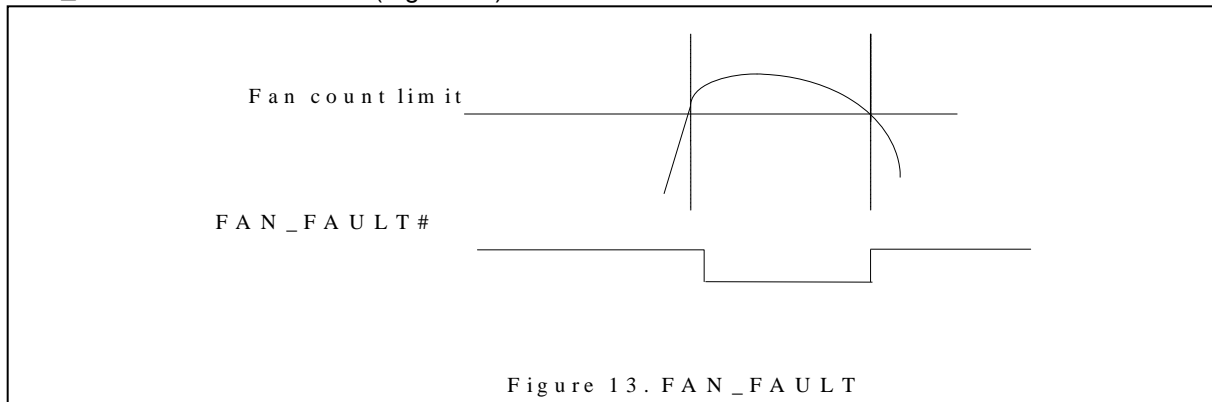
7.7   Fault Signal—INT#

7.7.1   Temperature

Pin INT# for temperature has 3 modes.

7.7.1.1. Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset when reading all of the Interrupt Status Registers. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}.   (Figure 14-1)

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7.7.1.2. Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 14-2)

7.7.1.3. One-Time Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, an interrupt will not occur again until the temperature exceeding T_O. (Figure 14-3)

*Interrupt Reset when Interrupt Status Registers are read

Figure 14-1. Comparator Interrupt Mode   Figure 14-2. Two-Times Interrupt Mode

* Interrupt Reset when Interrupt Status Registers are read

Figure 14-3. One-Time Interrupt Mode
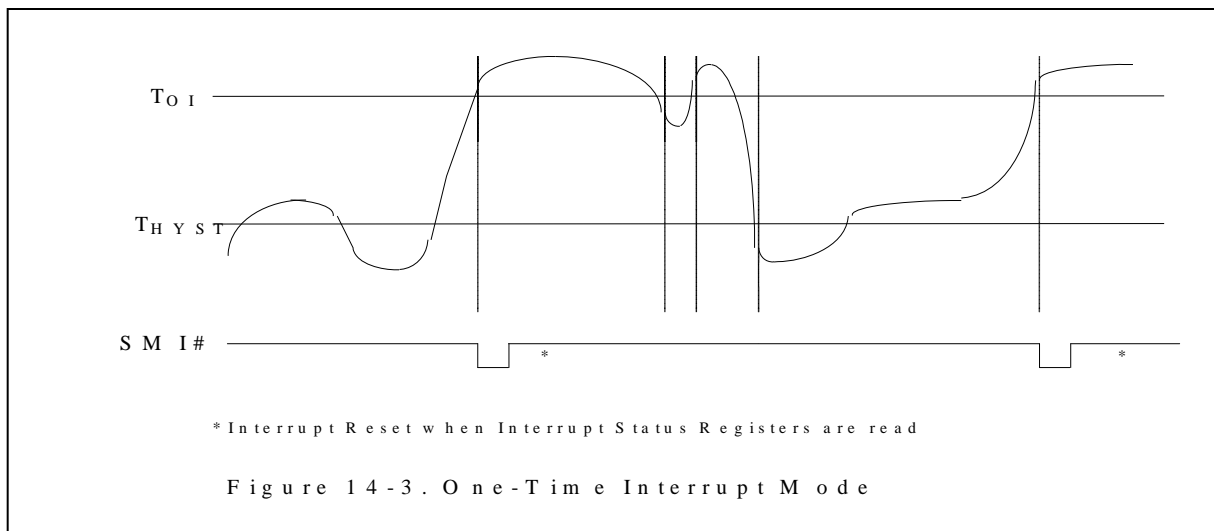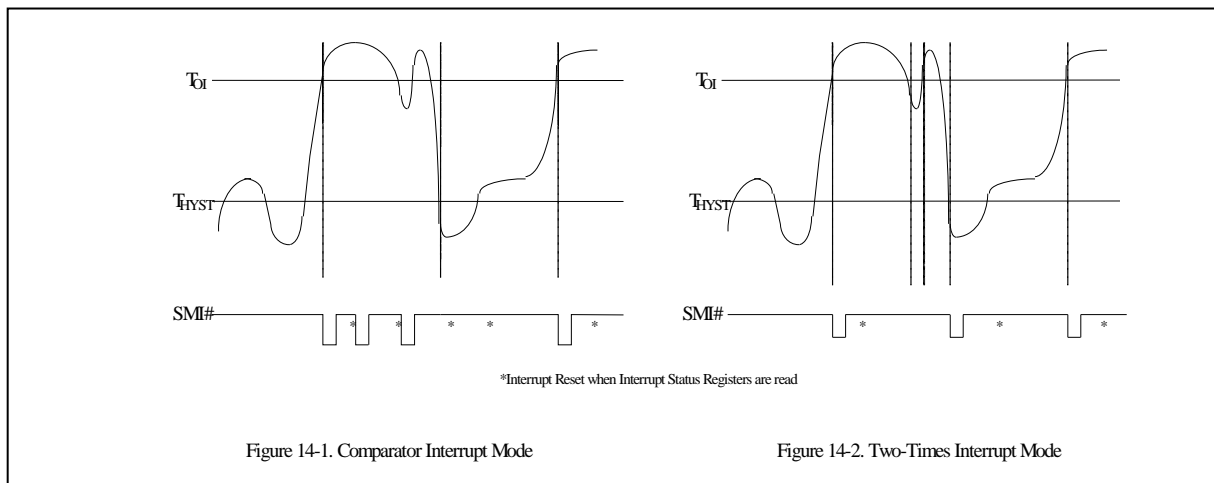
7.7.2 Voltage

INT# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 15-1)

7.7.3 Fan

INT# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit (set at value ram index 3Bh and 3Ch), will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 15-2)
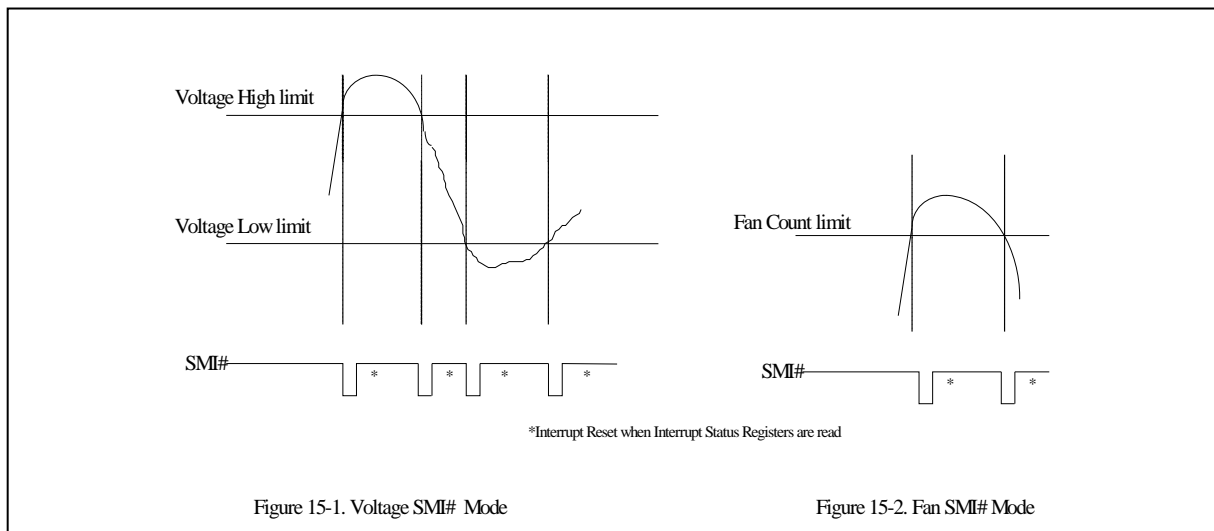
Figure 15-1. Voltage SMI# Mode   Figure 15-2. Fan SMI# Mode

8. CONTROL AND STATUS REGISTER

8.1 Configuration Register - Index 40h

Power on default [7:0] = 0000, 0001b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Software Reset	Read/Write	A one restores power on default value to all registers except the Serial Bus Address register. This bit is itself clear when it is set.
6-5	Reserved	Read/Write	Reserved
4	SOFT_PWDN	Read/Write	**Software Power Down.** Set to 1 to power down this chip, but I^{2}C interface is still working.
3	Reserved	Read/Write	Reserved
2	Reserved	Read/Write	Reserved
1	INT# Main Mask	Read/Write	A one disables the INT# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
0	START	Read/Write	A one enables startup of monitoring operations; a zero puts the part in standby mode. *Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.*

8.2 INT# Status Register 1 - Index 41h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read Only	Reserved
6	TEMP1_STS	Read Only	A one indicates a High or Low limit has been exceeded from temperature sensor 1 (VTIN1). This bit is cleared when this register is read.
5	TEMP0_STS	Read Only	A one indicates a High or Low limit has been exceeded from temperature sensor 0 (D+_D-). This bit is cleared when this register is read.
4-3	Reserved	Read Only	Reserved
2	VCC_STS	Read Only	A one indicates a High or Low limit has been exceeded. (VCC, +3.3V) This bit is cleared when this register is read.
1	VRAM_STS	Read Only	A one indicates a High or Low limit has been exceeded. (VRAM) This bit is cleared when this register is read.
0	VCORE_STS	Read Only	A one indicates a High or Low limit has been exceeded. (VCORE) This bit is cleared when this register is read.

8.3 INT# Status Register 2 - Index 42h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-2	Reserved	Read Only	Reserved.
1	FAN2_STS	Read Only	**A one indicates the fan count limit has been exceeded. This bit is cleared when this register is read.**
0	FAN1_STS	Read Only	**A one indicates the fan count limit has been exceeded. This bit is cleared when this register is read.**

8.4   INT# Mask Register 1 - Index 43h

Power on default <7:0> = **11**0**1**, **111**0 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/Write	Reserved
6	MSK_T1_INT	Read/Write	A one disables the corresponding interrupt status bit for SMI# interrupt. (Temperature 1)
5	MSK_T0_INT	Read/Write	A one disables the corresponding interrupt status bit for SMI# interrupt. (Temperature 0)
4-3	Reserved	Read/Write	Reserved
2	MSK_VCC_INT	Read/Write	A one disables the corresponding interrupt status bit for SMI# interrupt. (VCC, +3.3V)
1	MSK_VRAM_INT	Read/Write	A one disables the corresponding interrupt status bit for SMI# interrupt. (VRAM)
0	MSK_VCORE_INT	Read/Write	A one disables the corresponding interrupt status bit for SMI# interrupt. (VCORE)

8.5   INT# Mask Register 2 - Index 44h

Power on default <7:0> = 1111, 11**1**0 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-2	Reserved	Read/Write	Reserved.
1	MSK_FAN2_INT	Read/Write	**A one disables the corresponding interrupt status bit for SMI# interrupt. (Fan 2 speed counter)**
0	MSK_FAN1_INT	Read/Write	**A one disables the corresponding interrupt status bit for SMI# interrupt. (Fan 1 speed counter)**

8.6   Register - Index 45h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	Reserved	Read/write	Reserved.

8.7   Register - Index 46h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	Reserved	Read/write	Reserved

8.8   GPIO/GPO Function Enable Control Register - Index 47h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	EN_GPIO2	Read/Write	**Pin 2 Function Select.** <0> - Function of Pin 2 is TEMP_FAULT#. <1> - Function of Pin 2 is GPIO2.
6	EN_GPIO1	Read/Write	**Pin 1 Function Select.** <0> - Function of Pin 1 is FAN_FAULT#. <1> - Function of Pin 1 is GPIO1.
5	EN_GPIO7	Read/Write	**Pin 20 Function Select.** <0> - Function of Pin 20 is VOLTAGE_FAULT#. <1> - Function of Pin 20 is GPIO7.
4-3	Reserved	Read/Write	Reserved
2	EN_GPIO6	Read/Write	**Pin 18 Function Select.** <0> - Function of Pin 18 is PWM/DC_OUT2. <1> - Function of Pin 18 is GPIO6.
1	EN_GPIO5	Read/Write	**Pin 9 Function Select.** <0> - Function of Pin 9 is FANIN2. <1> - Function of Pin 9 is GPIO5.
0	EN_GPO3 &4	Read/Write	**Enable GPO3 & GPO4 Function of Pin 6 & Pin7.** **<0> - Functions of GPO3 & GPO4 are disabled.** **<1> - Functions of GPO3 & GPO4 are enabling.**

8.9   Register - Index 48h

Reserved

8.10 GPIO1-2 & 5-7 I/O Mode Control Register - Index 49h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/write	Reserved.
6	GPIO2_MODE	Read/Write	**GPIO2 I/O Mode Select.** (Only for GPIO function of Pin 2 is enabled.) <0> - GPIO2 is an input port. <1> - GPIO2 is an output port.
5	GPIO1_MODE	Read/Write	**GPIO1 I/O Mode Select.** (Only for GPIO function of Pin 1 is enabled.) <0> - GPIO1 is an input port. <1> - GPIO1 is an output port.
4	GPIO7_MODE	Read/Write	**GPIO7 I/O Mode Select.** (Only for GPIO function of Pin 20 is enabled.) <0> - GPIO7 is an input port. <1> - GPIO7 is an output port.
3-2	Reserved	Read/Write	Reserved
1	GPIO6_MODE	Read/Write	**GPIO6 I/O Mode Select.** (Only for GPIO function of Pin 18 is enabled.) <0> - GPIO6 is an input port. <1> - GPIO6 is an output port.
0	GPIO5_MODE	Read/Write	**GPIO5 I/O Mode Select.** (Only for GPIO function of Pin 9 is enabled.) <0> - GPIO5 is an input port. <1> - GPIO5 is an output port.

8.11 GPO3-4 Output Data Register - Index 4Ah

Power on default [7:0] = 000P, PPPP b (P: power on trapping)

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/write	Reserved.
6	GPO4_VAL	Read/Write	*GPO4 Value. Set the output value of GPO4 pin.*
5	GPO3_VAL	Read/Write	*GPO3 Value. Set the output value of GPO3 pin.*
4-0	Reserved	Read/Write	Reserved

8.12 GPIO1-2 & 5-7 Data Register - Index 4Bh

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/write	Reserved.
6	GPIO2_VAL	Read/Write	**GPIO2 Value.** Set the output value of GPIO2 pin. Reading this bit will return the value of pin 2.
5	GPIO1_VAL	Read/Write	**GPIO1 Value.** Set the output value of GPIO1 pin. Reading this bit will return the value of pin 1.
4	GPIO7_VAL	Read/Write	**GPIO7 Value.** Set the output value of GPIO7 pin. Reading this bit will return the value of pin 20.
3-2	Reserved	Read/Write	Reserved
1	GPIO6_VAL	Read/Write	**GPIO6 Value.** Set the output value of GPIO6 pin. Reading this bit will return the value of pin 18.
0	GPIO5_VAL	Read/Write	**GPIO5 Value.** Set the output value of GPIO5 pin. Reading this bit will return the value of pin 9.

8.13 Nuvoton Vendor ID (Low Byte) - Index 4Ch

Power-on default [7:0] = 1010, 0011 b (0xA3h)

BIT	NAME	READ/WRITE	DESCRIPTION
7:0	VIDL[7:0]	Read Only	Vendor ID Low Byte. Default A3h.

8.14 Nuvoton Vendor ID (High Byte) - Index 4Dh

Power-on default [7:0] = 0101, 1100 b (0x5Ch)

BIT	NAME	READ/WRITE	DESCRIPTION
7:0	VIDH[7:0]	Read Only	**Vendor ID High Byte.** Default 5Ch

8.15 Chip ID - Index 4Eh

Power on default [7:0] = **1000, 0000** b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	CHIPID[7:0]	Read Only	**Nuvoton Chip ID number.** Read this register will return *0x80h* for W83L786NR/NG.

8.16 Register - Index 4Fh

Reserved

8.17 Register - Index 50h

Reserved

8.18 GPIO1-2 & 5-7 Output Mode Control Register - Index 51h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/write	Reserved.
6	GPIO2_OB	Read/write	Enable GPIO2 as Output Buffer. Set to <1> GPIO2 can drive logical high or logical low. <0> GPIO2 is open-drain.
5	GPIO1_OB	Read/write	Enable GPIO1 as Output Buffer. Set to <1> GPIO1 can drive logical high or logical low. <0> GPIO1 is open-drain.
4	GPIO7_OB	Read/write	Enable GPIO7 as Output Buffer. Set to <1> GPIO7 can drive logical high or logical low. <0> GPIO7 is open-drain.
3-2	Reserved	Read/write	Reserved
1	GPIO6_OB	Read/write	Enable GPI6 as Output Buffer. Set to <1> GPIO6 can drive logical high or logical low. <0> GPIO6 is open-drain.
0	GPIO5_OB	Read/write	Enable GPIO5 as Output Buffer. Set to <1> GPIO5 can drive logical high or logical low. <0>GPIO5 is open-drain.

8.19 INT# Property Select - Index 52h

Power on - <7:0> --0000, 0100 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3-2	TEMP_INT_MD [1:0]	Read/Write	**Temperature INT Mode Select.** **<00>** - **Comparator Interrupt Mode:** Temperature 1/2 exceeds T_O (Over-temperature) limit causes an interrupt. Reading the Interrupt Status will reset this interrupt. **<01>** - **Two Time Interrupt Mode:**(Default) This bit use in temperature sensor 1/2 interrupt mode with hysteresis and T_O type. Temperature exceeding T_O, causes an interrupt and then temperature going below T_{HYST} will also cause another interrupt if the previous interrupt has been reset by reading the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}. **<10>** - **One Time Interrupt Mode:** This bit use in temperature sensor 1/2 interrupt mode with hysteresis type. Temperature exceeding T_O (Over-temperature) causes an interrupt and then temperature going below T_{HYST} (Hysteresis temperature) will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, and interrupt will not occur again until the temperature exceeding T_O.
1	EN_INT#	Read/Write	**Enable INT# Output.** A one enables the INT# Interrupt output.
0	Reserved	Read/Write	Reserved.

8.20 Thermal Sensor 1/2 Type Register - Index 53h

Power on default [7:0] = 0100, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-2	Reserved	Read/Write	Reserved.
1	T1_TYPE	Read/Write	Temperature sensor 1 type. <0> - Thermistor (10K @ 25 degree C, B=3435). <1> - thermal diode.
0	T0_TYPE	Read/Write	Temperature sensor 0 (GPU) type. <0> - Thermistor (10K @ 25 degree C, B=3435) <1> - thermal diode.

8.21 Fan Divisor Register - Index 54h

Power on default [7:0] = 0001, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/write	Reserved.
6-4	FAN2_DIV_SEL[2:0]	Read/Write	**FAN2 Divisor Select.** <000> - divide by 1; <001> - divide by 2; <010> - divide by 4; <011> - divide by 8. <100> - divide by 16. <101> - divide by 32. <110> - divide by 64. <111> - divide by 128.
3	Reserved	Read/write	Reserved.
2-0	FAN1_DIV_SEL[2:0]	Read/Write	**FAN1 Divisor Select.** <000> - divide by 1; <001> - divide by 2; <010> - divide by 4; <011> - divide by 8. <100> - divide by 16. <101> - divide by 32. <110> - divide by 64. <111> - divide by 128.

8.22 Reserved - Index 55h ~ 5Fh

Reserved

8.23 FAN Configuration Register - Index 80h

Power on default [7:0] = 00**11**, **11**00 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	EN_PWM2	Read/Write	FAN2 Control Mode <1> - PWM FAN Control Mode <0> - DC FAN Control Mode
6	EN_PWM1	Read/Write	FAN1 Control Mode <1> - PWM FAN Control Mode <0> - DC FAN Control Mode
5-4	FAN2_MODE	Read/Write	FAN2 Control Mode. <00> - Manual Control Mode. (Default) <01> - Thermal Cruise mode. <10> - SMART FAN^{TM} II Mode. <11> - FAN_SET.
3-2	FAN1_MODE	Read/Write	FAN 1 Control Mode. <00> - Manual Control Mode. (Default) <01> - Thermal Cruise mode. <10> - SMART FAN^{TM} II Mode. <11> - FAN_SET.
1-0	**Reserved**	**Read/Write**	**Reserved.**

8.24 DC FAN1 Output Voltage Level Control Register (Manual Mode) / FAN1 Output Voltage Table (SMART FAN^{TM} II Mode) – Index 81h

Power on default [7:0] **1111**, 1111 b

For **Manual Mode**

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3-0	FAN1_DC [3:0]	Read/Write	DC FAN1 Output Level. Only for Thermal Manual Mode while CR80h bit3-2 is 00. This 3-bit register determines the DC FAN driving voltage. <0x0h> - DC output is 0V. <0xFh> - DC output is 3.3V. <0xXh> - DC output levels are from 0V to 3.3v and they are separated into 16 levels equally.

For **SMART FAN**[TM] **II Mode**

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	FAN1_TAB2[3:0]	Read/Write	FAN1 Output Level 2 for SMART FAN[TM] II Mode.
3-0	FAN1_TAB1[3:0]	Read/Write	FAN1 Output Level 1 for SMART FAN[TM] II Mode.

8.25 FAN1 Output Voltage Table (SMART FANTM II Mode) - Index 82h

Power on default [7:0] **1111**, 1111 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	FAN1_TAB4[3:0]	Read/Write	FAN1 Output Level 4 for SMART FAN[TM] II Mode.
3-0	FAN1_TAB3[3:0]	Read/Write	FAN1 Output Level 3 for SMART FAN[TM] II Mode.

8.26 TEMP0 (D+_D-) Target Temperature Register (Thermal Cruise Mode) / TEMP_POINT1 for FAN1 (SMART FAN[TM] II Mode) - Index 83h

Power on default [7:0] = 0000, 0000 b

TEMP1 target temperature register for **Thermal Cruise mode**.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	TEMP_TAR_T0[**7**:0]	Read/Write	**TEMP0 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit3-2 is 01.

TEMP_**POINT1** register for **Smart FAN II Mode**.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	TEMP_**P**1F1[**7**:0]	Read/Write	**TEMP_POINT1 for FAN1 use Smart FAN II Mode.**

8.27 TEMP_POINT2 for FAN1 (SMART FANTM II Mode) - Index 84h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	**TEMP_P2F1[7:0]**	**Read/Write**	**TEMP_POINT2 for FAN1 use SMART FAN[TM] II Mode.**

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8.28 FAN 1 Speed Low Limit Rate Control Register (Thermal Cruise Mode) / TEMP_POINT3 for FAN1 (SMART FANTM II Mode) - Index 85h

Power on default [7:0] = *0000, 0000* b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3-0	FAN1_LL [3:0]	Read/Write	Low Limit Speed of FAN1. Only for **Thermal Cruise mode**.

TEMP_**POINT**3 register for **Smart FAN II Mode**.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	TEMP_*P*3F1[*7*:0]	Read/Write	**TEMP_*POINT*3 for FAN1 use SMART FANTM II Mode.**

8.29 TEMP_POINT4 for FAN1 (SMART FANTM II Mode) - Index 86h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	**TEMP_P4F1[7:0]**	Read/Write	**TEMP_POINT4 for FAN1 use SMART FANTM II Mode.**

8.30 DC FAN2 Output Voltage Level Control Register (Manual Mode)/ FAN2 Output Voltage Table (SMART FANTM II Mode) - 87h

Power on default [7:0] **1111**, 1111 b

For **Manual Mode**

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3-0	FAN2_DC [3:0]	Read/Write	DC FAN2 Output Level. Only for Thermal Manual Mode while CR80h bit5-4 is 00. This 3-bit register determines the DC FAN driving voltage. <0x0h> - DC output is 0V. <0xFh> - DC output is 3.3V. <0xXh> - DC output levels are from 0V to 3.3v and they are separated into 16 levels equally.

For **SMART FAN^{TM} II Mode**

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	FAN2_TAB2[3:0]	Read/Write	FAN2 Output Level 2 for SMART FAN^{TM} II Mode.
3-0	FAN2_TAB1[3:0]	Read/Write	FAN2 Output Level 1 for SMART FAN^{TM} II Mode.

8.31 FAN2 Output Voltage Table (SMART FANTM II Mode) - Index 88h

Power on default [7:0] **1111,** 1111 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	FAN2_TAB4[3:0]	Read/Write	FAN2 Output Level 4 for SMART FAN^{TM} II Mode.
3-0	FAN2_TAB3[3:0]	Read/Write	FAN2 Output Level 3 for SMART FAN^{TM} II Mode.

8.32 TEMP1 (VTIN1) Target Temperature Register (Thermal Cruise Mode) / TEMP_POINT1 for FAN2 (SMART FAN^{TM} II Mode) - Index 89h

Power on - [7:0] = 0000, 0000 b

TEMP2 target temperature register for **Thermal Cruise mode**.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	TEMP_TAR_T1[**7**:0]	Read/Write	**TEMP1 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit5-4 is 01.

TEMP_POINT1 register for **SMART FAN^{TM} II Mode**.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	TEMP_**P**1F2[**7**:0]	Read/Write	**TEMP_POINT1 for FAN2 use SMART FAN^{TM} II Mode.**

8.33 TEMP_POINT2 for FAN2 (SMART FANTM II Mode) - Index 8Ah

Power on - [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	**TEMP_P2F2[7:0]**	**Read/Write**	**TEMP_POINT2 for FAN2 use SMART FAN^{TM} II Mode.**

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8.34 FAN 2 Speed Low Limit Rate Control Register/ TEMP_POINT3 for FAN2 SMART FAN™ II Mode) - Index 8Bh

Power on default [7:0] =*0000, 0000* b

BIT	NAME	READ/WRITE	DESCRIPTION
7-5	Reserved	Read/Write	Reserved.
4-1	FAN2_LL [3:0]	Read/Write	Low Limit Speed of FAN2. Only for **Thermal Cruise mode**.

TEMP_**POINT3** register for **SMART FAN™ II Mode**.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	TEMP_**P**3F2[**7**:0]	Read/Write	**TEMP_POINT3 for FAN2 use SMART FAN™ II Mode.**

8.35 TEMP_POINT4 for FAN2 (SMART FANTM II Mode) - Index 8Ch

Power on default [7:0] = 0000, 0000 b.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	**TEMP_P4F2[7:0]**	Read/Write	**TEMP_POINT4 for FAN2 use SMART FAN™ II Mode.**

8.36 Tolerance of Temperature Register - Index 8Dh

Power on default [7:0] = **0011, 0011** b

For Thermal Cruise mode

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	TOL_T1[3:0]	Read/Write	**Tolerance of Fan 2 Target Temperatures (Temp1).** Only for Thermal Cruise mode.
3-0	TOL_T0[3:0]	Read/Write	**Tolerance of Fan 1 Target Temperature (Temp0).** Only for Thermal Cruise mode.

For Smart FAN II Mode

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	TOL_T1[3:0]	Read/Write	**Tolerance of Fan 2 Temperatures (Temp1).** Only for SMART FAN™ II Mode.
3-0	TOL_T0[3:0]	Read/Write	**Tolerance of Fan 1 Temperature (Temp0).** Only for SMART FAN™ II Mode.

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8.37 FAN 2D/3D state Control Register - Index 8Eh

At SMART FAN^{TM} II Mode, FAN will be controlled by 2D/3D mode after writing **2Dh/3Dh** to CR8A

8.38 FAN Pre-Scale Register - Index 8Fh
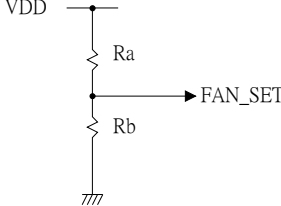
Power on default [7:0] = 0010, 0010 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	*PWM2_CLK_SEL*	*Read/Write*	*PWM Input Clock Select of Fan 2. This bit select FAN input clock to pre-scale divider.* *<0> - 1.44MHz* *<1> - 180KHz*
6-4	*PWM2_CLK_DIV [2:0]*	*Read/Write*	*FAN 2 PWM Input Clock divider.* *<000> - divider is 1* *<001> - divider is 2* *<010> - divider is 4* *<011> - divider is 8* *<100> - divider is 16* *<101> - divider is 32* *<110> - divider is 64* *<111> - divider is 128*
3	*PWM1_CLK_SEL*	*Read/Write*	*PWM Input Clock Select of Fan 1. This bit select FAN input clock to pre-scale divider.* *<0h> - 1.44MHz* *<1h> - 180KHz*
2-0	*PWM1_CLK_DIV [2:0]*	*Read/Write*	*FAN 1 PWM Input Clock divider.* *<000> - divider is 1* *<001> - divider is 2* *<010> - divider is 4* *<011> - divider is 8* *<100> - divider is 16* *<101> - divider is 32* *<110> - divider is 64* *<111> - divider is 128*

8.39 FAN Initial Output Value – Index90h

Power on trapping

BIT	NAME	READ/WRITE	DESCRIPTION
7	**FAN_3DST**	**Read**	***A one indicates FAN is working at 3D mode (for SMART FAN™ II Mode).*** ***It can be programmed directly by I²C.***
6-4	Reserved	Read/Write	Reserved.
3-0	FANINI [3:0]	Read/Write	**FAN Initial Speed.** Use two resistors to divide a four section to represent different initial FAN Speed. The table is shown as following.

Section	FAN Speed rate	Ra	Rb
3	100%	9.1K	×
2	81%	4.7K	9.1K
1	62%	9.1K	4.7K
0	43%	×	9.1K

8.40 Fan Step down Time Register - Index 91h

Power on default [7:0] = **0001, 0100** b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STEP_DOWN_T[7:0]	Read/Write	The time interval, which is 1-second unit, to decrease DC output level in SMART FAN™ II Control mode.

8.41 Fan Step up Time Register - Index 92h

Power on default [7:0] = 0000, 1010 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STEP_UP_T[7:0]	Read/Write	The time interval, which is 1-second unit, to increase DC output level in SMART FAN™ II Control mode.

8.42 Temperature Sensor 0 (D+_D-) Offset Register - Index 93h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	OFFSET0[7:0]	Read/Write	Temperature 0 base temperature. The real temperature is sum of both monitor value and offset value. 0111,1111 => +127/4 degree C 0111,1110 => +126/4 degree C 　　　　　: 0000,0001 => +1/4 degree C 0000,0000 => +0 degree C 1111,1111 => -1/4 degree C 1111,1110 => -2/4 degree C 　　　　　: 1000,0000 => -128/4 degree

8.43 Temperature Sensor 1 (VTIN1) Offset Register – Index 94h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	OFFSET1[7:0]	Read/Write	Temperature 1 base temperatures. The real temperature is sum of both monitor value and offset value. 0111,1111 => +127/4 degree C 0111,1110 => +126/4 degree C 　　　　　: 0000,0001 => +1/4 degree C 0000,0000 => +0 degree C 1111,1111 => -1/4 degree C 1111,1110 => -2/4 degree C 　　　　　: 1000,0000 => -128/4 degree

8.44 Register - Index 95h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	Reserved	Read/Write	

8.45 Register - Index 96h

Power-on default [7:0] = 0001, 1001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	Reserved	Read/Write	

8.46 Register - Index 97h

Power-on default [7:0] = 0001, 1001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	Reserved	Read/Write	

Value RAM and Limit Value

8.47 Value RAM - Index 20h- 3Fh or 60h - 7Fh

INDEX A7-A0	DESCRIPTION	UNIT
20h	VCORE reading	
21h	VRAM reading	
22h	VCC reading	
23h	Reserved	
24h	Reserved	
25h	Temperature 0 reading (D+_D-, 0 ~ 255)	°C
26h	Temperature 1 reading (VTIN1, 0 ~ 255)	°C
27h	Reserved	
28h	FANIN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.	Count
29h	FANIN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.	Count
2Ah	Reserved	
2Bh	VCORE High Limit. (0xff)	
2Ch	VCORE Low Limit. (0x00)	
2Dh	VRAM High Limit. (0xff)	
2Eh	VRAM Low Limit. (0x00)	
2Fh	VCC High Limit. (0xff)	

Value RAM - Index 20h- 3Fh or 60h - 7Fh, continued.

INDEX A7-A0	DESCRIPTION	UNIT
30h	**VCC Low Limit. (0x00)**	
31h	Reserved	
32h	Reserved	
33h	Reserved	
34h	Reserved	
35h	Over Temperature 0 Limit (High). (0x50)	°C
36h	Temperature 0 Hysteresis Limit (Low). (0x4b)	°C
37h	Over Temperature 1 Limit (High). (0x50)	°C
38h	Temperature 1 Hysteresis Limit (Low). (0x4b)	°C
39h	Reserved	°C
3Ah	Reserved	°C
3Bh	FAN1 Fan Count Limit. (0xff) **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.	Count
3Ch	FAN2 Fan Count Limit. (0xff) **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.	Count
3Dh	*FAN1 Speed Control Output Level*	
3Eh	*FAN2 Speed Control Output Level*	
3Fh	Reserved	

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9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{CC}+0.5	V
Operating Temperature	0 to +70	$^\circ$ C
Storage Temperature	-55 to +150	$^\circ$ C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 DC Characteristics

(Ta = 0° C to 70° C, V_{DD} = 5V $\pm$ 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O$_{12t}$ - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O$_{12ts}$ - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT$_{12t}$ - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V$_{OL}$			0.4	V	I$_{OL}$ = 12 mA
Output High Voltage	V$_{OH}$	2.4			V	I$_{OH}$ = -12 mA
OD$_8$ - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V$_{OL}$			0.4	V	I$_{OL}$ = 8 mA
OD$_{12}$ - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V$_{OL}$			0.4	V	I$_{OL}$ = 12 mA
OD$_{48}$ - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V$_{OL}$			0.4	V	I$_{OL}$ = 48 mA
IN$_t$ - TTL level input pin						
Input Low Voltage	V$_{IL}$			0.8	V	
Input High Voltage	V$_{IH}$	2.0			V	
Input High Leakage	I$_{LIH}$			+10	μA	V$_{IN}$ = V$_{DD}$
Input Low Leakage	I$_{LIL}$			-10	μA	V$_{IN}$ = 0 V
IN$_{ts}$ - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V$_{t-}$	0.5	0.8	1.1	V	V$_{DD}$ = 5 V
Input High Threshold Voltage	V$_{t+}$	1.6	2.0	2.4	V	V$_{DD}$ = 5 V
Hysteresis	V$_{TH}$	0.5	1.2		V	V$_{DD}$ = 5 V
Input High Leakage	I$_{LIH}$			+10	μA	V$_{IN}$ = V$_{DD}$
Input Low Leakage	I$_{LIL}$			-10	μA	V$_{IN}$ = 0 V

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9.3   AC Characteristics

9.3.1   Serial Bus Timing Diagram

Serial Bus Timing Diagram
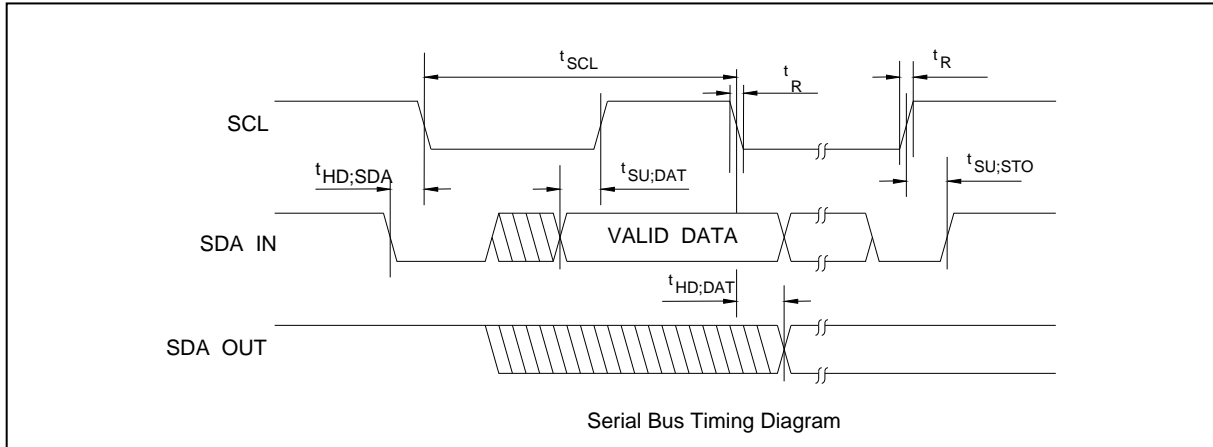
Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t$_{SCL}$	10		uS
Start condition hold time	t$_{HD;SDA}$	4.7		uS
Stop condition setup-up time	t$_{SU;STO}$	4.7		uS
DATA to SCL setup time	t$_{SU;DAT}$	120		nS
DATA to SCL hold time	t$_{HD;DAT}$	5		nS
SCL and SDA rise time	t$_R$		1.0	uS
SCL and SDA fall time	t$_F$		300	nS

9.3.2   VID Input Skew
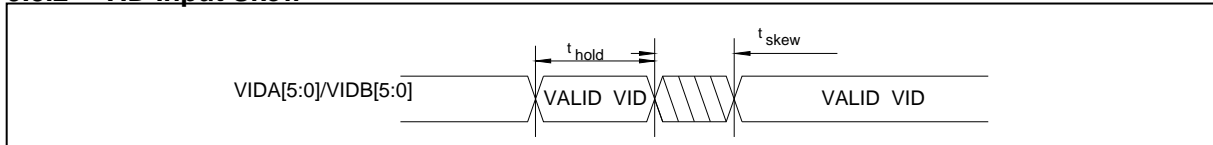
VID Input Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
VID Input Unstable Time	t$_{Skew}$		0.8	uS
VID Valid Input Hold Time	t$_{hold}$	4		uS

10. THE TOP MARKING

The top marking of W83L786NR

W83L786NR
2826978Y-61
443OB

Left: Nuvoton logo
1st line: part number: W83L786NR
2nd line: Tracking code 2 826978Y-61
3rd line: Tracking code   443 O B

    443: packages made in '04, week 43
    O: assembly house ID; A means ASE, S means SPIL, O means OSE
    B: IC revision

The top marking of W83L786NG

W83L786NG
2826978Y-61
443OB

Left: Nuvoton logo
1st line: part number: W83L786NG, G means Pb-free package
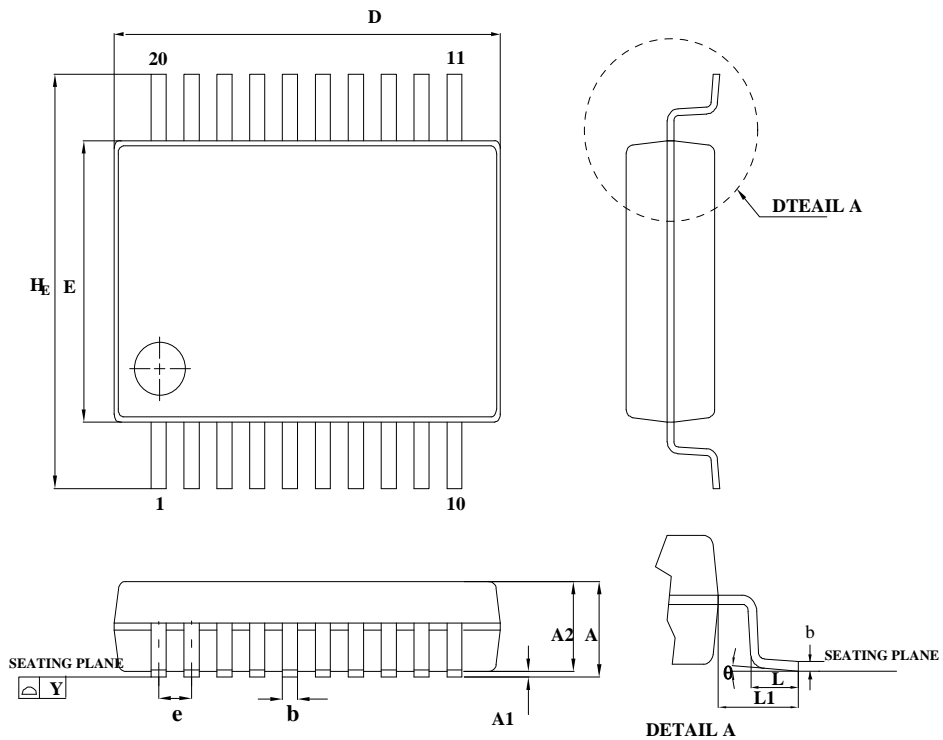2nd line: Tracking code 2 826978Y-61
3rd line: Tracking code   443 O B

    443: packages made in '04, week 43
    O: assembly house ID; A means ASE, S means SPIL, O means OSE
    B: IC revision

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11. PACKAGE SPECIFICATION

■ 20L SSOP-209 mil

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

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