MCF52235 Chip Errata

Silicon Revision: All

This document identifies implementation differences between the MCF5223*x* processors and the description contained in the *MCF52235 ColdFire® Reference Manual*. Refer to http://www.freescale.com/coldfire for the latest updates.

The latest version of the MCF5223x family is revision A or mask 3M23E.

Table 1. Summary of MCF5223x Errata

Errata	Module Affected	Date Errata Added	Revision Affected?		
			MCF5223x		MCF5223xA
			2M23E	3M23E	
SECF025	EPHY	4/29/05	Yes	No	No
SECF015	Flash	11/17/06	Yes	No	No
SECF020	ADC	4/17/07	Yes	No	No
SECF018	ADC	3/28/08	Yes	Yes	Yes
SECF019	ADC	3/28/08	Yes	Yes	Yes
SECF006	FEC	5/31/07	Yes	Yes	Yes
SECF014	BDM	3/20/08	Yes	Yes	Yes
SECF127	Clock	2/4/09	Yes	No	No
SECF010	FEC	2/4/09	Yes	Yes	Yes
SECF128	EPHY	2/4/09	Yes	Yes	Yes
SECF195	OSC	04/05/11	Yes	Yes	Yes

The table below provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Date	Substantive Changes
0	6/2006	Initial release
1	11/2006	Reformatted document. Added SECF015 Updated Table 1
2	4/2007	Added SECF020 and updated Table 1.
3	5/2007	Added SECF006 and updated Table 1.
4	3/2008	Added SECF018, SECF019, SECF014
5	2/2009	Added Status section to SECF025 and SECF015 stating that these errata will be fixed. Added SECF127, SECF010, SECF128
6	5/2009	Added new 'A' suffix device revision to Table 1. Changed Status section in SECF025, SECF015, SECF020, and SECF127 from "This errata will be fixed." to "This erratum is fixed in devices labeled with the A suffix."
7	10/2009	Added 3M23E mask to Table 1 and to the same errata's fix plans as revision A devices.
8	04/2011	Added SECF195
9	02/2015	Updated SECF015

SECF025: EPHY Not Accepting Valid LTP Greater Than 100 ns

Errata type: Silicon
Affects: EPHY
Description: If a link partner's LTP is greater than 100 ns, using auto-negotiation, the EPHY does not recognize it. This results in a failure to auto-negotiate.

Workaround: Disable auto-negotiation and configure the EPHY or link partner to operate in 100TX or 10BaseT mode.

Software implementation is available in the ColdFire_Lite stack, which is available at http://www.freescale.com/coldfire.

Fix plan: This erratum is fixed in devices labeled with the A suffix or 3M23E mask.

SECF015: Internal Flash Speculation Address Qualification Incomplete

Errata type: Silicon
Affects: Flash controller

Description: The flash controller uses a variety of advanced techniques, including two-way 32-bit bank interleaving, address speculation, and pipelining to improve performance. An issue involving a complex series of interactions between the local flash controller and other memory accesses (internal SRAM, EIM, or SDRAM) has been uncovered. In rare instances, the interaction between a non-flash memory access and a flash access can result in incorrect data usage for a read operation. This may produce unexpected exceptions, incorrect execution, or silent data corruption.

The problem requires two accesses where the modulo (flash size) address and address mask configuration are the same for both a flash access and a non-flash access that occur close in time.

Workaround: **Workaround Step 1 (Always do this)**: Use FLASHBAR[6] to disable the address speculation mechanisms of the flash controller. The default configuration (FLASHBAR[6] = 0) enables the address speculation. If FLASHBAR[6] equals 1, address speculation is disabled. Core performance may be degraded from 4% – 9%, depending heavily on application code.

NOTE

FLASHBAR[6] is user accessible via the movec instruction. FLASHBAR[6] always reads back as 0.

NOTE

On MCF528x and MCF521x devices FLASHBAR[6] is already set to 1 for datecodes XXX0327 and later. The bit still reads back as 0.

Workaround Step 2a (Select one of the step 2 options to use): Construct the device memory map so the flash and SRAM spaces are disjoint within the modulo-(flash_size) addresses. In some cases if this approach is selected, the upper portion of the flash memory might be unused and the SRAM be mapped to this unused flash space.

Consider an example where the flash memory size is 256 Kbytes and the on-chip SRAM size is 32 Kbytes. If 224 Kbytes or less of flash are used, the SRAM can be based at the upper 32 Kbytes (within the modulo-256 Kbyte address) of the flash address space:

```
Flash: size = 0x40000, base = 0x0000_0000
RAM: size = 0x08000, base = 0x8003_8000 = RAM_BASE+(256-32) Kbytes
```

where the flash and SRAM base addresses are unique BA[31:16].

In summary, this approach can be applied if the combined size of the used flash and used SRAM is less than the total flash size, with the flash contents justified to the lower address range and the SRAM contents justified to the upper address range.

Workaround Step 2b (Select one of the step 2 options to use): Separate the contents of the SRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR and RAMBAR to restrict accesses. For example, if the flash contains only instructions and the SRAM contains only operands (all data), the appropriate address space mask fields are specified to prevent flash and SRAM accesses from overlapping.

Workaround Step 3a (Select one of the step 3 options to use if external parallel memory is used in the system): Do not enable caching of external memories. With caching disabled the timing requirements for an issue to occur will not be met, so this will prevent conflicts between flash and external parallel memory accesses through the EIM or SDRAMC.

Workaround Step 3b (Select one of the step 3 options to use if external parallel memory is used in the system): Separate the contents of the EIM and/or SDRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR,

CSMRn, and DMRn to restrict accesses. For example, if the flash contains only instructions and the SDRAM contains only operands (all data), the appropriate address space mask fields are specified to prevent flash and SRAM accesses from overlapping.

Fix plan: This erratum is fixed in devices labeled with the A suffix or 3M23E mask.

SECF020: ADC May Drop Conversions If Powered Down for Extended Periods of Time at High Temperature

Errata type: Silicon
Affects: ADC
Description: If the ADC is powered down for an extended amount of time (e.g. days) at continuously high temperature (>70°C) and then powered back up, the ADC result may randomly drop to 0 or jump to 4095 (2^{12}-1). Periodic powering down does not exhibit a problem; however, extended periods in a continuous powered down state may result in invalid conversions. Also, shutting the power off to the entire device for an extended amount of time does not cause a problem. The issue has only been observed when the device is powered up while the ADC is powered off (in software).

Workaround: If the device operates at temperatures higher than 70°C and the application requires the use of the ADC, keep the ADC powered up during normal operation. Do not power the ADC down, even if it is not in use at that time.

Powering the ADC up or down is controlled by bits PD0 and PD1 in the POWER register of the ADC.

Fix plan: This erratum is fixed in devices labeled with the A suffix or 3M23E mask.

SECF018: ADC Might Give Erroneous Results if V_{REFH} and V_{REFL} are Not at the Same Potential as V_{DDA} and V_{SSA} Respectively

Errata type: Silicon
Affects: ADC
Description: The ADC could produce an error if the ADC reference voltage VREFH is below the analog supply voltage VDDA, or if the ADC reference voltage VREFL is above analog ground VSSA by more than 50 mV. The error is that the ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

Workaround: Connect V_{REFH} directly to V_{DDA}. Similarly, connect V_{REFL} to V_{SSA}.

Fix plan: Currenty, there are no plans to fix this.

SECF019: ADC Might Give Erroneous Results if the ADC Reference Voltage (V_{REFH}) is Below 3.1 V

Errata type: Silicon
Affects: ADC
Description: If the ADC reference voltage V_{REFH} is less than 3.1 V, either of the following error conditions could result:

- Low analog input voltages to the ADC might not be measured properly. (for example, input voltages less than 100 mV might yield measurements equal to 0)
- The ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

Workaround: Ensure that V_{REFH} is at or above 3.1 V.

Fix plan: Currenty, there are no plans to fix this.

SECF006: FEC Duplicate Transmission

Errata type: Silicon
Affects: FEC
Description: In some cases, the FEC transmits single frames more than once. The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding Tx data continuously until the Tx FIFO is full. It does not determine whether the TxBD to be fetched is already being processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. To remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC fetches from memory a BD that has already been processed but not yet written back (it is read a second time with the R bit set). In this case, the data is fetched and transmitted again.

Workaround: Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for large or small frames, one of the following must be true:

- The FEC software driver ensures that there is always at least one TxBD with the Ready bit cleared.
- Every frame uses more than one TxBD and every TxBD, but the last is written back immediately after the data is fetched.

The FEC software driver ensures a minimum frame size, n. The minimum number of TxBDs is then rounded up to the nearest integer (though the result cannot be less than 3). The default Tx FIFO size is 192 Bytes; this size is programmable.

Fix plan: Currently, there are no plans to fix this.

SECF014: Level 2 Trigger Operation Controlled by TDR[31]

Errata type: Silicon
Affects: BDM
Description: The TDR[L2T] bit (TDR bit 15) has no effect on the level 2 trigger. Bit 31 of the TDR register provides both trigger response control and logical operation of the level 2 trigger.

Workaround: Use the TDR[31] bit to control the logical operation for the level 2 trigger as follows:

- 0 -- Level 2 trigger = PC_condition & Address_range & Data_condition
- 1 -- Level 2 trigger = PC_condition | (Address_range & Data_condition)

Since TDR[31] is also part of the trigger response control, only certain combinations of trigger responses and logical operations are available as shown below:

Table 3. TDR[31:30] Definitions

TDR[31:30]	Level 2 Trigger	Trigger Response
00	PC_cond & (Add_range & Data_cond)	Display on DDATA
01		Processor halt
10	PC_cond | (Add_range & Data_cond)	Debug interrupt
11		Reserved

Fix plan: Currently, there are no plans to fix this.

SECF127: Clock control high register (CCHR) not writable

Errata type: Silicon
Affects: Clock
Description: Writes to the clock control high register have no effect, even though reading this register shows it has been updated.

Workaround: There is no known workaround.

Fix plan: This erratum is fixed in devices labeled with the A suffix or 3M23E mask.

SECF010: FEC Interrupts will not Trigger on Consecutive Transmit Frames

Errata type: Silicon
Affects: FEC
Description: The late collision (LC), retry limit (RL), and underrun (UN) interrupts do not trigger on consecutive transmit frames. For example, if back-to-back frames cause a transmit underrun, only the first frame generates an underrun interrupt. No other underrun interrupts are generated until a frame is transmitted that does not underrun or the FEC is reset.

Workaround: Because late collision, retry limit, and underrun errors are not directly correlated to a specific transmit frame, in most cases a workaround for this problem is not needed. If a workaround is required, there are two independent workarounds:

- Ensure that a correct frame is transmitted after a late collision, retry limit, or underrun errors are detected.
- Perform a soft reset of the FEC by setting ECR[RESET] when a late collision, retry limit, or underrun errors are detected.

Fix plan: Currently, there are no plans to fix this.

SECF128: EPHY Incorrectly Advertises It Can Receive Next Pages

Errata type: Silicon
Affects: Ethernet PHY

Description: The EPHY from reset incorrectly advertises that it can receive next pages from the link partner. These next pages are most often used to send gigabit Ethernet ability information between link partners. This device is 10/100 Mbit only, so there is no need to advertise this capability. In fact if advertised this additional pages of information must be handled in a special manor not typical of 10/100 Ethernet drivers.

Workaround: The NXTP bit in the auto-negotiate (A/N) advertisement register (4.15) should be cleared as soon as possible after reset; ideally before enabling auto-negotiation.

Fix plan: Currently, there are no plans to fix this.

SECF195: OSC: Limited input voltage range on EXTAL pin.

Errata type: Silicon
Affects: Oscillator
Description: The input circuit of the EXTAL pin should be limited to 3.0 V. Failure to keep the voltage below 3.0V may lead to a decrease in lifespan of the device.

Workaround: It is recommended that the following action be taken to avoid problems:

- Ensure that the maximum voltage on EXTAL is below 3.0V. Use a resistor divider or other method to keep input voltage on EXTAL pin below 3.0V.

Fix plan: No plans to fix.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: MCF52235DE
Rev. 9, 02/2015