

TLE9832-2

Microcontroller with LIN and Power Switches for Automotive Applications

Data Sheet

Rev. 1.1, 2012-03-08

Edition 2012-03-08

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2012 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Table of Contents

| | | |
|----------|--|----|
| | Table of Contents | 3 |
| 1 | Summary of Features | 5 |
| 1.1 | Device Types / Ordering Information | 6 |
| 1.2 | Abbreviations | 7 |
| 2 | General Device Information | 9 |
| 2.1 | Pin Configuration | 9 |
| 2.2 | Pin Definitions and Functions | 10 |
| 3 | Functional Description | 14 |
| 3.1 | Power Management Unit (PMU) | 19 |
| 3.1.1 | Voltage Regulator 5.0V (VDDP) | 22 |
| 3.1.2 | Voltage Regulator 1.5V (VDDC) | 23 |
| 3.1.3 | External Voltage Regulator 5.0V (VDDEXT) | 24 |
| 3.2 | System Control Unit | 25 |
| 3.2.1 | System Control Unit - Power Modules | 25 |
| 3.2.2 | System Control Unit - Digital Part | 26 |
| 3.3 | XC800 Core | 26 |
| 3.4 | Memory Architecture | 28 |
| 3.5 | Flash Memory | 29 |
| 3.6 | Watchdog Timer 1 (WDT1) | 29 |
| 3.7 | Watchdog Timer (WDT) | 31 |
| 3.8 | Interrupt System | 32 |
| 3.9 | Multiplication/Division Unit | 38 |
| 3.10 | Parallel Ports | 38 |
| 3.11 | Timer 0 and Timer 1 | 41 |
| 3.12 | Timer 2 and Timer 21 | 42 |
| 3.13 | Timer 3 | 43 |
| 3.14 | Capture/Compare Unit 6 (CCU6) | 44 |
| 3.15 | UART | 46 |
| 3.16 | LIN Transceiver | 47 |
| 3.17 | High-Speed Synchronous Serial Interface | 47 |
| 3.18 | Measurement Unit | 49 |
| 3.19 | Measurement Core Module (incl. ADC2) | 51 |
| 3.20 | Analog Digital Converter (ADC1) | 52 |
| 3.21 | High Voltage Monitor Input | 53 |
| 3.22 | High Side Switches | 54 |
| 3.23 | Low Side Switches | 55 |
| 3.24 | PWM Generator | 56 |
| 3.25 | Debug System | 57 |
| 4 | Application Information | 58 |
| 4.1 | Electric Drive Application | 58 |
| 4.2 | Connection of N.C. Pins | 59 |
| 4.3 | Connection of ADCGND Pin | 59 |
| 4.4 | Connection of Exposed Pad | 59 |
| 4.5 | Voltage Regulators-Blocking Capacitors | 59 |
| 4.6 | Additional External Components | 59 |
| 4.7 | ESD Tests | 60 |
| 5 | Electrical Characteristics | 61 |

Table of Contents

| | | |
|----------|---|-----------|
| 5.1 | General Characteristics | 61 |
| 5.1.1 | Absolute Maximum Ratings | 61 |
| 5.1.2 | Functional Range | 62 |
| 5.1.3 | Current Consumption | 63 |
| 5.1.4 | Thermal Resistance | 63 |
| 5.1.5 | Timing Characteristics | 64 |
| 5.2 | Power Management Unit (PMU) | 65 |
| 5.2.1 | PMU I/O Supply Parameters VDDP | 65 |
| 5.2.2 | PMU Core Supply Parameters VDDC | 66 |
| 5.2.3 | VDDEXT Voltage Regulator 5.0V | 67 |
| 5.3 | System Clocks | 68 |
| 5.3.1 | Oscillators and PLL | 68 |
| 5.3.2 | External Clock Parameters XTAL1, XTAL2 | 69 |
| 5.4 | Flash Parameters | 70 |
| 5.5 | Parallel Ports (GPIO) | 71 |
| 5.5.1 | Functional Range | 71 |
| 5.5.2 | DC Parameters | 71 |
| 5.6 | LIN Transceiver | 74 |
| 5.6.1 | Electrical Characteristics | 74 |
| 5.7 | High-Speed Synchronous Serial Interface | 78 |
| 5.8 | Measurement Unit | 79 |
| 5.8.1 | Analog Digital Converter 8-Bit | 79 |
| 5.8.2 | Measurement Unit (VBAT_SENSE - Supply Voltage Attenuator) | 79 |
| 5.8.3 | Measurement Functions Monitoring Input Voltage Attenuator | 80 |
| 5.8.4 | Temperature Sensor Module | 81 |
| 5.9 | ADC - 10-Bit | 82 |
| 5.9.1 | VAREF | 82 |
| 5.9.1.1 | Functional Range | 82 |
| 5.9.1.2 | Electrical Characteristics | 82 |
| 5.9.2 | Analog/Digital Converter Parameters | 83 |
| 5.10 | High-Voltage Monitor Input | 85 |
| 5.11 | High Side Switches | 86 |
| 5.11.1 | Functional Range | 86 |
| 5.11.2 | Electrical Characteristics | 86 |
| 5.12 | Low Side Switches | 89 |
| 5.12.1 | Functional Range | 89 |
| 5.12.2 | Electrical Characteristics | 89 |
| 6 | Package Outlines | 91 |
| 7 | Revision History | 92 |

1 Summary of Features

- High performance XC800 core
 - compatible to standard 8051 core
 - up to 40 MHz clock frequency
 - two clocks per machine cycle architecture
 - two data pointers
- On-chip memory
 - 32 kByte + 4 kByte Flash for program code and data (4 kByte EEPROM emulation built-in)
 - 512 Byte One Time Programmable Memory (OTP)
 - 512 Byte 100 Time Programmable Memory (100TP)
 - 256 Byte RAM, 3 kByte XRAM
 - BootROM for startup firmware and Flash routines
- Core logic supply at 1.5 V
- On-chip OSC and PLL for clock generation
 - Loss of clock detection with fail safe mode for power switches
- Watchdog timer (WDT) with programmable window feature for refresh operation and warning prior to overflow
- General-purpose I/O Port (GPIO) with wake-up capability
- Multiplication/division unit (MDU) for arithmetic calculation
- Software libraries to support floating point and MDU calculations
- Five 16-Bit timers - Timer 0, Timer 1, Timer 2, Timer 21 and Timer 3
- Capture/compare unit for PWM signal generation (CCU6) with Timer 12 and Timer 13
- Full duplex serial interface (UART) with LIN support
- Synchronous serial channel (SSC)
- On-chip debug support via 2-wire Device Access Port (DAP)
- LIN Bootstrap loader (LIN BSL)
- LIN transceiver compliant to LIN 1.3, LIN 2.0 and LIN 2.1
- 2 x Low Side Switches with clamping capability incl. PWM functionality, e.g. as relay driver
- 2 x High Side Switches with cyclic sense option and PWM functionality, e.g. for LED or powering of switches
- 5 x High Voltage Monitor Input pins for wake-up and with cyclic sense and analog measurement option
- Measurement unit with 10 channels, 8-Bit A/D Converter (ADC2) and data post processing
- 8 channels, 10-Bit A/D Converter (including battery voltage and supply voltage measurement) (ADC1)
- Single power supply from 3.0 V to 27 V
- Low-dropout voltage regulators (LDO)
- Dedicated 5 V voltage regulator for external loads (e.g. hall sensor)
- Programmable window watchdog (WDT1) with independent on-chip clock source
- Power saving modes
 - MCU slow-down mode
 - Stop Mode
 - Sleep Mode
 - Cyclic wake-up and cyclic sense during Stop Mode and Sleep Mode
- Power-on and undervoltage/brownout reset generator
- Overtemperature protection
- Overcurrent protection with shutdown
- Supported by a full range of development tools including C compilers, macro assembler packages, emulators, evaluation boards, HLL debugger, programming tools, software packages
- Temperature Range T_j : -40 °C up to 150 °C
- Packages TLE9832-2QV: VQFN-48-22 and TLE9832-2QX: VQFN-48-29
- Green package (RoHS compliant)

1.1 Device Types / Ordering Information

The TLE983x product family features devices with different peripheral modules, configurations and program memory sizes to offer cost-effective solutions for different application requirements. [Table 1](#) describes the TLE9832-2 device configuration.

Table 1 Device Configuration

| Device Name | Max Clock Frequency | High Side Switches | High Voltage Monitor Inputs | Flash Size | Bidirectional Parallel Port I/O's | Operational Amplifier |
|-------------|---------------------|--------------------|-----------------------------|------------|-----------------------------------|-----------------------|
| TLE9832-2QV | 40 MHz | 2 | 5 | 36 kByte | 11 | no |
| TLE9832-2QX | 40 MHz | 2 | 5 | 36 kByte | 11 | no |

1.2 Abbreviations

The following acronyms and terms are used within this document. List see in [Table 2](#).

Table 2 Acronyms

| Acronyms | Name |
|----------|--|
| ALU | Arithmetic Logic Unit |
| CCU6 | Capture Compare Unit 6 |
| CGU | Clock Generation Unit |
| CMU | Cyclic Management Unit |
| DAP | Device Access Port |
| DPP | Data Post Processing |
| ECC | Error Correction Code |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| GPIO | General Purpose Input Output |
| FSR | Full Scale Range |
| ICU | Interrupt Control Unit |
| IRAM | Internal Random Access Memory - Internal Data Memory |
| LDO | Low DropOut voltage regulator |
| LIN | Local Interconnect Network |
| LSB | Least Significant Bit |
| MCU | Micro Controller Unit |
| MDU | Multiplication Division Unit |
| MMC | Monitor Mode Control |
| MSB | Most Significant Bit |
| NMI | Non Maskable Interrupt |
| OCDS | On Chip Debug Support |
| OTP | One Time Programmable |
| OSC | Oscillator |
| PC | Program Counter |
| PCU | Power Control Unit |
| PD | Pull Down |
| PGU | Power supply Generation Unit |
| PLL | Phase Locked Loop |
| PMU | Power Management Unit |
| PSW | Program Status Word |
| PU | Pull Up |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| RCU | Reset Control Unit |
| RMU | Reset Management Unit |

Table 2 Acronyms

| Acronyms | Name |
|-----------------|---|
| ROM | Read Only Memory |
| SCK | SSC Clock |
| SFR | Special Function Register |
| SOW | Short Open Window (for WDT1) |
| SPI | Serial Peripheral Interface |
| SSC | Synchronous Serial Channel |
| SSU | System Status Unit |
| TMS | Test Mode Select |
| UART | Universal Asynchronous Receiver Transmitter |
| UDIG | Universal Digital Controller for ADC1 |
| VBG | Voltage reference Band Gap |
| WDT | Watchdog timer |
| WMU | Wake-up Management Unit |
| XRAM | On-Chip eXternal Data Memory |
| XSFR | On-Chip eXternal Special Function Register |

2 General Device Information

2.1 Pin Configuration

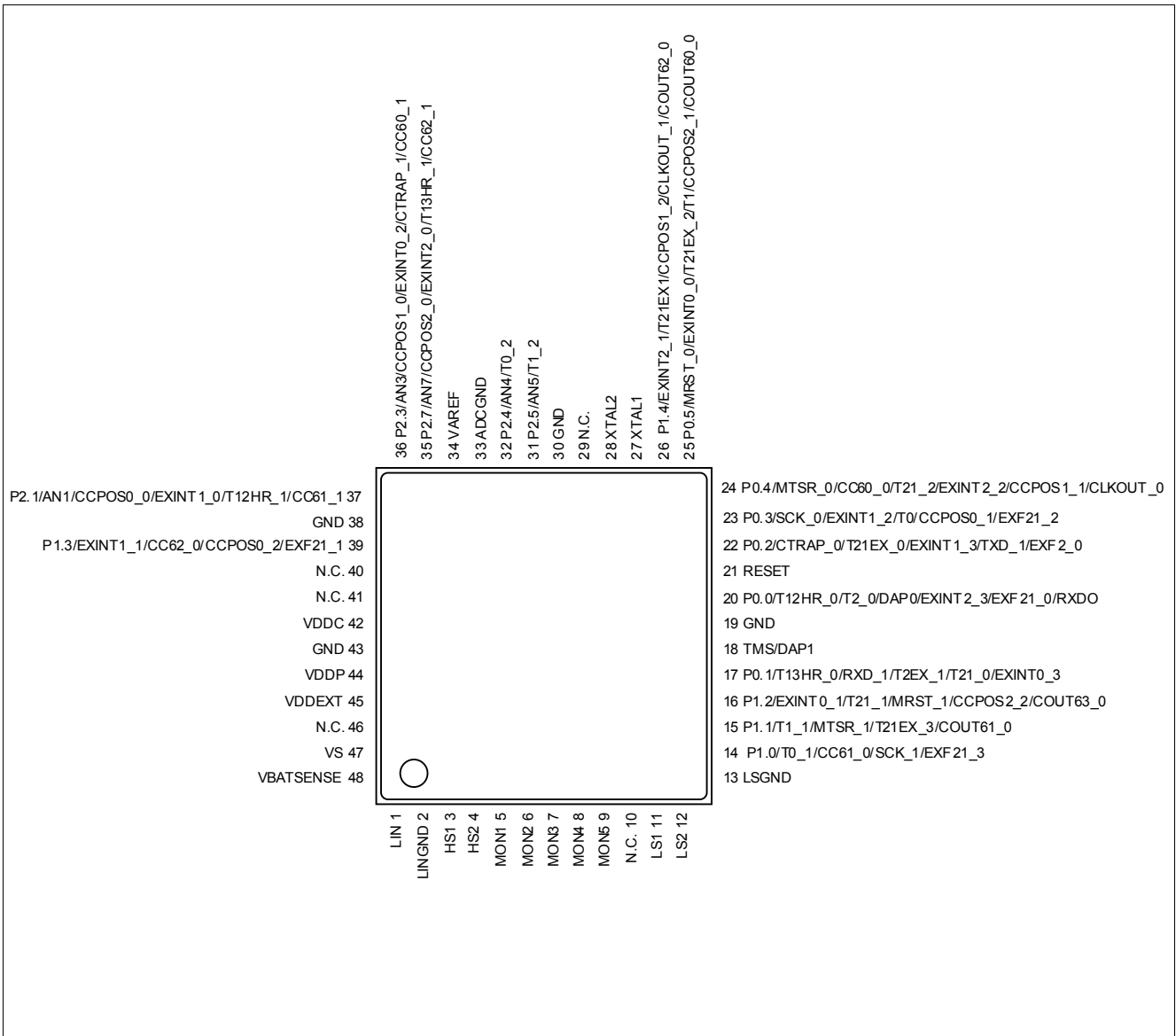


Figure 1 TLE9832-2 pin configuration, VQFN-48-22 and VQFN-48-29 packages (top view)

2.2 Pin Definitions and Functions

After reset, all pins are configured as input (except supply and LIN pins) with one of the following settings:

- Pull-up device enabled only (PU)
- Pull-down device enabled only (PD)
- Input with both pull-up and pull-down devices disabled (I)
- Output with output stage deactivated = high impedance state (Hi-Z)

The functions and default states of the TLE9832-2 external pins are provided in the following table.

Type: indicates the pin type.

- I/O: Input or output
- I: Input only
- O: Output only
- P: Power supply

Table 3 Pin Definitions and Functions

| Symbol | Pin Number | Type | Reset State | Function |
|-----------|------------|------|-------------|---|
| P0 | | | | Port 0 Port 0 is an 6-Bit bidirectional general purpose I/O port. Alternate functions can be assigned as follows: DAP, CCU6, Timer 0, Timer 1, Timer 2, Timer 21, UART, SSC, external interrupt input and clock output. |
| P0.0 | 20 | I/O | I/PU | T12HR_0 CCU6 Timer 12 hardware run input T2_0 Timer 2 input DAP0 Debug Access Port 0 EXINT2_3 External interrupt input 0 EXF21_0 Timer 21 external flag output RXDO UART transmit data output (synchronous mode) |
| P0.1 | 17 | I/O | I/PU | T13HR_0 CCU6 Timer 13 hardware run input RXD_1 UART receive input T2EX_1 Timer 2 external trigger input T21_0 Timer 21 input EXINT0_3 External interrupt input 0 |
| P0.2 | 22 | I/O | I/PU | CTRAP_0 CCU6 trap input T21EX_0 Timer 21 external trigger input EXINT1_3 External interrupt input 1 TXD_1 UART transmit output EXF2_0 Timer 2 external flag output |
| P0.3 | 23 | I/O | I/PU | SCK_0 SSC clock input (for slave) / output (for master) EXINT1_2 External interrupt input 1 T0 Timer 0 input CCPOS0_1 CCU6 hall input 0 EXF21_2 Timer 21 external flag output |
| P0.4 | 24 | I/O | I/PU | MTSR_0 SSC master transmit output / slave receive input CC60_0 CCU6 capture/compare channel 0 input/output T21_2 Timer 21 input EXINT2_2 External interrupt input 2 CCPOS1_1 CCU6 hall input 1 CLKOUT_0 Clock output |

Table 3 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|-----------|------------|------|-------------|---|
| P0.5 | 25 | I/O | I/PU | MRST_0 SSC master receive input / slave transmit output EXINT0_0 External interrupt input 0 T21EX_2 Timer 21 external trigger input T1 Timer 1 input CCPOS2_1 CCU6 hall input 2 COUT60_0 CCU6 capture/compare channel 0 output |
| P1 | | | | Port 1 Port 1 is an 5-Bit bidirectional general purpose I/O port. Alternate functions can be assigned as follows: CCU6, Timer 0, Timer 1 Timer 21, SSC, external interrupt input and clock output. |
| P1.0 | 14 | I/O | I | T0_1 Timer 0 input CC61_0 CCU6 capture/compare channel 1 input/output SCK_1 SSC clock input (for slave) / output (for master) EXF21_3 Timer 21 external flag output |
| P1.1 | 15 | I/O | I | T1_1 Timer 1 input MTRSR_1 SSC master transmit output/slave receive input T21EX_3 Timer 21 external trigger input COUT61_0 CCU6 capture/compare channel 1 output |
| P1.2 | 16 | I/O | I | EXINT0_1 External interrupt input 0 T21_1 Timer 21 input MRST_1 SSC master receive input/slave transmit output CCPOS2_2 CCU6 hall input 2 COUT63_0 CCU6 capture/compare channel 3 output |
| P1.3 | 39 | I/O | I | EXINT1_1 External interrupt input 1 CC62_0 CCU6 capture/compare channel 2 input/output CCPOS0_2 CCU6 hall input 0 EXF21_1 Timer 21 external flag output |
| P1.4 | 26 | I/O | I | EXINT2_1 External interrupt input 2 T21EX_1 Timer 21 external trigger input CCPOS1_2 CCU6 hall input 1 CLKOUT_1 Clock output COUT62_0 CCU6 capture/compare channel 2 output |
| P2 | | | | Port 2 Port 2 is an 5-Bit general purpose input-only port. Alternate functions can be assigned as follows: CCU6, Timer 0, Timer 1, Timer 21 and external interrupt input It is also used as analog inputs for the 10-Bit ADC (ADC1). |
| P2.1 | 37 | I | I | AN1 ADC1 analog input channel 1 CCPOS0_0 CCU6 hall input 0 EXINT1_0 External interrupt input 1 T12HR_1 CCU6 Timer 12 hardware run input CC61_1 CCU6 capture/compare channel 1 input |

Table 3 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|----------------|------|-------------|---|
| P2.3 | 36 | I | I | AN3 ADC1 analog input channel 3 CCPOS1_0 CCU6 hall input 1 EXINT0_2 External interrupt input 0 CTRAP_1 CCU6 trap input CC60_1 CCU6 capture/compare channel 0 input |
| P2.4 | 32 | I | I | AN4 ADC1 analog input channel 4 T0_2 Timer 0 input |
| P2.5 | 31 | I | I | AN5 ADC1 analog input channel 5 T1_2 Timer 1 input |
| P2.7 | 35 | I | I | AN7 ADC1 analog input channel 7 CCPOS2_0 CCU6 hall input 2 EXINT2_0 External interrupt input 2 T13HR_1 CCU6 timer 13 hardware run input CC62_1 CCU6 capture/compare channel 2 input |
| Power Supply | | | | |
| VS | 47 | P | – | Battery supply input |
| VDDP | 44 | P | – | I/O port supply (5.0 V). Do not connect external loads. For buffer and bypass capacitors. |
| VDDC | 42 | P | – | Core supply (1.5 V during Active Mode, 0.9 V during Stop Mode). Do not connect external loads. For buffer/bypass capacitor. |
| VDDEXT | 45 | P | – | External voltage supply output (5.0 V, 20 mA) |
| LSGND | 13 | P | – | Low Side ground LS1, LS2 |
| GND | 30, 43, 19, 38 | P | – | Core supply ground; analog supply ground |
| ADCGND | 33 | P | – | Analog supply ground for ADC1 |
| LINGND | 2 | P | – | LIN ground |
| Monitor Inputs | | | | |
| MON1 | 5 | I | I | High Voltage Monitor Input 1 |
| MON2 | 6 | I | I | High Voltage Monitor Input 2 |
| MON3 | 7 | I | I | High Voltage Monitor Input 3 |
| MON4 | 8 | I | I | High Voltage Monitor Input 4 |
| MON5 | 9 | I | I | High Voltage Monitor Input 5 |
| High Side Switch / Low Side Switch Outputs | | | | |
| LS1 | 11 | O | Hi-Z | Low Side Switch output 1 |
| LS2 | 12 | O | Hi-Z | Low Side Switch output 2 |
| HS1 | 3 | O | Hi-Z | High Side Switch output 1 |
| HS2 | 4 | O | Hi-Z | High Side Switch output 2 |
| LIN Interface | | | | |
| LIN | 1 | I/O | PU | LIN bus interface input/output |

Table 3 Pin Definitions and Functions (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---------------|-----------------------|------|-------------|--|
| Others | | | | |
| VAREF | 34 | I/O | O | 5V ADC1 reference voltage |
| XTAL1 | 27 | I | I | External oscillator input |
| XTAL2 | 28 | O | Hi-Z | External oscillator output |
| TMS | 18 | I | I/PD | TMS test mode select input DAP1 Debug Access Port 1 |
| RESET | 21 | I/O | I/O/PU | Reset input, not available during Sleep Mode |
| VBAT_SENSE | 48 | I | I | Battery supply voltage sense input |
| N.C. | 10, 29, 40, 41, 46 | – | – | Not connected - can be connected to GND |

3 Functional Description

This highly integrated circuit contains analog and digital functional blocks. For system and interface control an embedded 8-Bit state-of-the-art microcontroller, compatible to the standard 8051 core with On-Chip Debug Support (OCDS), is available. For internal and external power supply purposes, on-chip low drop-out regulators are existent. An internal oscillator provides a cost effective and suitable clock in particular for LIN slave nodes. As communication interface, a LIN transceiver and several High Voltage Monitor Inputs with adjustable threshold and filters are available. Furthermore two High Side Switches (e.g. for driving LEDs or cyclic powering of switches), two Low Side Switches (e.g. for relays) and several general purpose input/outputs (GPIO) with pulse-width modulation (PWM) capabilities are available.

The Micro Controller Unit (MCU) supervision and system protection including reset feature is controlled by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support terminal 30 connected automotive applications. A wake-up from the power saving mode is possible via a LIN bus message, via the monitoring inputs, via the GPIO ports or repetitive with a programmable time period (cyclic wake-up).

The integrated circuit is available in a VQFN-48-22 and VQFN-48-29 package with 0.5 mm pitch and is designed to withstand the severe conditions of automotive applications.

Block Diagram

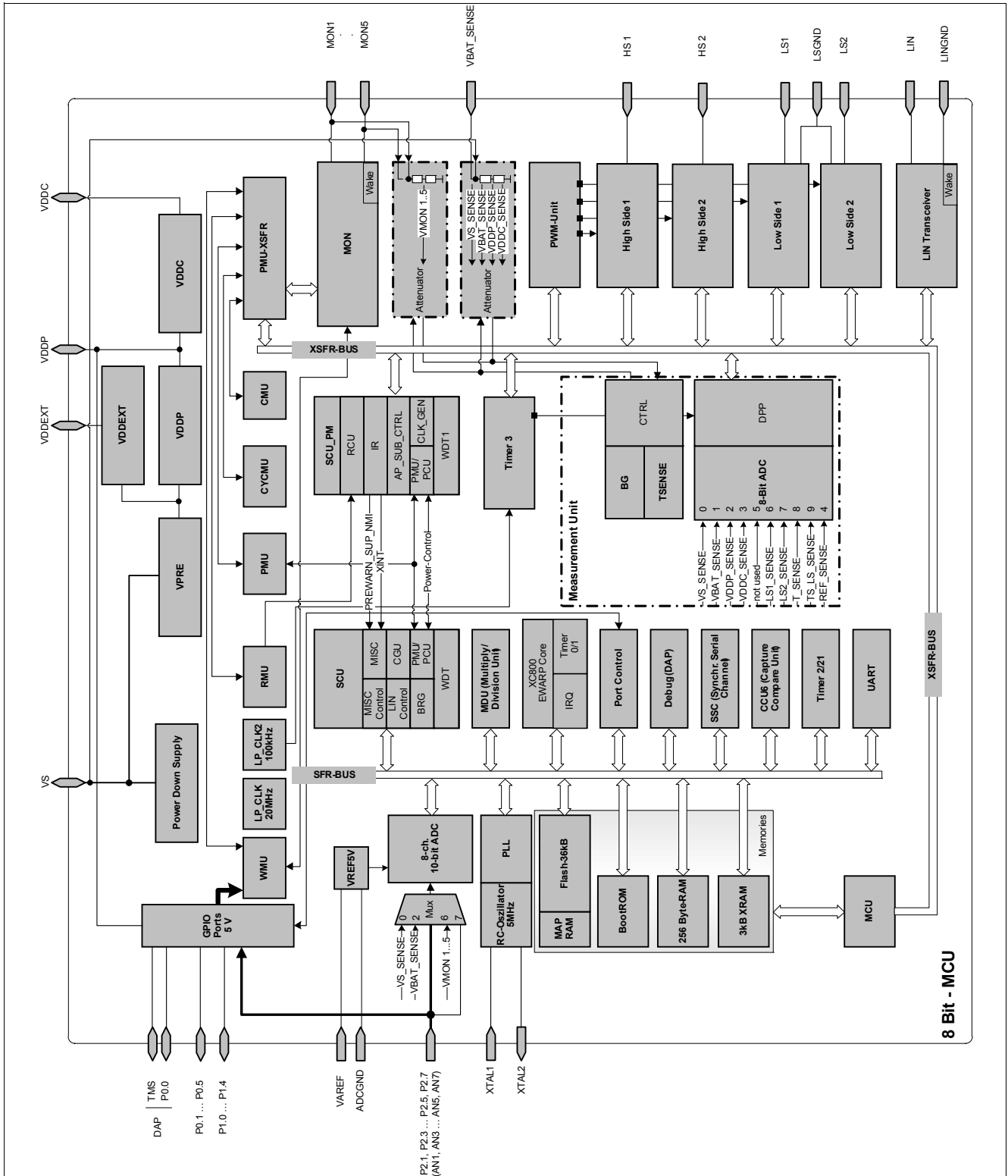


Figure 2 Block Diagram

The TLE9832-2 has several operational modes mainly to support low power consumption requirements. The low power modes and state transitions are depicted in [Figure 3](#) below.

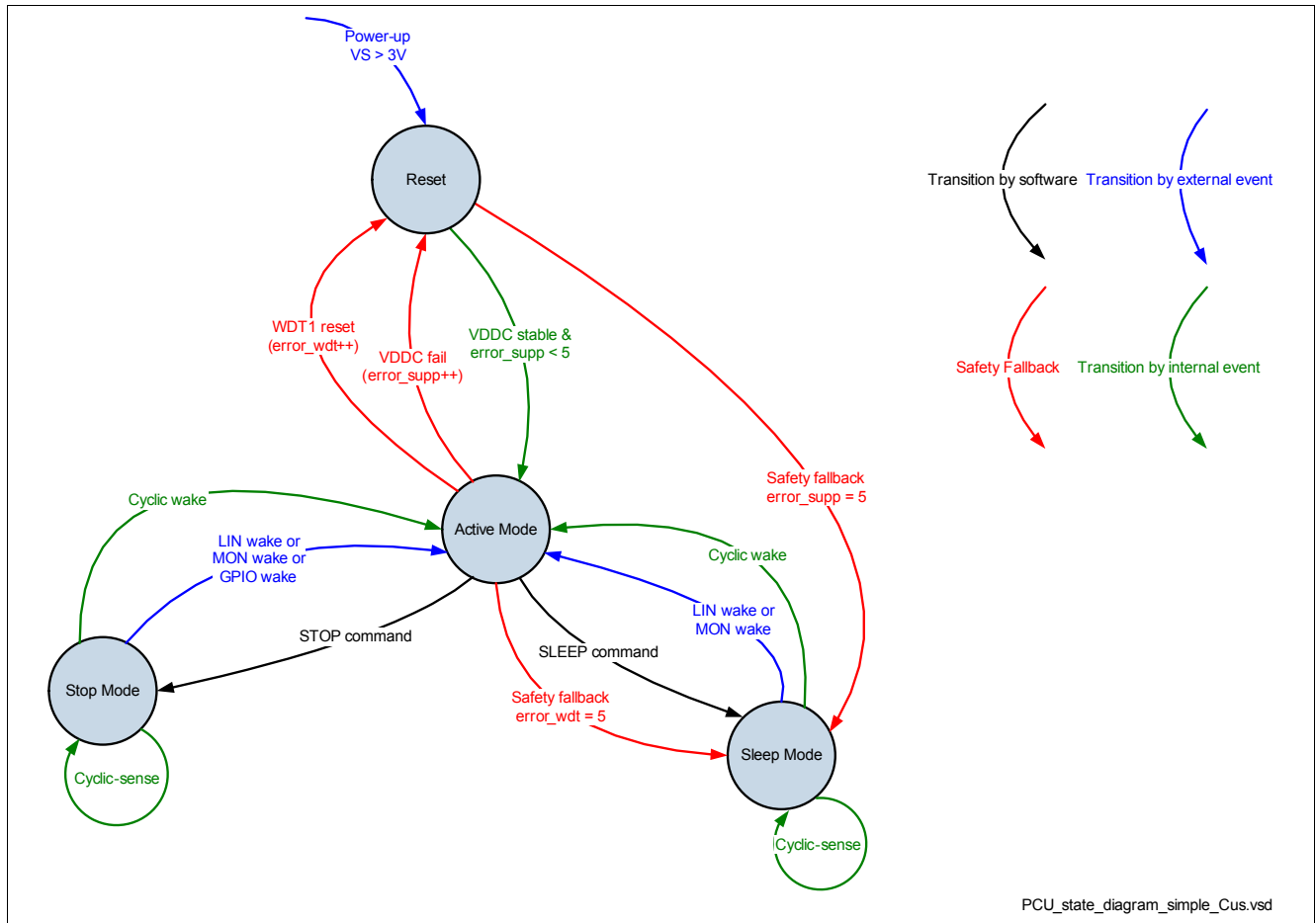


Figure 3 Power Control State Diagram

Reset Mode

The Reset Mode is a transition mode e.g. during power-up of the device after a power-on reset. In this mode the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the Active Mode is entered. In case the watchdog timer WDT1 fails for more than four times, a fail-safe transition to the Sleep Mode is done.

Active Mode

In Active Mode all modules are activated and the TLE9832-2 is fully operational.

Stop Mode

The Stop Mode is one out of two low power modes. The transition to the low power modes is done by setting the respective Bits in the mode control register. In Stop Mode the embedded microcontroller is still powered allowing faster wake-up reaction times. A wake-up from this mode is possible by LIN bus activity, the High Voltage Monitor Input pins or the respective 5V GPIOs.

Sleep Mode

The Sleep Mode is the second low-power mode. The transition to the low-power modes is done by setting the respective Bits in the MCU mode control register. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption, but the wake-up time is longer compared to the Stop Mode. A wake-up from this mode is possible by LIN bus activity or the High Voltage Monitor Input pins. A wake-up from Sleep Mode behaves similar to a power-on reset.

Cyclic Wake-up Mode

The cyclic wake-up mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic wake-up mode is done by first setting the respective Bits in the mode control register followed by the SLEEP or STOP command. Additional to the cyclic wake-up behavior (wake-up after a programmable time period), the wake-up sources of the normal Stop Mode and Sleep Mode are available.

Cyclic Sense Mode

The cyclic sense mode is a special operating mode of the Sleep Mode and the Stop Mode. The transition to the cyclic sense mode is done by first setting the respective Bits in the mode control register followed by the STOP or SLEEP command. In cyclic sense mode a High Side Switch can be switched on periodically for biasing some switches for example. The wake-up condition is configurable, when the sense result of defined monitor inputs at a window of interest changed compared to the previous wake-up period or reached a defined state respectively. In this case the Active Mode is entered immediately. For cyclic sense in Stop Mode VDDEXT can be switched on periodically. Furthermore cyclic sense allows to sense dedicated GPIO port states and transitions when in Stop Mode.

The following table shows the possible power mode configurations of each major module or function respectively.

Table 4 Power mode configurations

| Module/function | Active Mode | Stop Mode | Sleep Mode | Comment |
|---------------------------|------------------------------|---|----------------------------|--------------------------------|
| VDD1V5PD | ON | ON | ON | Power Down Supply |
| VPRE, VDDP, VDDC | ON | ON (no dynamic load) | OFF | – |
| VDDEXT | ON/OFF | ON (no dynamic load)/OFF cyclic ON/OFF | OFF | – |
| HSx | ON/OFF | cyclic ON/OFF | cyclic ON/OFF | cyclic sense |
| LSx | ON/OFF | OFF | OFF | – |
| PWM GEN. | ON/OFF | OFF | OFF | – |
| LIN TRx | ON/OFF | wake-up only/ OFF | wake-up only/ OFF | – |
| MON1 - MON5 (wake-up) | n.a. | disabled/static/cyclic | disabled/static/ cyclic | cyclic: combined with HS=on |
| MON1 - MON5 (measurement) | ON/OFF | OFF | OFF | available on four channels |
| VS sense | ON/OFF brownout detection | brownout detection | brownout detection | brownout detection done in PCU |
| VBAT_SENSE | ON/OFF | OFF | OFF | – |
| GPIO 5V (wake-up) | n.a. | disabled/static/cyclic | OFF | – |
| GPIO 5V (active) | ON | ON | OFF | – |
| WDT1 | ON | OFF | OFF | – |

Table 4 Power mode configurations

| Module/function | Active Mode | Stop Mode | Sleep Mode | Comment |
|-------------------|-----------------------|-------------------------------------|-------------------------------------|--|
| CYCLIC Modes | n.a. | cyclic wake-up/ cyclic sense/OFF | cyclic wake-up/ cyclic sense/OFF | cyclic sense with HS, VDDEXT; wake-up from cyclic wake needs MC for entering Sleep Mode / Stop Mode again |
| Measurement Unit | ON ¹⁾ | OFF | OFF | – |
| MCU | ON/slow- down/HALT | STOP ²⁾ | OFF | – |
| CLOCK GEN (MC) | ON | OFF | OFF | – |
| LP_CLK (20 MHz) | ON | OFF | OFF | WDT1 |
| LP_CLK2 (100 kHz) | ON | ON | ON | for cyclic wake-up |

1) Cannot not be switched off due to safety reasons

2) MC PLL clock disabled, MC supply reduced to 0.9 V

Wake-up Source Prioritization

All wake-up sources have the same priority. In order to handle the asynchronous nature of the wake-up sources, the first wake-up signal will initiate the wake-up sequence. Nevertheless all wake-up sources are latched in order to provide all wake-up events to the application software. The software can clear the wake-up source flags. It is ensured, that no wake-up event is lost.

As default wake-up sources, the LIN and MON inputs are activated after power-on reset only. GPIO ports as wake-up sources are disabled by default after power-on reset. The application software can reconfigure the wake-up sources according to the application needs.

Wake-up Levels and Transitions

The wake-up can be triggered by rising, falling or both signal edges for each monitor and GPIO input individually.

3.1 Power Management Unit (PMU)

The purpose of the power management unit is to ensure the fail safe behavior of embedded automotive systems. Therefore the power management unit controls all system modes including the corresponding transitions. The power management unit is responsible for generating all required voltage supplies for the embedded MCU (VDDC, VDDP) and the external sensor supply (VDDEXT). Additionally, the PMU provides well defined sequences for the system mode transitions and generates hierarchical reset priorities. The reset priorities control the reset behavior of all system functionalities, especially the reset behavior of the embedded MCU, including the test hardware. All these functions are controlled by finite state machines. The system master functionality of the PMU forces the generation of an independent logic supply (Power Down Supply) and system clock (LP_CLK). Therefore the PMU needs a module internal logic supply and system clock which works independently of the MCU clock.

The following state diagram shows the available modes of the device.

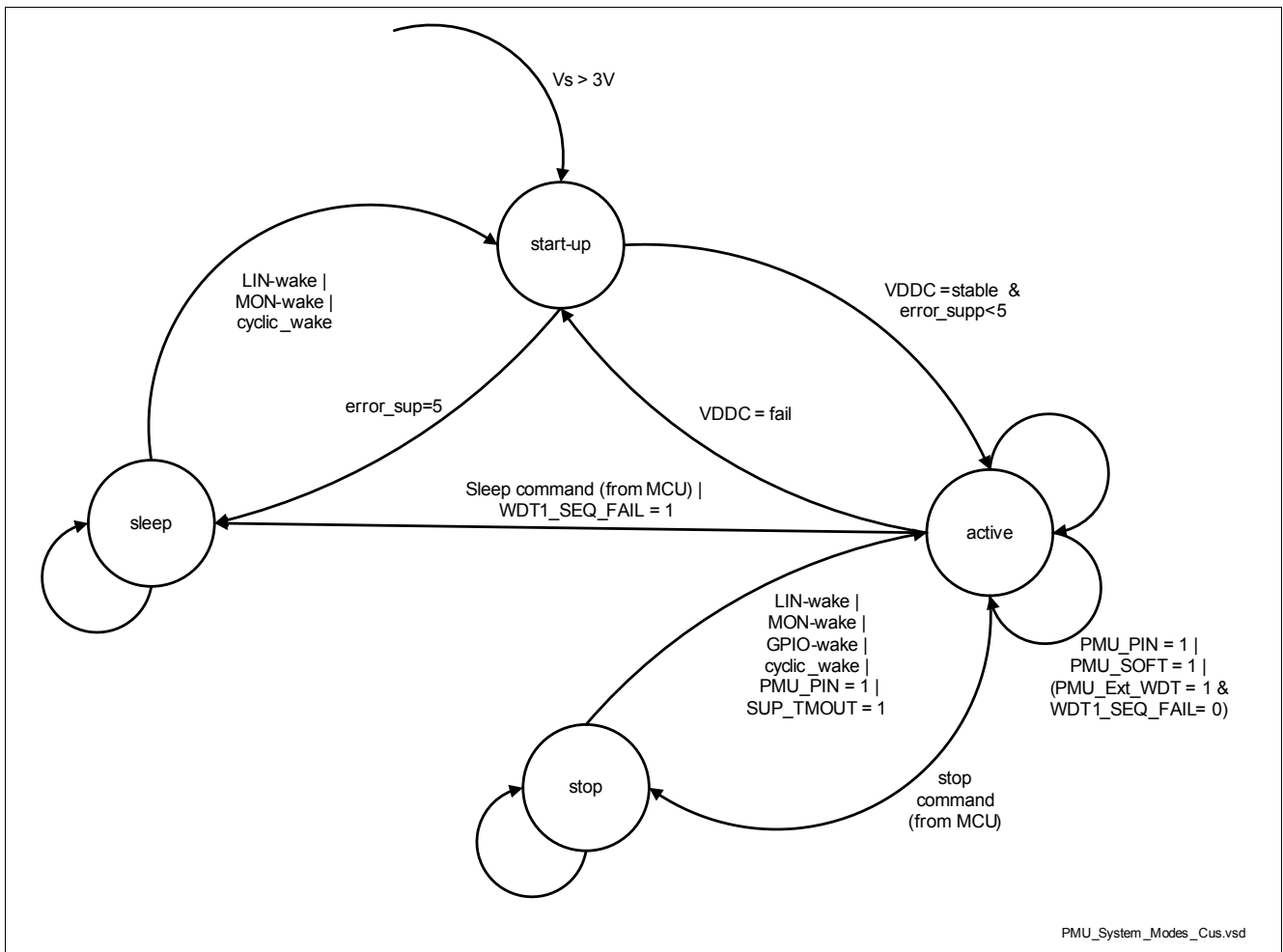


Figure 4 Power Management Unit System Modes

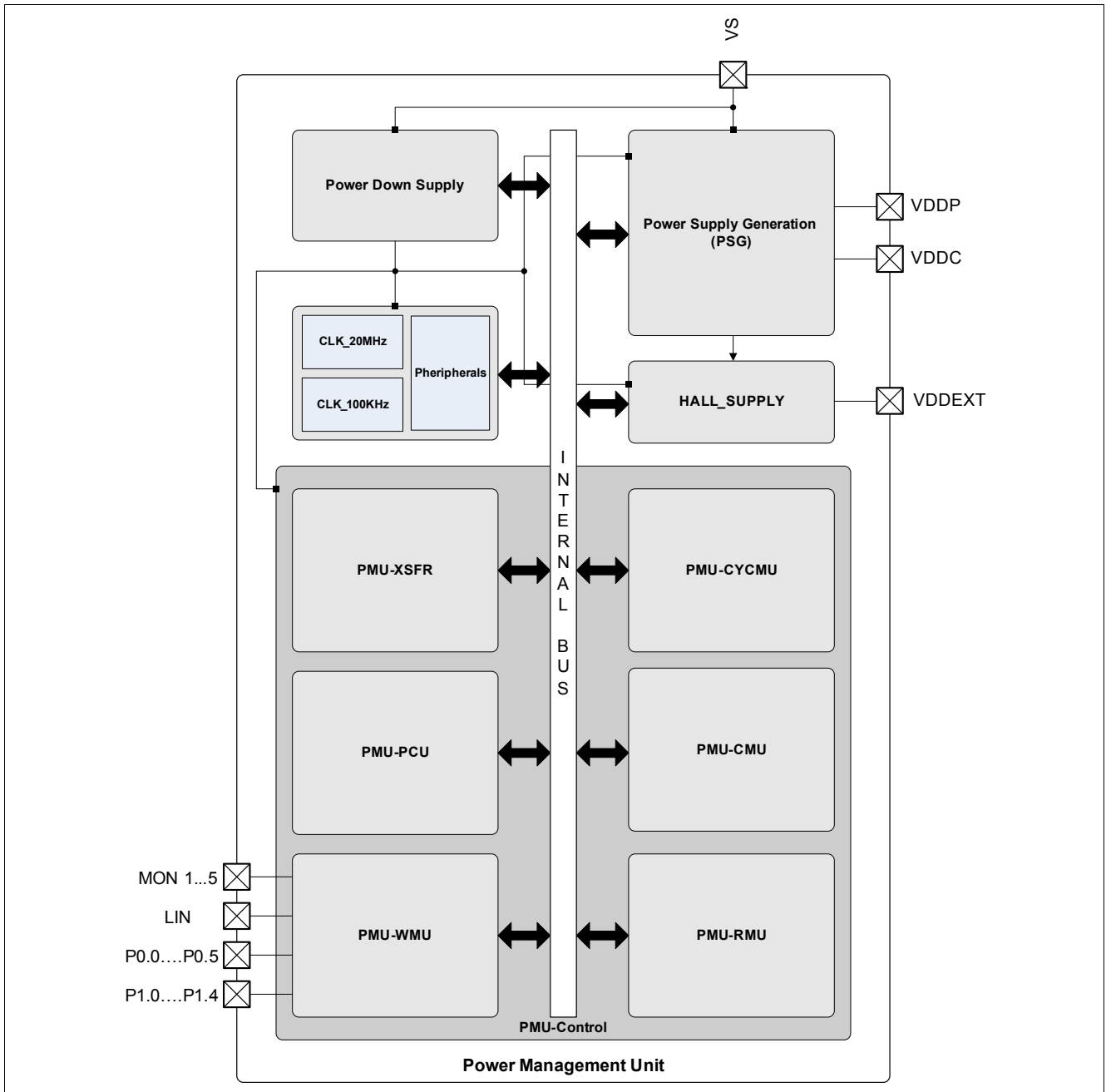


Figure 5 Power Management Unit Block Diagram

Table 5 Description of PMU Submodules

| Mod. Name | Modules | Functions |
|------------------------------------|--|--|
| Power Down Supply | Independent Supply Voltage Generation for PMU | This supply is only dedicated to the PMU to ensure a independent operation of generated power supplies (VDDP, VDDC). |
| LP_CLK (= 20 MHz) | - Clock Source for all PMU submodules - Backup Clock Source for System - Clock Source for WDT1 | This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL clock failure and as independent clock source for WDT1 |
| LP_CLK2 (= 100 kHz) | Clock Source for PMU | This ultra low power oscillator generates the clock for the PMU mainly in Stop Mode and in the cyclic modes. |
| Peripherals | Peripheral blocks of PMU | This blocks includes all relevant peripherals to ensure a stable and fail safe PMU startup and operation |
| Power Supply Generation Unit (PGU) | Voltage regulators for VDDP and VDDC | This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC) including all diagnosis and safety features |
| VDDEXT (Hall Sensor Supply) | Voltage regulator for VDDEXT to supply external modules (e.g. Hall Sensors) | This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor) |
| PMU-XSFR | All PMU relevant Extended Special Function Registers | This module contains all PMU relevant registers, which are needed to control and monitor the PMU. |
| PMU-PCU | Power Control Unit of the PMU | This block is responsible for controlling all power related actions within the PGU Module. |
| PMU-WMU | Wake-up Management Unit of the PMU | This block is responsible for controlling all wake-up related actions within the PMU Module. |
| PMU-CYCMU | Cyclic Management Unit of the PMU | This block is responsible for controlling all actions within cyclic mode. |
| PMU-CMU | Clock Management Unit of the PMU | This block is responsible for controlling all clocking actions within the PMU. |
| PMU-RMU | Reset Management Unit of the PMU | This block is responsible for generating all system required resets. |

3.1.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which serves as pad supply for the parallel port pins and other 5 V analog functions.

Features

- 5 V low-drop voltage regulator
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (Interrupt)
- Overvoltage monitoring with MCU signalling (Interrupt)
- Undervoltage monitoring with MCU signalling (Interrupt)
- Preregulator for VDDC regulator
- GPIO supply
- Pull-down current source at the output for Sleep Mode (100 μ A)

The output capacitor C_{VDDP} is mandatory to ensure a proper regulator functionality.

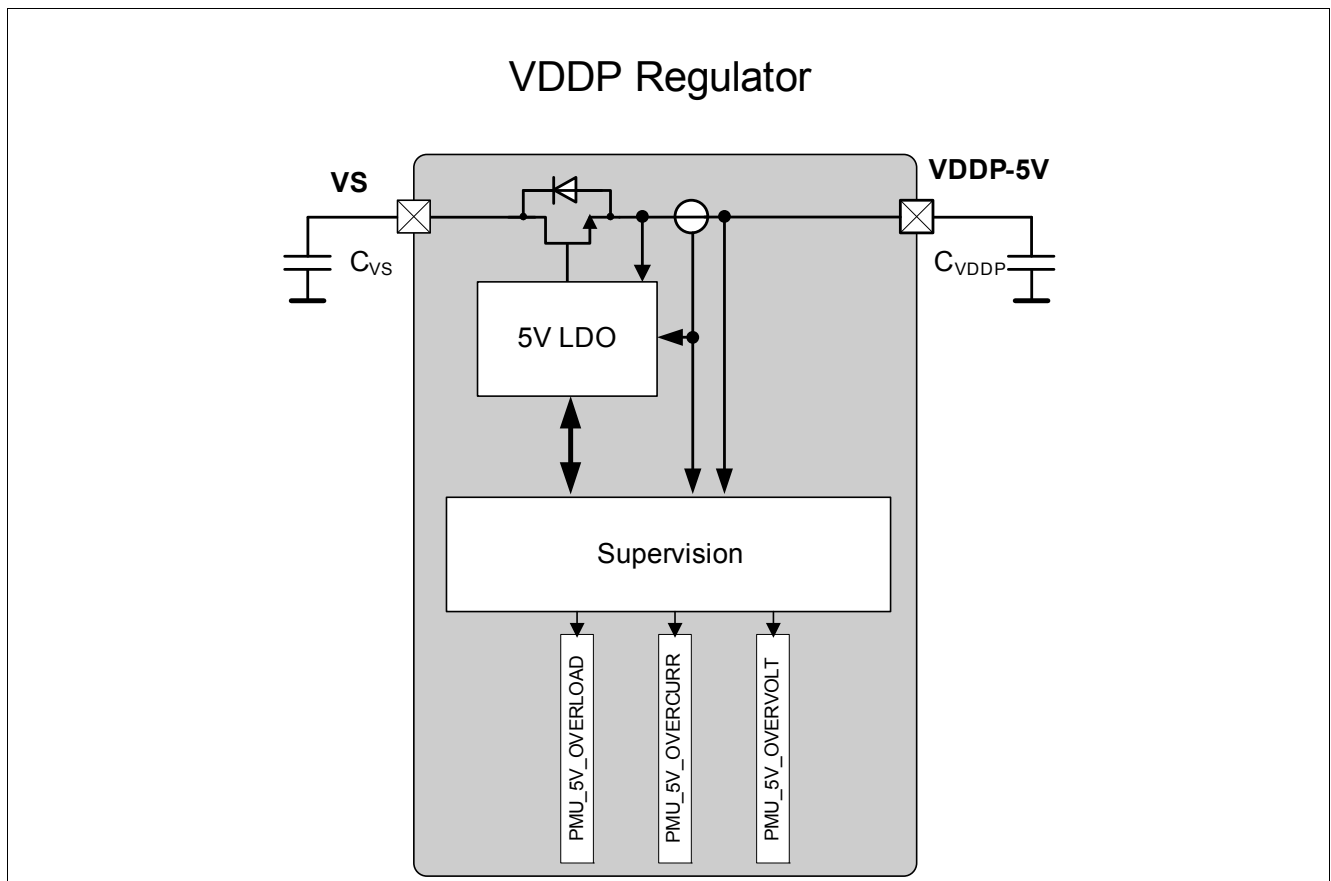


Figure 6 Module Block Diagram of VDDP Voltage Regulator

3.1.2 Voltage Regulator 1.5V (VDDC)

This module represents the 1.5 V voltage regulator, which serves as core supply for the 8-bit μ C and other chip internal analog 1.5 V functions (e.g. 8 Bit ADC). To further reduce the current consumption of the 8-bit MCU during Stop Mode the output voltage is optionally reduced to 0.9 V.

Features

- 1.5 V low-drop voltage regulator
- Optional 0.9 V in Stop Mode
- Current limitation
- Overcurrent monitoring and shutdown with MCU signalling (interrupt)
- Overvoltage monitoring with MCU signalling (interrupt)
- Undervoltage monitoring with MCU signalling (interrupt)
- Pull-down current source at the output for Sleep Mode (100 μ A)

The output capacitor C_{VDDC} is mandatory to ensure a proper regulator functionality.

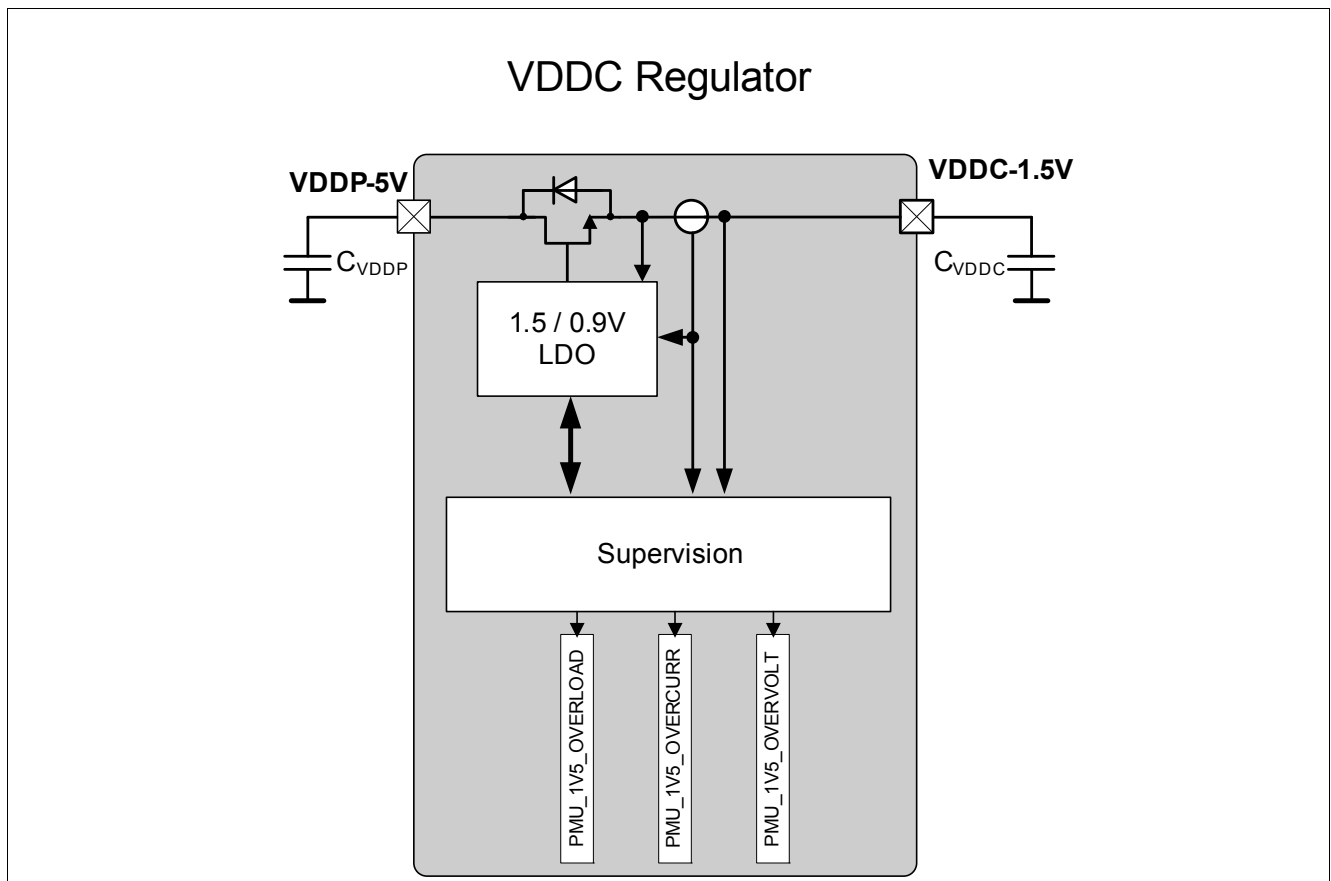


Figure 7 Module Block Diagram of VDDC Voltage Regulator

3.1.3 External Voltage Regulator 5.0V (VDDEXT)

The external voltage regulator provides 5 V output voltage in order to supply external circuitry like LEDs, hall sensors or potentiometers.

Features

- Switchable +5 V, 20 mA low-drop voltage regulator
- Switch-on overcurrent blanking time in order to drive small capacitive loads
- Short circuit robust
- Overvoltage monitoring with MCU interrupt signalling
- Undervoltage monitoring with MCU interrupt signalling
- Selectable switch-on slew-rate 0.95 V/ μ s max. @10 mA supply current, 10 nF capacitive load
- Pull-down current source at the output for Sleep Mode and off mode (100 μ A)
- Cyclic sense option together with GPIOs

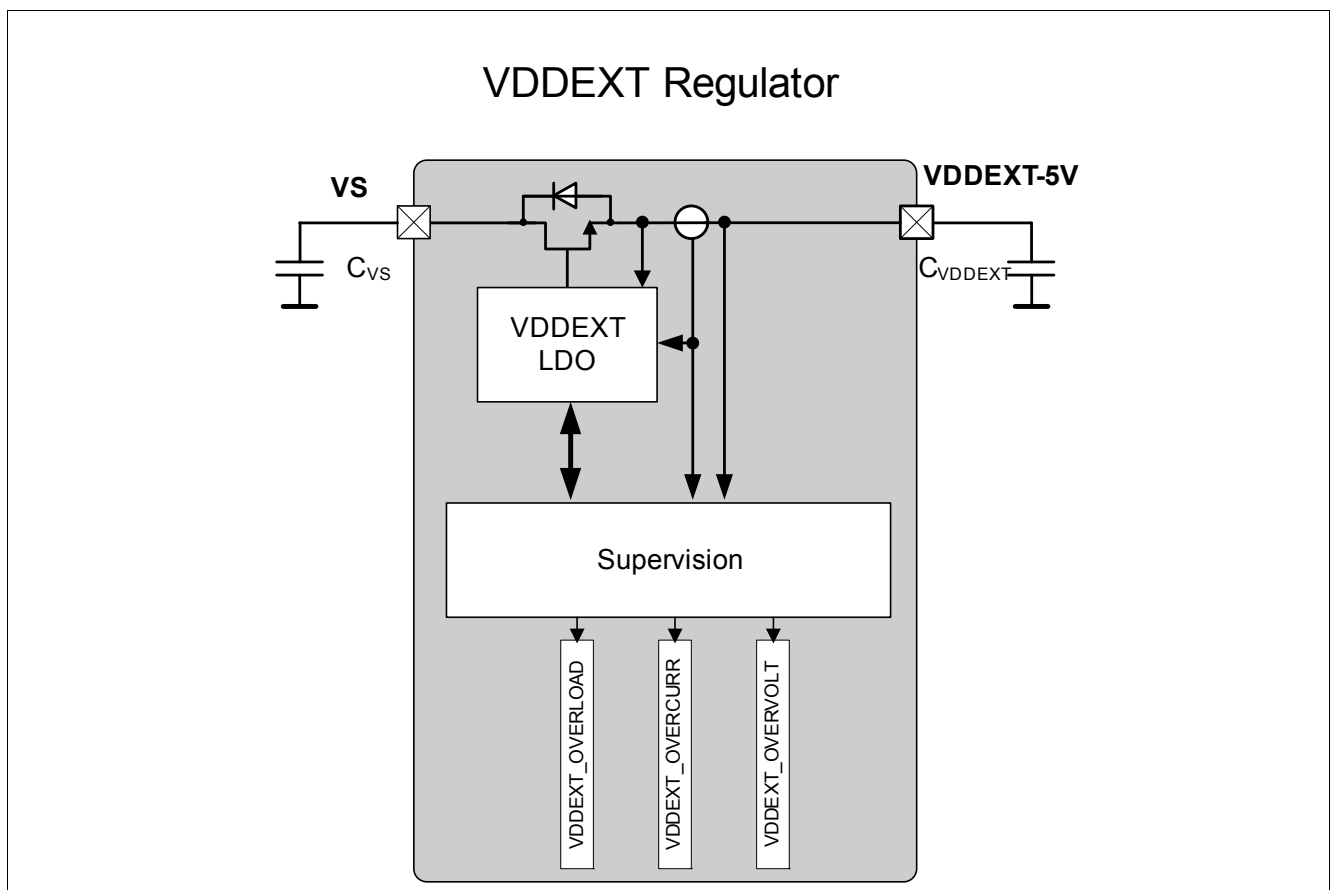


Figure 8 Module Block Diagram

3.2 System Control Unit

3.2.1 System Control Unit - Power Modules

The System Control Unit of the power modules consists of the following sub-modules:

- Reset Control Unit (RCU): generation of all required subsystem resets
- Clock Generation Unit (CGU): providing all required clocks to the analog subsystem
- Interrupt Control Unit (ICU): all system relevant interrupt flags and status flags
- Power Control Unit (PCU): takes over control when device enters and exits Sleep Mode and Stop Mode
- System Status Unit (SSU): controls mode changes due to system failures
- External Watchdog (WDT1): independent system watchdog to monitor system activity

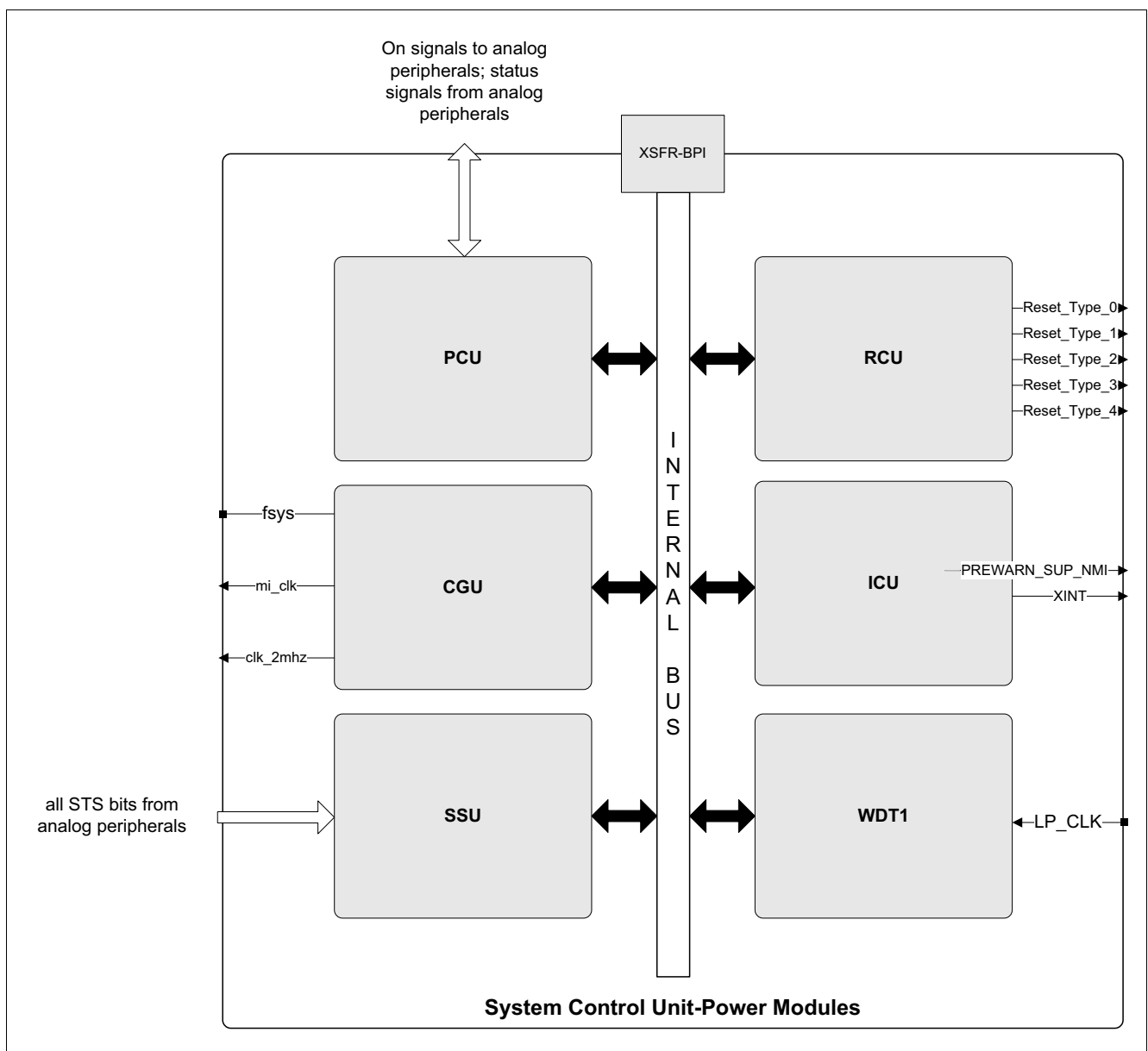


Figure 9 Block Diagram of System Control Unit - Power Modules

3.2.2 System Control Unit - Digital Part

The System Control Unit - Digital Part supports all central control tasks in the TLE9832-2. It consists of the following submodules:

- Clock System and Control
- Reset Control
- Power Management
- Interrupt Management
- General Port Control
- Flexible Peripheral Management
- Module Suspend Control
- Watchdog Timer
- XRAM Addressing Modes
- Error Detection and Correction in Data Memory
- Miscellaneous Control
- Register Mapping

3.3 XC800 Core

The XC800 Core is a complete, high performance CPU core that is functionally upward compatible to the 8051. While the standard 8051 core is designed around a 12-clock machine cycle, the XC800 Core uses a two-clock period machine cycle.

The instruction set consists of 45% one-Byte, 41% two-Byte and 14% three-Byte instructions. Each instruction takes 1, 2 or 4 machine cycles to execute. In case of access to slower memory, the access time may be extended by wait cycles (one wait cycle lasts one machine cycle, which is equivalent to two clock cycles).

Via the dedicated DAP interface the XC800 Core supports a range of debugging features including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and special function registers.

The key features of the XC800 Core implemented are listed below.

- Two clocks per machine cycle
- 256 Byte of internal data memory
- Program memory download option
- 15-source, 4-level interrupt controller
- 2 data pointers
- Power saving modes
- Dedicated debug mode via low-pin-count DAP interface (native JTAG mode)
- Two 16-Bit timers (Timer 0 and Timer 1)

Figure 10 shows the functional blocks of the XC800 Core. The XC800 Core consists mainly of the instruction decoder, the arithmetic section, the program control section, the access control section, and the interrupt controller.

The instruction decoder decodes each instruction and accordingly generates the internal signals required to control the functions of the individual units within the core. These internal signals have an effect on the source and destination of data transfers and control the ALU processing.

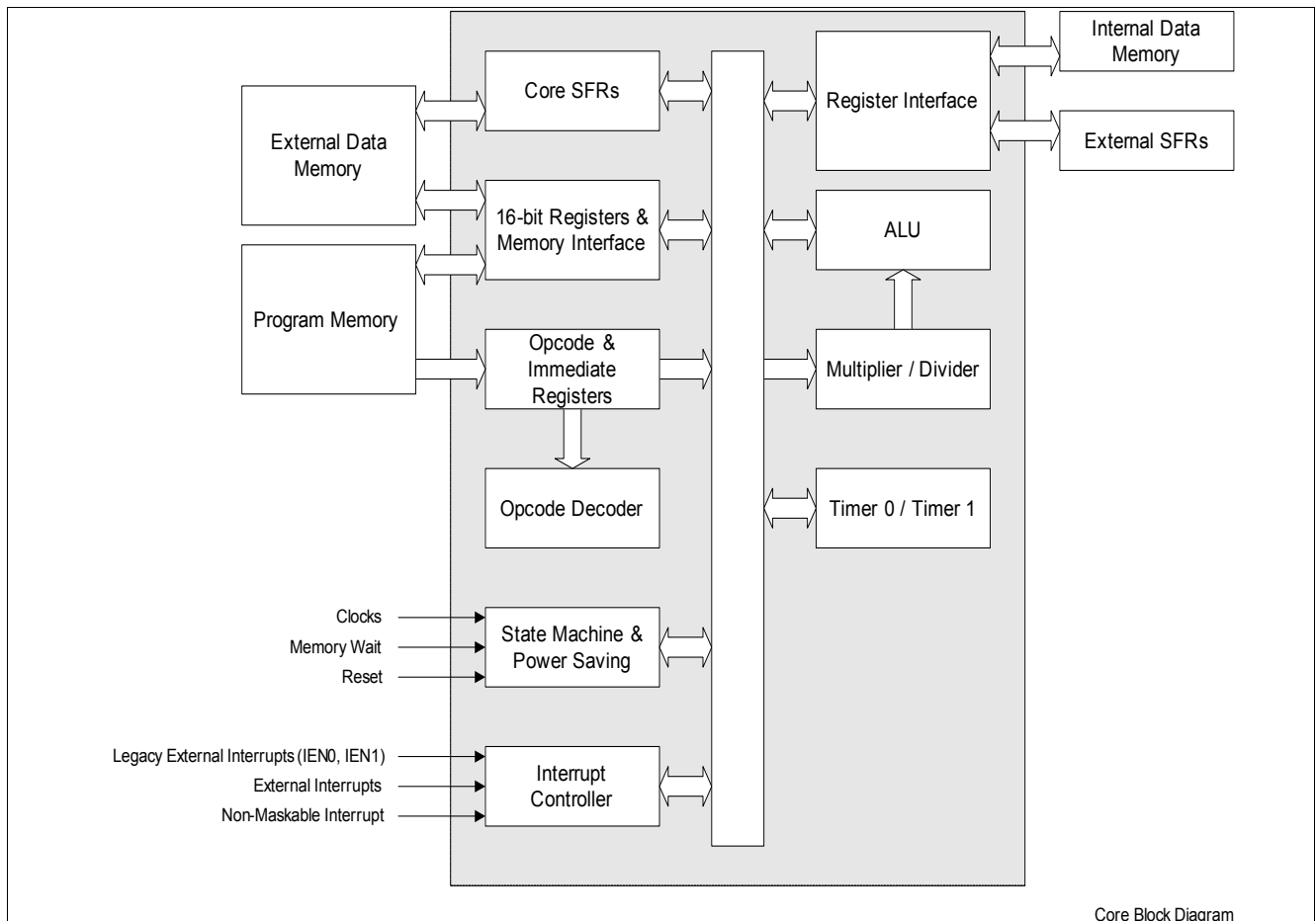


Figure 10 XC800 Core Block Diagram

The arithmetic section of the processor performs extensive data manipulation and consists of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-Bit data words from one or two sources and generates an 8-Bit result under the control of the instruction decoder. The ALU performs both arithmetic and logic operations. Arithmetic operations include add, subtract, multiply, divide, increment, decrement, BCD-decimal-add-adjust and compare. Logic operations include AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean unit performing the Bit operations as set, clear, complement, jump-if-set, jump-if-not-set, jump-if-set-and-clear and move to/from carry. The ALU can perform the Bit operations of logical AND or logical OR between any addressable Bit (or its complement) and the carry flag, and place the new result in the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-Bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

The access control unit is responsible for the selection of the on-chip memory resources. The interrupt requests from the peripheral units are handled by the interrupt controller unit.

3.4 Memory Architecture

The TLE9832-2 CPU manipulates operands in the following memory spaces:

- 36 kByte of Flash memory in code space
- BootROM memory in code space
- 256 Byte of internal RAM data memory in internal data space
- 3 kByte of XRAM memory in code space and external data space (XRAM can be read/written as program memory or external data memory)
- 128 Byte of special function registers SFR in internal data space
- 256 Byte of special function registers XSFR in external data space.

Figure 11 illustrates the memory address spaces of the TLE9832-2.

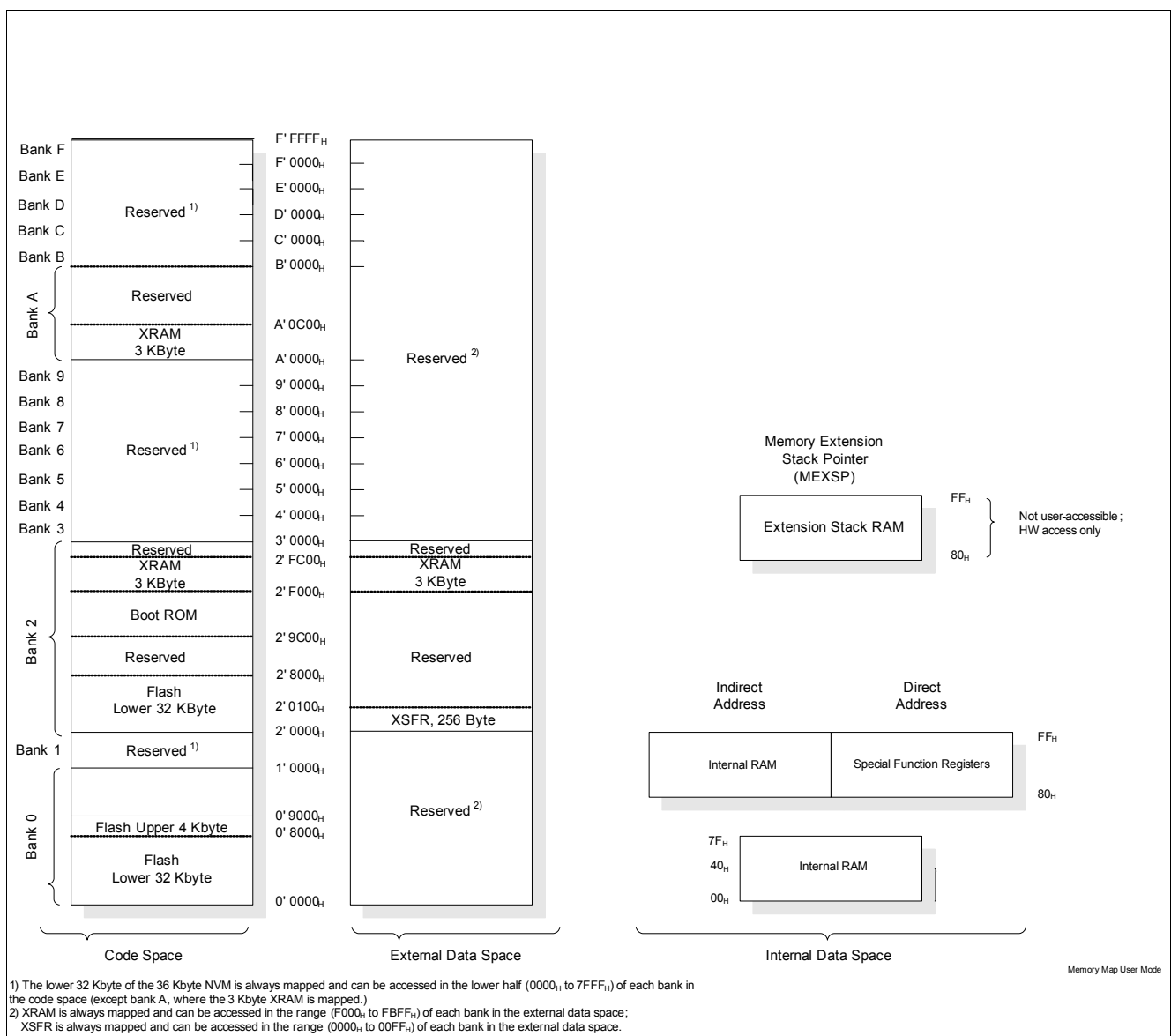


Figure 11 TLE9832-2 Memory Map

3.5 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 1.5V supply (VDDC) from the internal voltage regulator and does not require additional programming or erasing voltage.

Features

- In-System Programming via LIN (Flash mode) and DAP
- Error Correction Code (ECC) for dynamic correction of single Bit errors and signalling for double Bit failures
- Support for aborting erase operation
- Program width of 128 Byte (page)
- Minimum erase width of 128 Byte (page)
- 4 Byte read access
- Read access time: 75 ns
- Program time for 1 page: 3 ms
- Page erase time: 4 ms

3.6 Watchdog Timer 1 (WDT1)

Features

- Windowed Watchdog Timer with programmable timing in Active Mode
- Long open window (80ms) after power-up, reset, wake-up
- Short open window (30ms) to facilitate Flash programming
- Disabled during debugging
- Safety shutdown to Sleep Mode after 5 missed WDT1 services

There are two watchdog timers in the system. The Watchdog Timer (WDT) within the microcontroller (see [Chapter 3.7](#)) and the Watchdog Timer 1 (WDT1), which is described in this section.

In Active Mode, the WDT1 acts as a windowed watchdog timer, which provides a highly reliable and safe way to recover from software or hardware failures.

The WDT1 is always enabled in Active Mode. In Sleep Mode, Stop Mode and OCDS mode the WDT1 is disabled.

The behavior of the Watchdog Timer 1 in Active Mode is depicted in [Figure 12](#).

3.7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a sub-module in the System Control Unit (SCU). The Watchdog Timer provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT helps to abort an accidental malfunction of the TLE9832-2 in a user-specified time period. When enabled, the WDT will cause the TLE9832-2 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing an TLE9832-2 system reset. Hence, routine service of the WDT confirms that the system is functioning properly.

The WDT is disabled by default.

In debug mode, the WDT is suspended by default and stops counting (its debug suspend Bit is set by default i.e. MODSUSP.WDTSUSP = 1). Therefore during debugging, there is no need to refresh the WDT.

Features

- 16-Bit Watchdog Timer
- Programmable reload value for upper 8 Bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$

The Watchdog Timer is a 16-Bit timer, which is incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-Bit timer is realized as two concatenated 8-Bit timers. The upper 8 Bits of the Watchdog Timer can be preset to a user-programmable value via a watchdog service access in order to vary the watchdog expiring time. The lower 8 Bits are reset on each service access. **Figure 13** shows the block diagram of the watchdog timer unit.

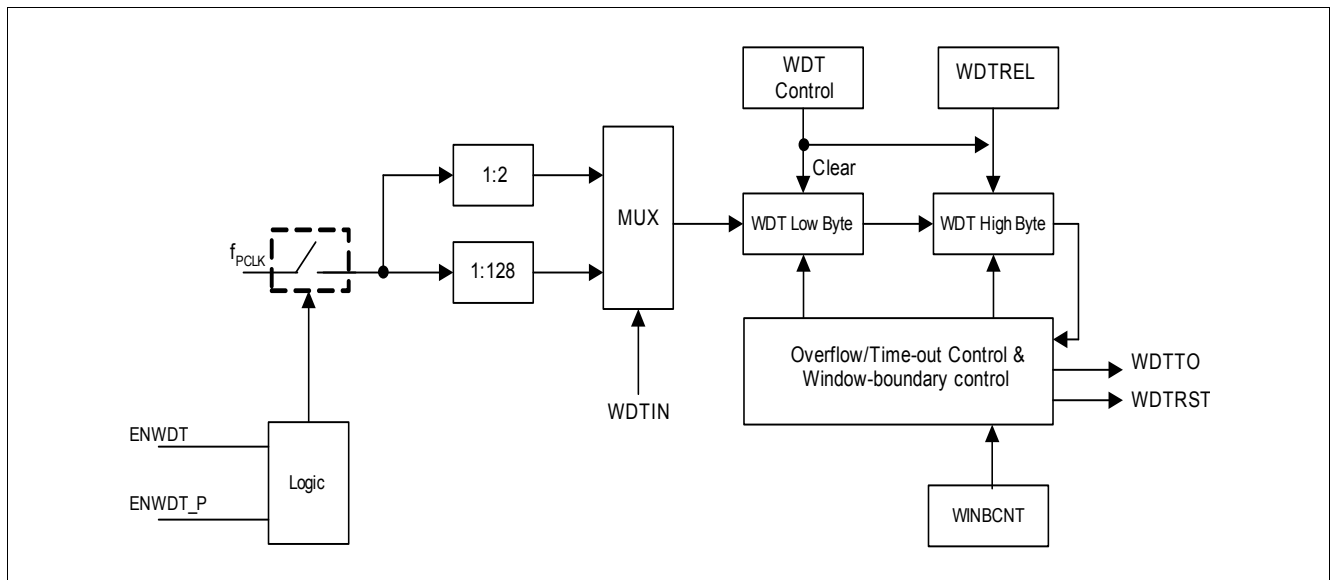


Figure 13 WDT Block Diagram

3.8 Interrupt System

The TLE9832-2 supports 14 interrupt vectors with four priority levels. Eleven of these interrupt vectors are assigned to the on-chip peripherals: Timer 0, Timer 1, UART, SSC and A/D Converter are each assigned to one dedicated interrupt vector; while Timer2, Timer21, MDU, LIN and the Capture/Compare Unit share six interrupt vectors.

Two interrupt vectors are assigned to the external interrupts. External interrupts 0 to 1 are each assigned to one dedicated interrupt vector, external interrupt 2 shares on interrupt vector with Timer21 and the MDU.

One interrupt vector is dedicated to the XINT interrupt events whose interrupt flags are also located in registers in XSFR area.

A non-maskable interrupt (NMI) with the highest priority is shared by the following:

- Watchdog Timer, warning before overflow
- MI_CLK Watchdog Timer overflow event
- PLL, loss of lock
- Flash, on operation complete, e.g. erase.
- OCDS, on user IRAM event
- Oscillator watchdog detection for too low oscillation of f_{OSC}
- Flash map error
- Uncorrectable ECC error on Flash, XRAM and IRAM
- VSUP supply pre warning when any supply voltage drops below or exceeds any threshold.

Figure 14, **Figure 15**, **Figure 16**, **Figure 17** and **Figure 18** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags. **Figure 19** gives the corresponding overview for the NMI sources.

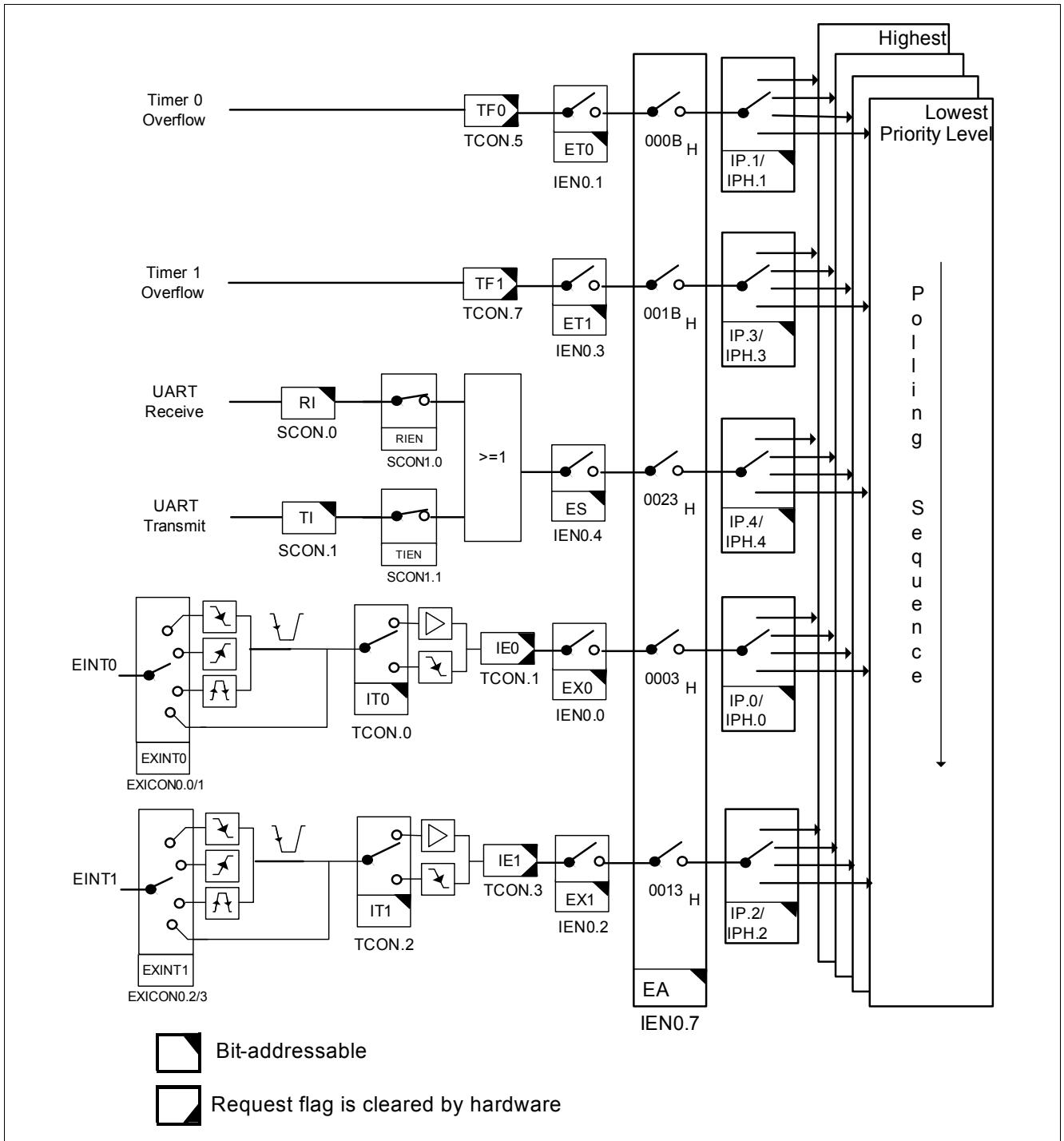


Figure 14 Interrupt Request Sources (Part 1)

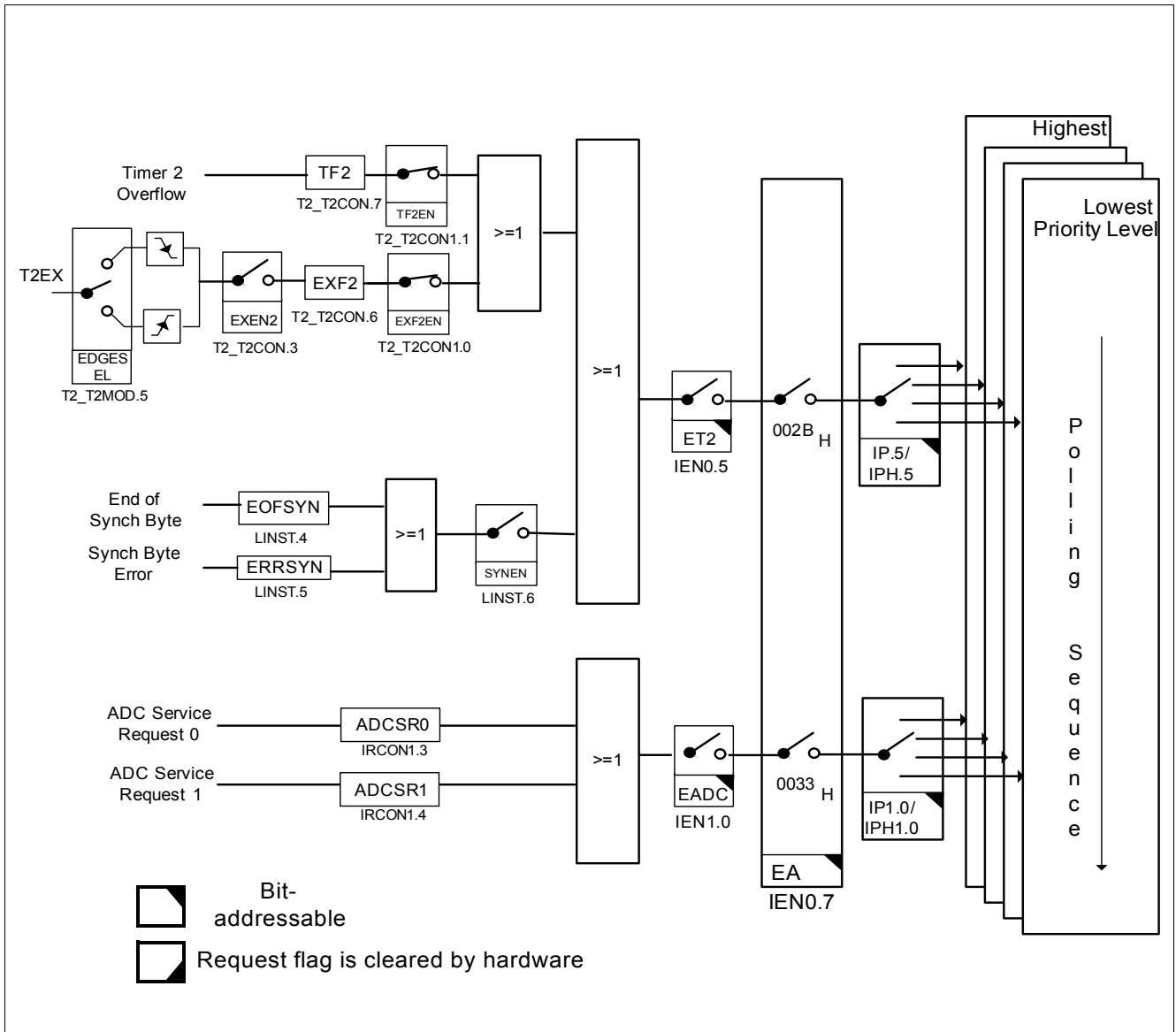


Figure 15 Interrupt Request Sources (Part 2)

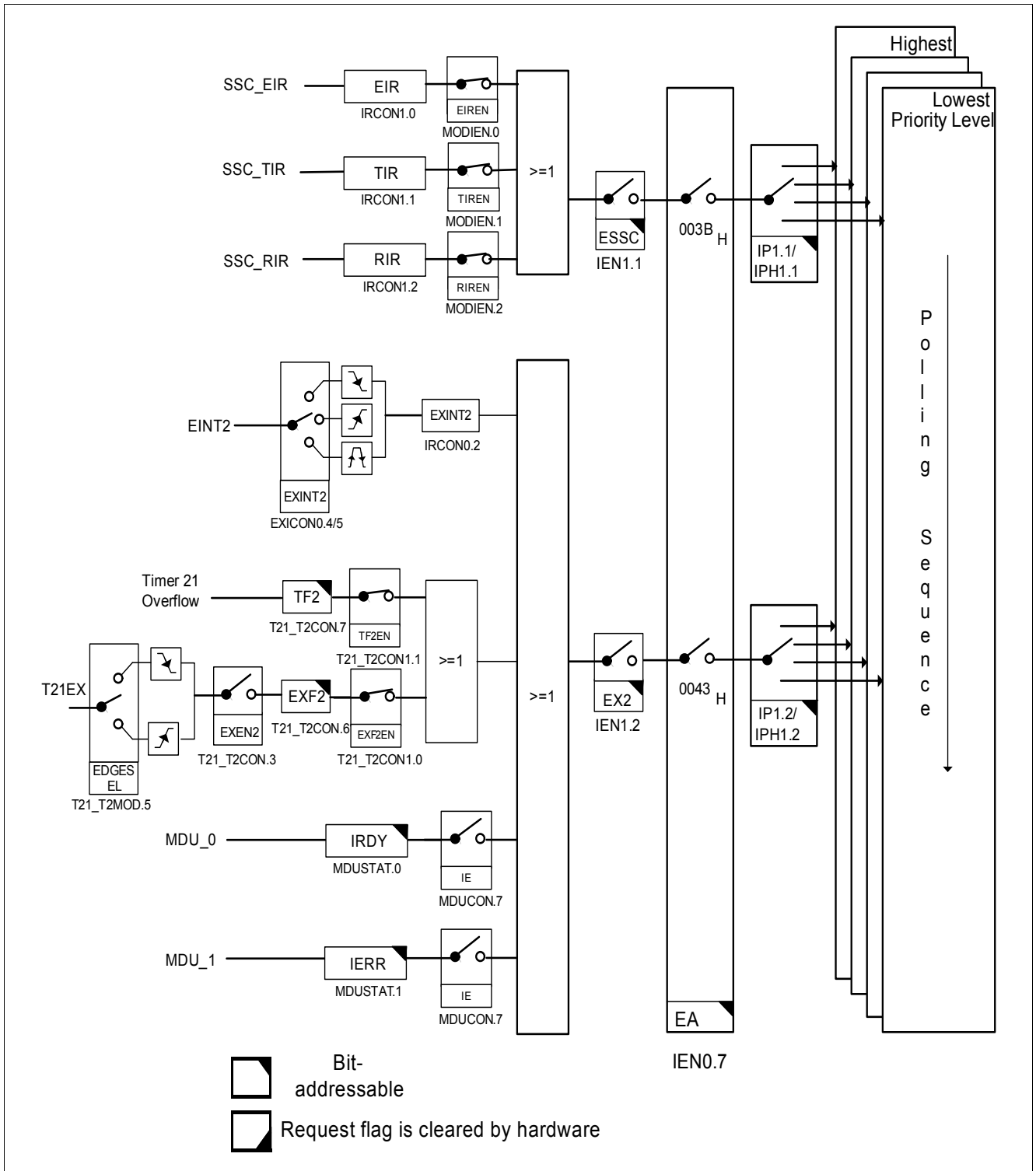


Figure 16 Interrupt Request Sources (Part 3)

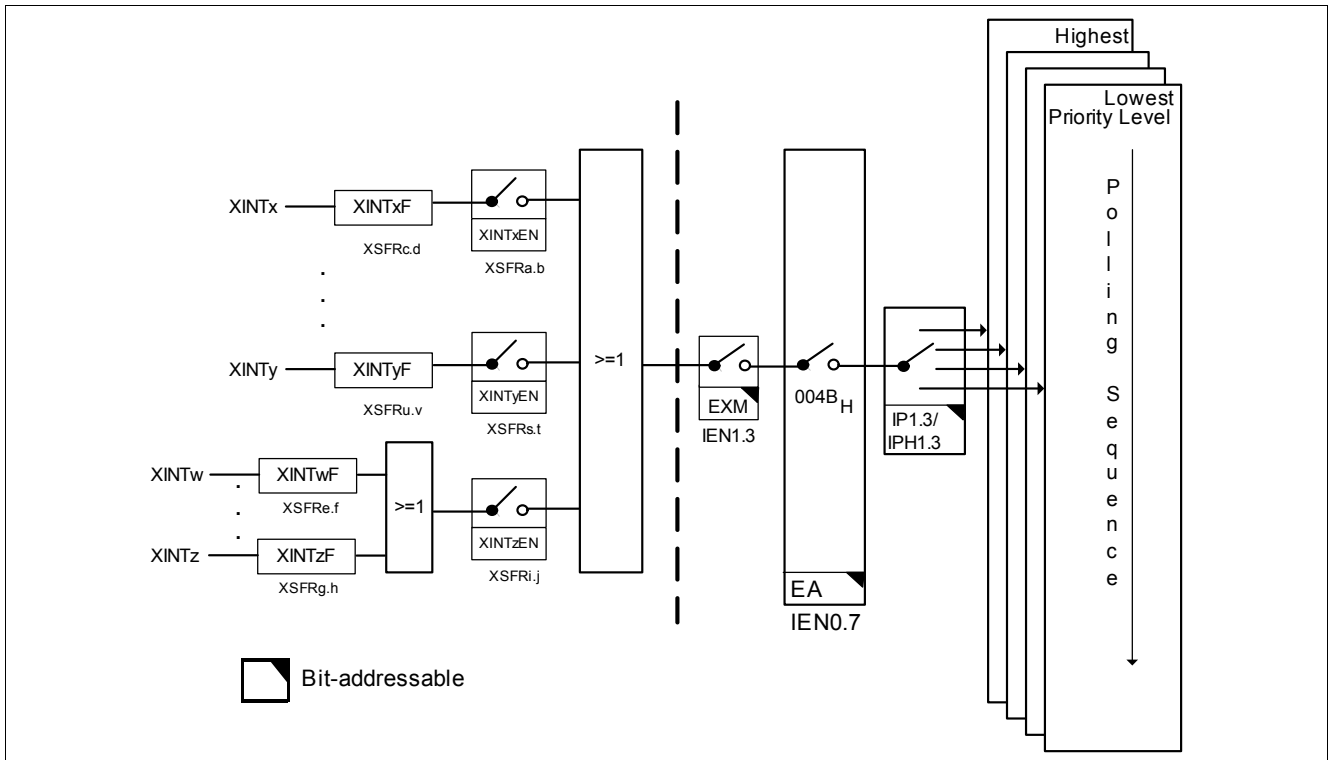


Figure 17 Interrupt Request Sources (Part 4)

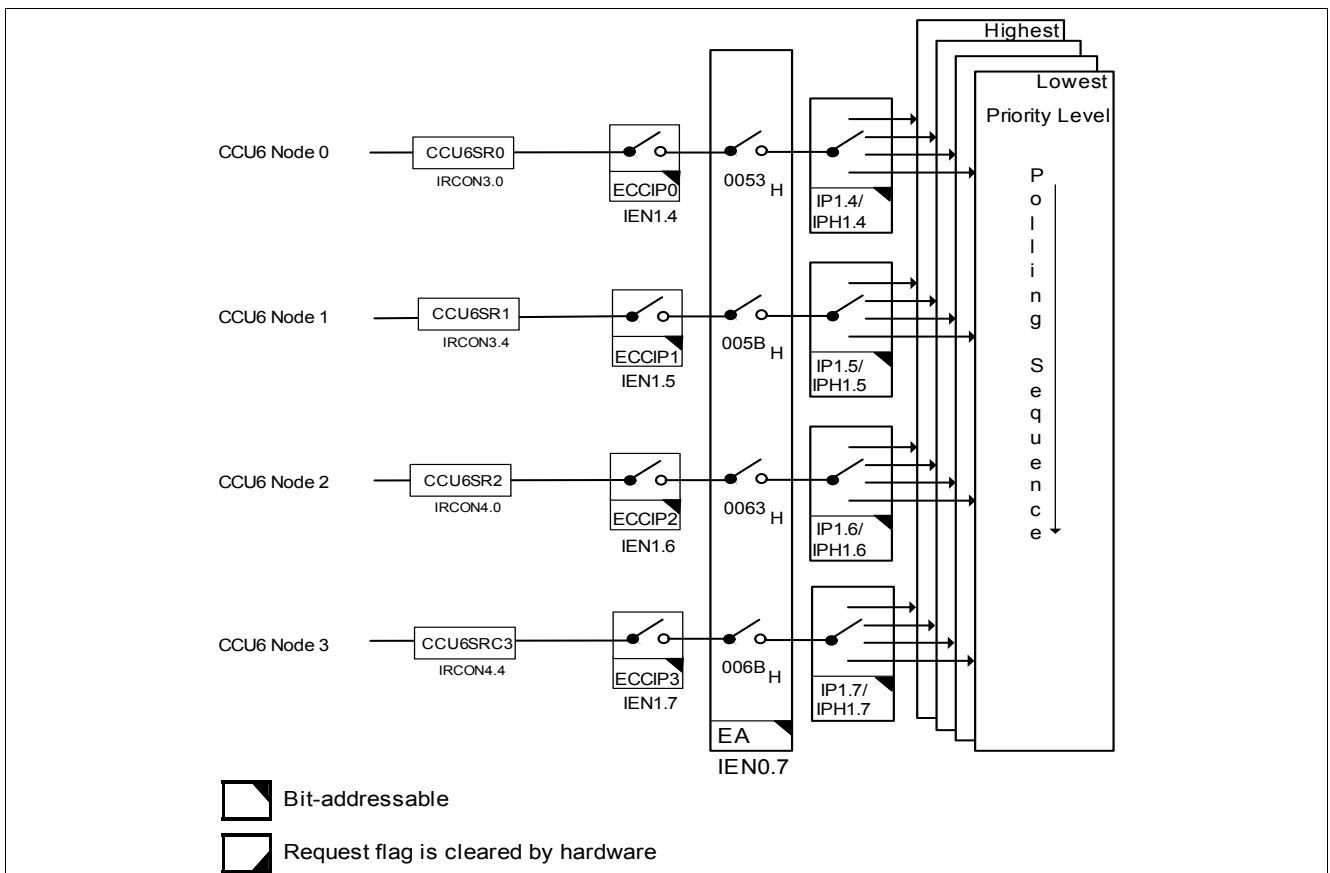


Figure 18 Interrupt Request Sources (Part 5)

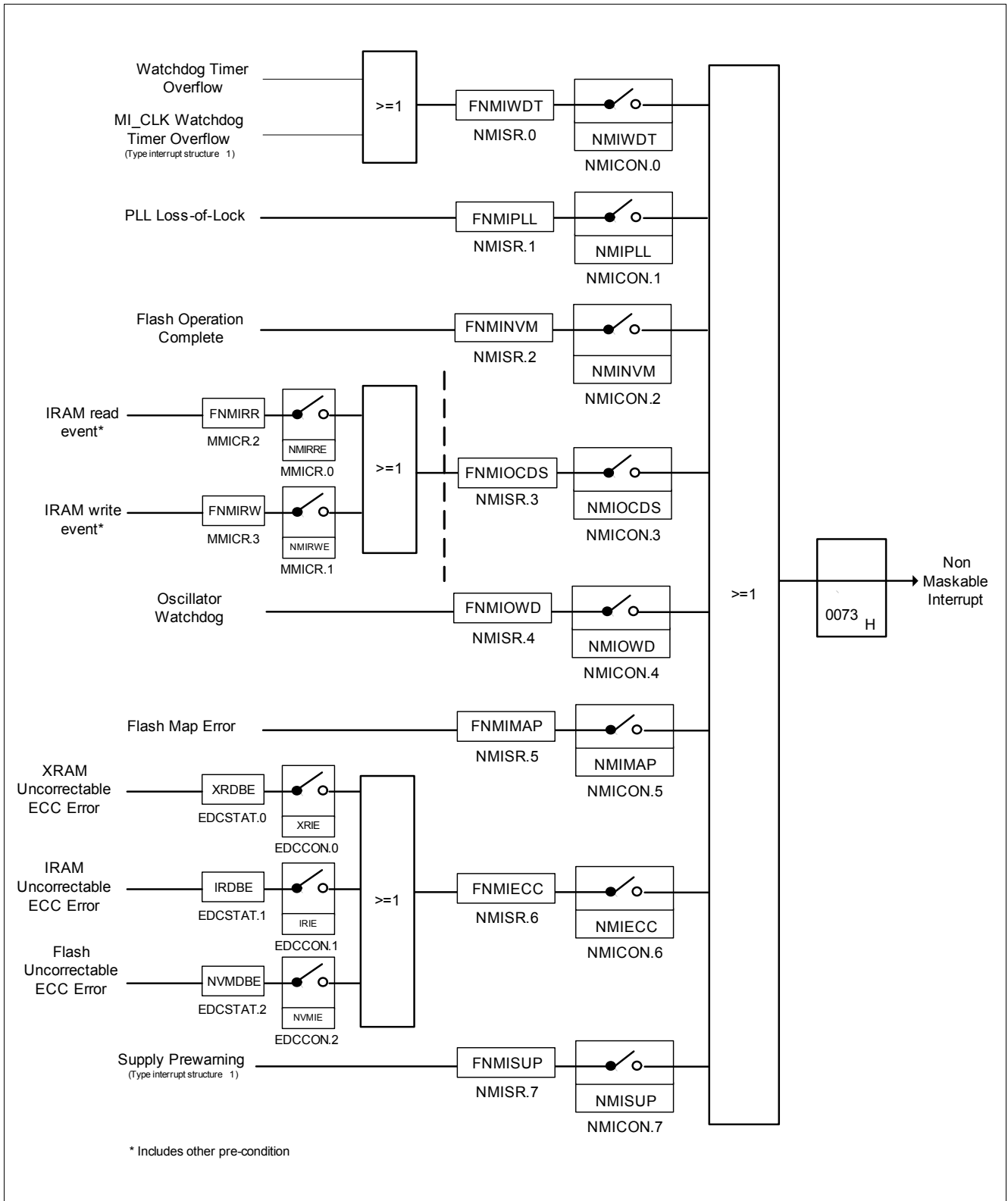


Figure 19 Non-Maskable Interrupt Request Source

3.9 Multiplication/Division Unit

The Multiplication/Division Unit (MDU) provides fast 16-Bit multiplication, 16-Bit and 32-Bit division as well as shift and normalize features. It has been integrated to support the TLE9832-2 core in real-time control applications, which require fast mathematical computations.

Features

- Fast signed/unsigned 16-Bit multiplication
- Fast signed/unsigned 32-Bit divide by 16-Bit and 16-Bit divide by 16-Bit operations
- 32-Bit unsigned normalize operation
- 32-Bit arithmetic/logical shift operations

3.10 Parallel Ports

The TLE9832-2 has 16 port pins organized into three parallel ports: Port 0 (P0), Port 1 (P1) and Port 2 (P2). Each port pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. P0 and P1 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected.

Bidirectional Port Features (P0, P1)

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

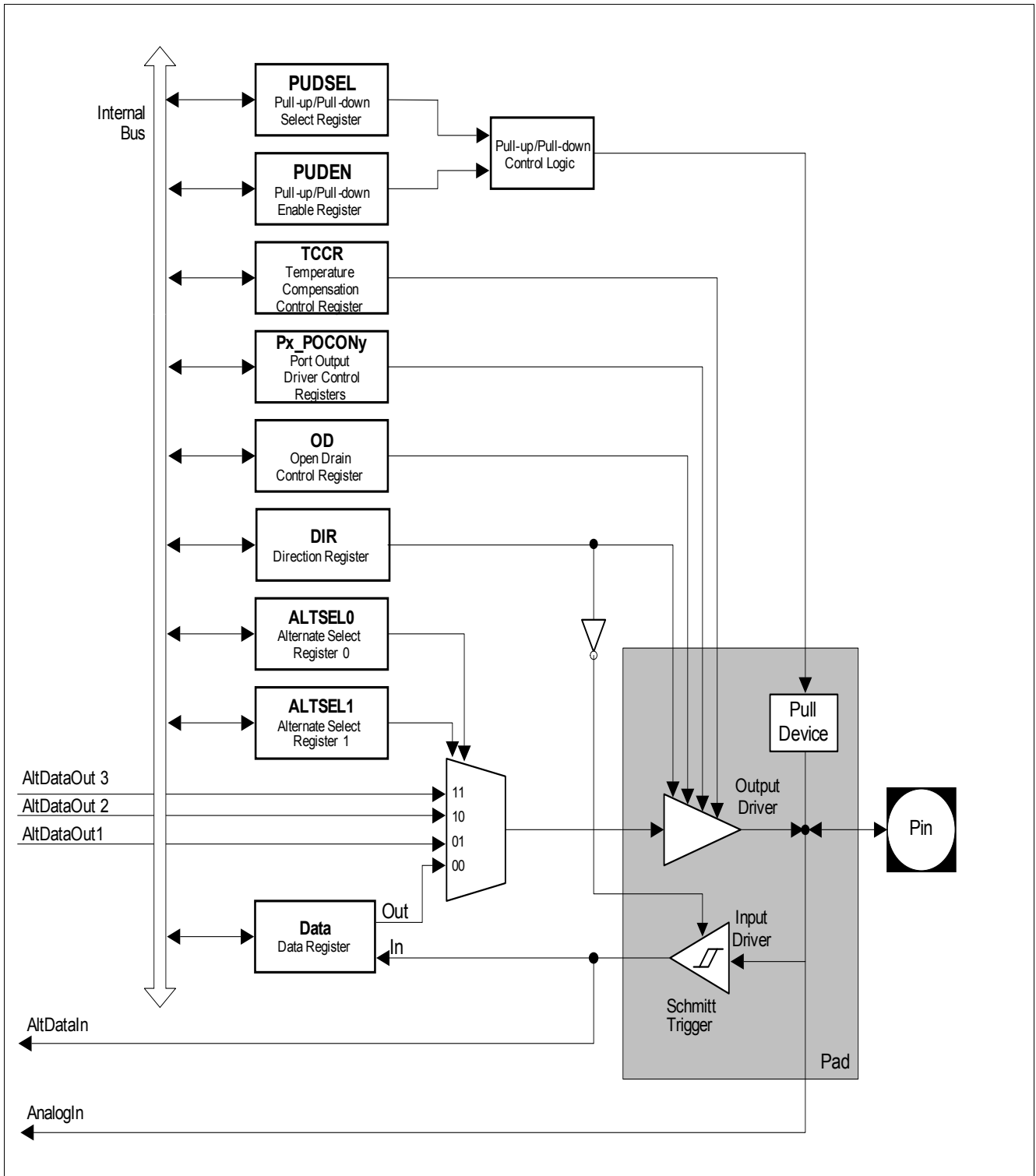


Figure 20 General Structure of a Bidirectional Port Pin

Figure 21 shows the structure of an input-only port pin. Each P2 pin can only function in input mode. Register P2_DIR is provided to enable or disable the input driver. When the input driver is enabled, the actual voltage level present at the port pin is translated into a logic 0 or 1 via a Schmitt-Trigger device and can be read via register. Each pin can also be programmed to activate an internal weak pull-up or pull-down device. The analog input (Analog In) bypasses the digital circuitry and Schmitt-Trigger device for direct feed-through to the ADC1 input channel.

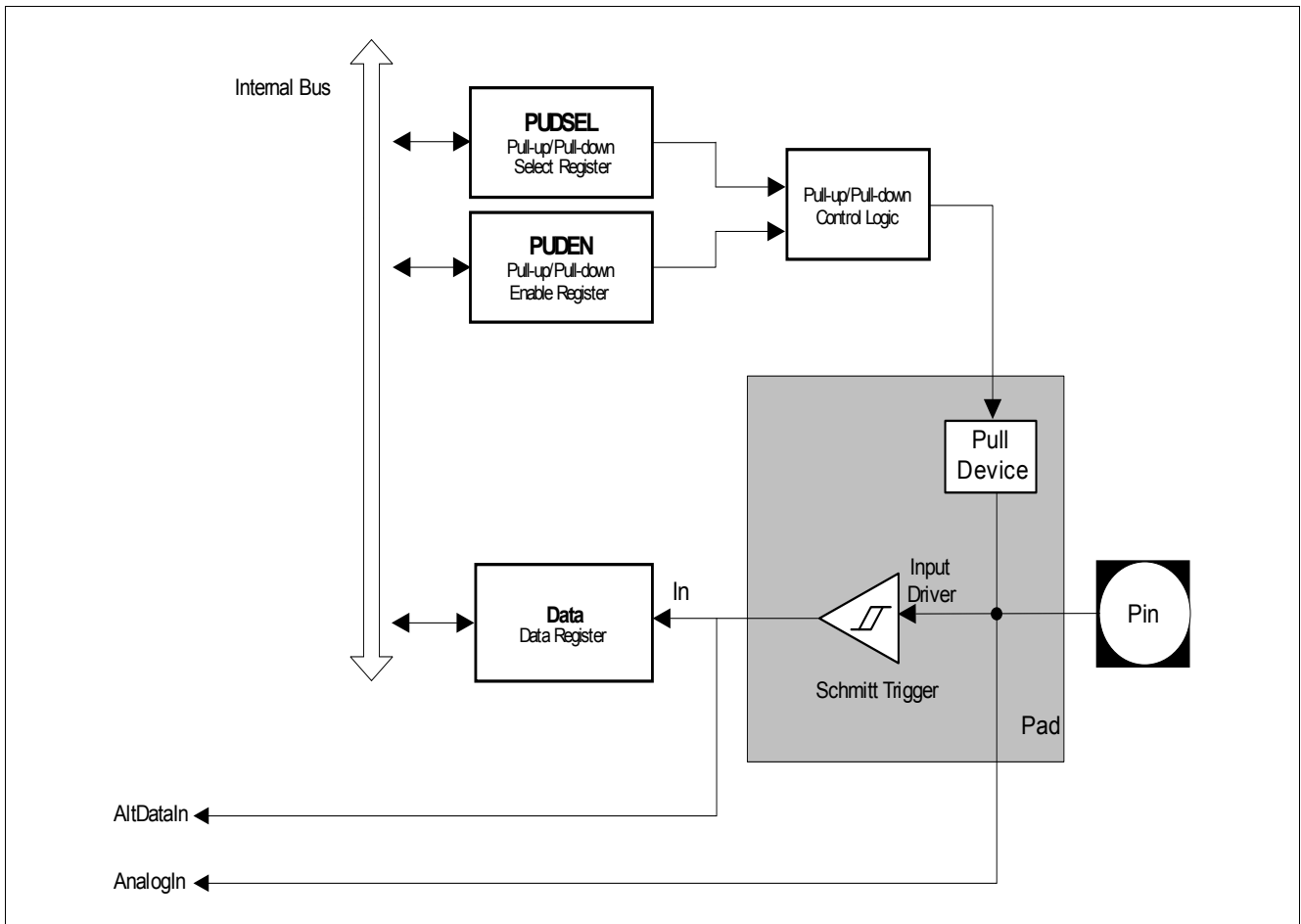


Figure 21 General Structure of an Input Port Pin

3.11 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both, timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented with every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at its respective external input pins, T0 or T1. Timer 0 and Timer 1 are fully compatible and can be configured in four different operating modes to use in a variety of applications, see [Table 6](#). In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 6 Timer 0 and Timer 1 Modes

| Mode | Operation |
|------|---|
| 0 | 13-Bit-timer The timer is essentially an 8-Bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices. |
| 1 | 16-Bit-timer The timer registers, TLx and THx, are concatenated to form a 16-Bit counter. |
| 2 | 8-Bit timer with auto-reload The timer register TLx is reloaded with a user-defined 8-Bit value in THx upon overflow. |
| 3 | Timer 0 operates as two 8-Bit timers The timer registers, TL0 and TH0, operate as two separate 8-Bit counters. Timer 1 is halted and retains its count even if enabled. |

3.12 Timer 2 and Timer 21

Timer 2 and Timer 21 are 16-Bit general purpose timers that are fully compatible and have two modes of operation, a 16-Bit auto-reload mode and a 16-Bit one channel capture mode, see [Table 7](#). As a timer, the timers count with an input clock of PCLK/12 (if prescaler is disabled). As a counter, they count 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is PCLK/24 (if prescaler is disabled).

Table 7 Timer 2 Modes

| Mode | Description |
|------------------------|---|
| Auto-reload | <p>Up/Down Count Disabled</p> <ul style="list-style-type: none"> • Count up only • Start counting from 16-Bit reload value, overflow at FFFF_H • Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well • Programmable reload value in register RC2 • Interrupt is generated with reload events. |
| Auto-reload | <p>Up/Down Count Enabled</p> <ul style="list-style-type: none"> • Count up or down, direction determined by level at input pin T2EX • No interrupt is generated • Count up <ul style="list-style-type: none"> – Start counting from 16-Bit reload value, overflow at FFFF_H – Reload event triggered by overflow condition – Programmable reload value in register RC2 • Count down <ul style="list-style-type: none"> – Start counting from FFFF_H, underflow at value defined in register RC2 – Reload event triggered by underflow condition – Reload value fixed at FFFF_H |
| Channel capture | <ul style="list-style-type: none"> • Count up only • Start counting from 0000_H, overflow at FFFF_H • Reload event triggered by overflow condition • Reload value fixed at 0000_H • Capture event triggered by falling/rising edge at pin T2EX • Captured timer value stored in register RC2 • Interrupt is generate with reload or capture event |

3.13 Timer 3

Timer 3 can function as timer or counter. When functioning as a timer, Timer 3 is incremented in periods based on the system clock. When functioning as a counter, Timer 3 is incremented in response to a 1-to-0 transition (falling edge) at its respective input. Timer 3 can be configured in four different operating modes to use in a variety of applications, see [Table 8](#).

Table 8 Timer 3 Modes

| Mode | Sub-Mode | Operation |
|------|----------|---|
| 0 | - | 13-Bit Timer The timer is essentially an 8-Bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices. |
| 1 | a | 16-Bit Timer The timer registers, TLx and THx, are concatenated to form a 16-Bit counter. |
| 1 | b | 16-Bit Timer The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable a single shot measurement on a preset channel with the measurement unit. |
| 1 | c | 16-Bit Timer The timer registers, TLx and THx, are concatenated to form a 16-Bit counter, which is triggered by the PWM Unit to enable the LIN Baudrate Measurement. |
| 2 | - | 8-Bit Timer with Auto-reload The timer register TLx is reloaded with a user-defined 8-Bit value in THx upon overflow. |
| 3 | a | Timer 3 operates as Two 8-Bit Timers The timer registers, TL3 and TH3, operate as two separate 8-Bit counters. |
| 3 | b | Timer 3 operates as Two 8-Bit Timers The timer registers, TL3 and TH3, operate as two separate 8-Bit counters. In this mode the 100 kHz Low Power Clock can be measured. TL3 acts as an edge counter for the clock edges and TH3 as an counter which counts the time between the edges. |

3.14 Capture/Compare Unit 6 (CCU6)

The CCU6 unit is made up of a Timer T12 block with three capture/compare channels and a Timer T13 block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status Bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6). A capture/compare channel inside this module is named CC6x.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for High Side and Low Side Switches)
- 16-Bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Multiple interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-Bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for brushless DC-drives implemented
- Position detection via hall sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

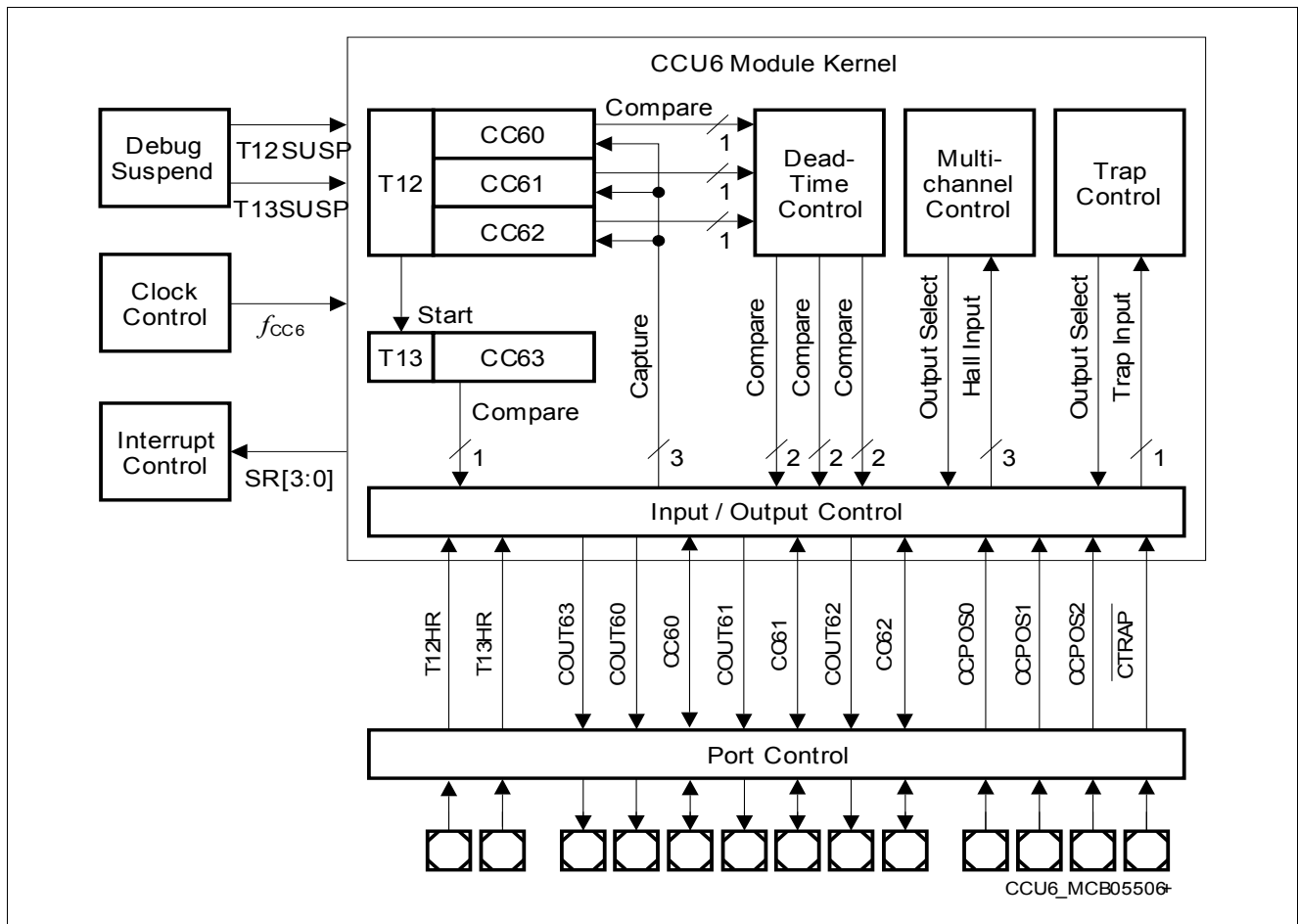


Figure 22 CCU6 Block Diagram

3.15 UART

The UART provides a full-duplex asynchronous receiver/transmitter, i.e. it can transmit and receive simultaneously. It is also receive-buffered, i.e. it can commence reception of a second Byte before a previously received Byte has been read from the receive register. However, if the first Byte still has not been read by the time reception of the second Byte is complete, one of the Bytes will be lost. The serial port receive and transmit registers are both accessed at Special Function Register (SFR) SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

UART Features

- Full-duplex asynchronous modes
 - 8-Bit or 9-Bit data frames, LSB first
 - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception
- Baud-rate generator with fractional divider for generating a wide range of baud rates
- Hardware logic for break and synch Byte detection

UART Modes

The UART can be used in four different modes. In mode 0, it operates as an 8-Bit shift register. In mode 1, it operates as an 8-Bit serial port. In modes 2 and 3, it operates as a 9-Bit serial port. The only difference between mode 2 and mode 3 is the baud rate, which is fixed in mode 2 but variable in mode 3. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator.

The different modes are selected by setting Bits SM0 and SM1 to their corresponding values, as shown in [Table 9](#).

Table 9 UART Modes

| SM0 | SM1 | Operating Mode | Baud Rate |
|-----|-----|------------------------------|---------------|
| 0 | 0 | Mode 0: 8-Bit shift register | $f_{PCLK}/2$ |
| 0 | 1 | Mode 1: 8-Bit shift UART | Variable |
| 1 | 0 | Mode 2: 9-Bit shift UART | $f_{PCLK}/64$ |
| 1 | 1 | Mode 3: 9-Bit shift UART | Variable |

3.16 LIN Transceiver

The LIN module is a transceiver for the Local Interconnect Network (LIN) compliant to the standards LIN 1.3, LIN 2.0 and LIN 2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kbps and 20 kbps. Additionally baud rates up to 40 kbaud are implemented.

The LIN module offers several different operation modes, including a Sleep Mode and the normal operation mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115 kbaud is also implemented.

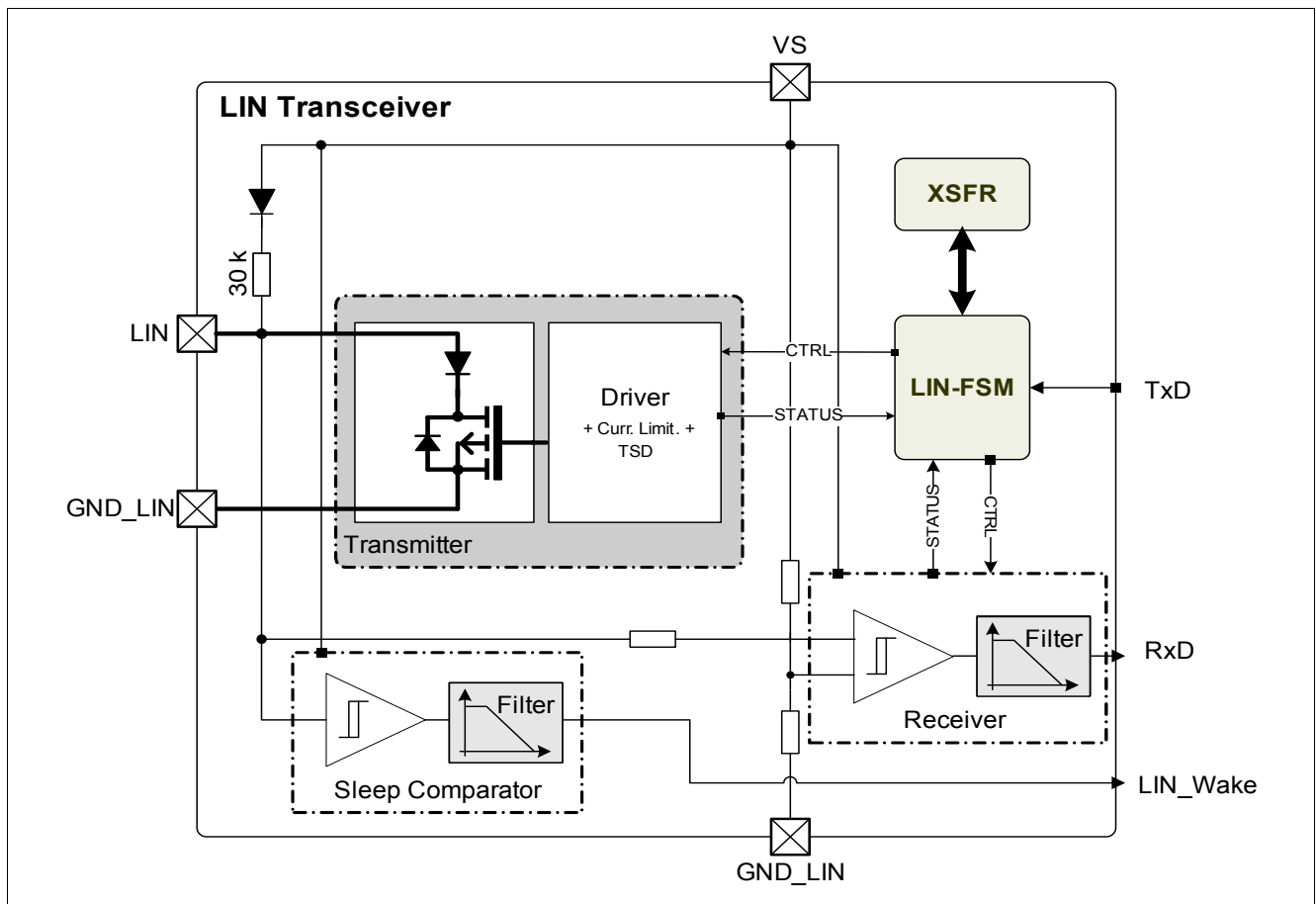


Figure 23 LIN Transceiver Block Diagram

3.17 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-Bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features

- Master and slave mode operation
 - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format

- Programmable number of data Bits: 2 to 8 Bits
- Programmable shift direction: LSB or MSB shift first
- Programmable clock polarity: idle low or high state for the shift clock
- Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

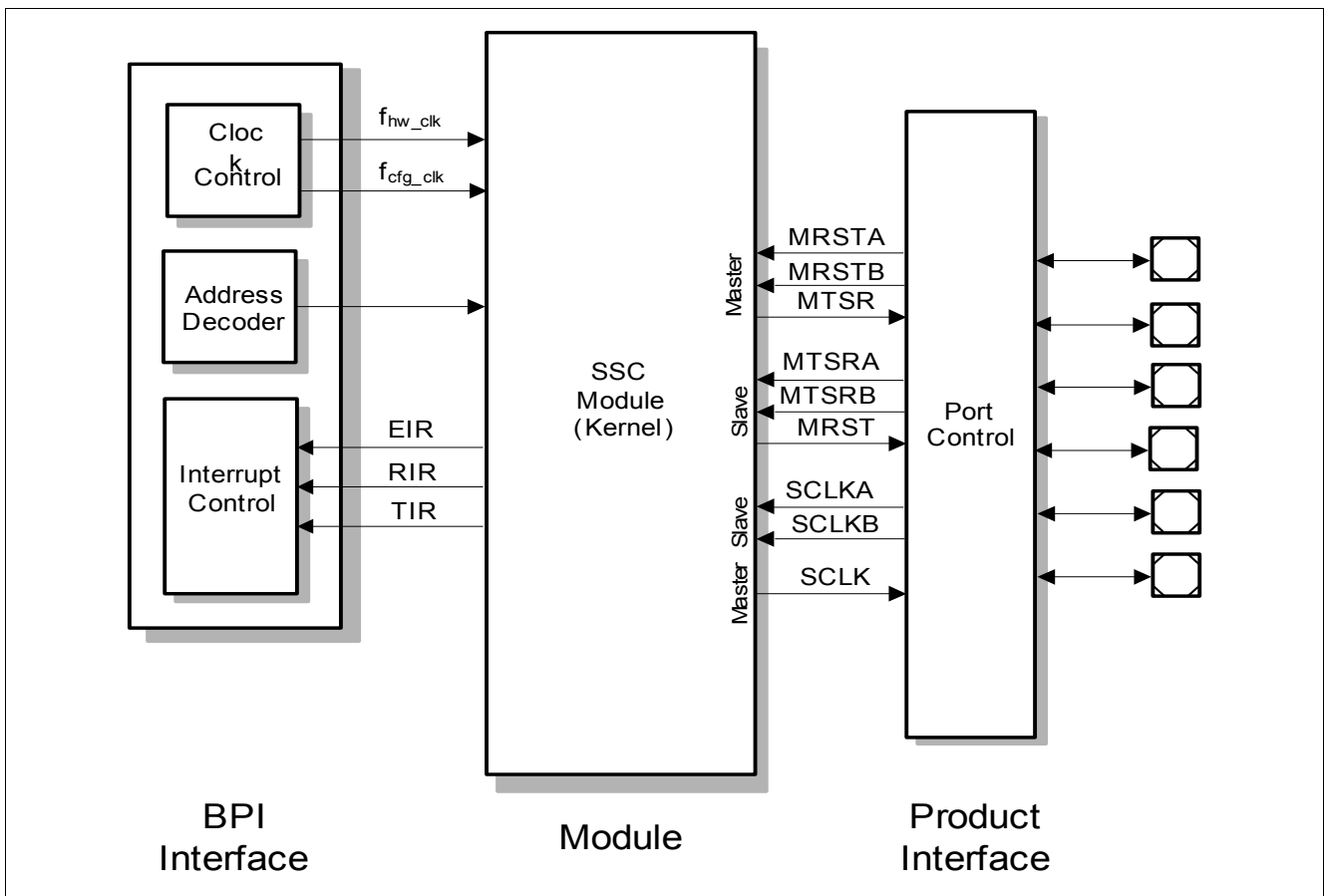


Figure 24 SSC Interface Diagram

3.18 Measurement Unit

The measurement unit is a functional unit that comprises the following associated sub-modules:

- 1 x 8 Bit ADC (ADC2) with 10 inputs. 5 are for single ended input signals and 5 are for differential input signals.
- Monitoring inputs voltage attenuators with two selectable attenuation settings: divide by 4 and divide by 6
- Supply voltage attenuators with attenuation of VBAT_SENSE, VS, VDDP and VDDC.
- VBG monitoring of 8-Bit ADC (ADC2) to guarantee functional safety requirements.
- Low Side Switch current sensing of LS1 and LS2. Allows a scalable overcurrent pre warning.
- Temperature sensor for monitoring the chip temperature and Low Side Switches temperature.
- Supplement block with reference voltage generation, bias current generation, voltage buffer for Flash reference voltage, voltage buffer for analog module reference voltage and test interface.

Table 10 Measurement functions and associated modules

| Module Name | Modules | Functions |
|--|---|--|
| Central Functions Unit | Bandgap reference circuit | The bandgap-reference sub-module provides two reference voltages 1. a trimmable reference voltage for the 8-Bit ADC. A local dedicated bandgap circuit is implemented to avoid deterioration of the reference voltage arising e.g. from crosstalk or ground voltage shift. 2. the reference voltage for the Flash module |
| 8-Bit ADC (ADC2) | 8-Bit ADC module with 10 multiplexed inputs | 1. 5 single-ended inputs 0 ... 1.23V 2. 5 differential inputs 0 ... 1.23V (allocation see following overview figure) |
| 10-Bit ADC (ADC1) | 10-Bit ADC module including analog test bus interface - part of μ C subsystem | 1. VBAT_SENSE measurement on channel 0 of ADC1. 2. VS measurement on channel 2 of ADC1. 3. MONx measurement on channel 6 of ADC1. 4. 5 additional (5V) analog inputs from Port 2. |
| Supply Voltage Attenuator | Resistive supply voltage attenuator | Scales down the supply voltages of the system to the input voltage range of ADC1 and ADC2. |
| Monitoring Input Attenuator | Resistive attenuator for (HV) | Scales down 5 monitoring input voltages to the input voltage range of the ADC1. |
| Central Temperature - Low Side Switch Temperature Sensor | Temperature sensor readout with two multiplexed ΔV_{be} sensing elements | Generates outputs voltage which is a linear function of the local chip (junction) temperature. |
| Measurement Core Module | Digital signal processing and ADC control unit | 1. Generates the control signal for the 8-Bit ADC2 and the synchronous clock for the switched capacitor circuits, 2. Performs digital signal processing functions and provides status outputs for interrupt generation. |

The structure of the measurement functions module is shown in [Figure 29](#).

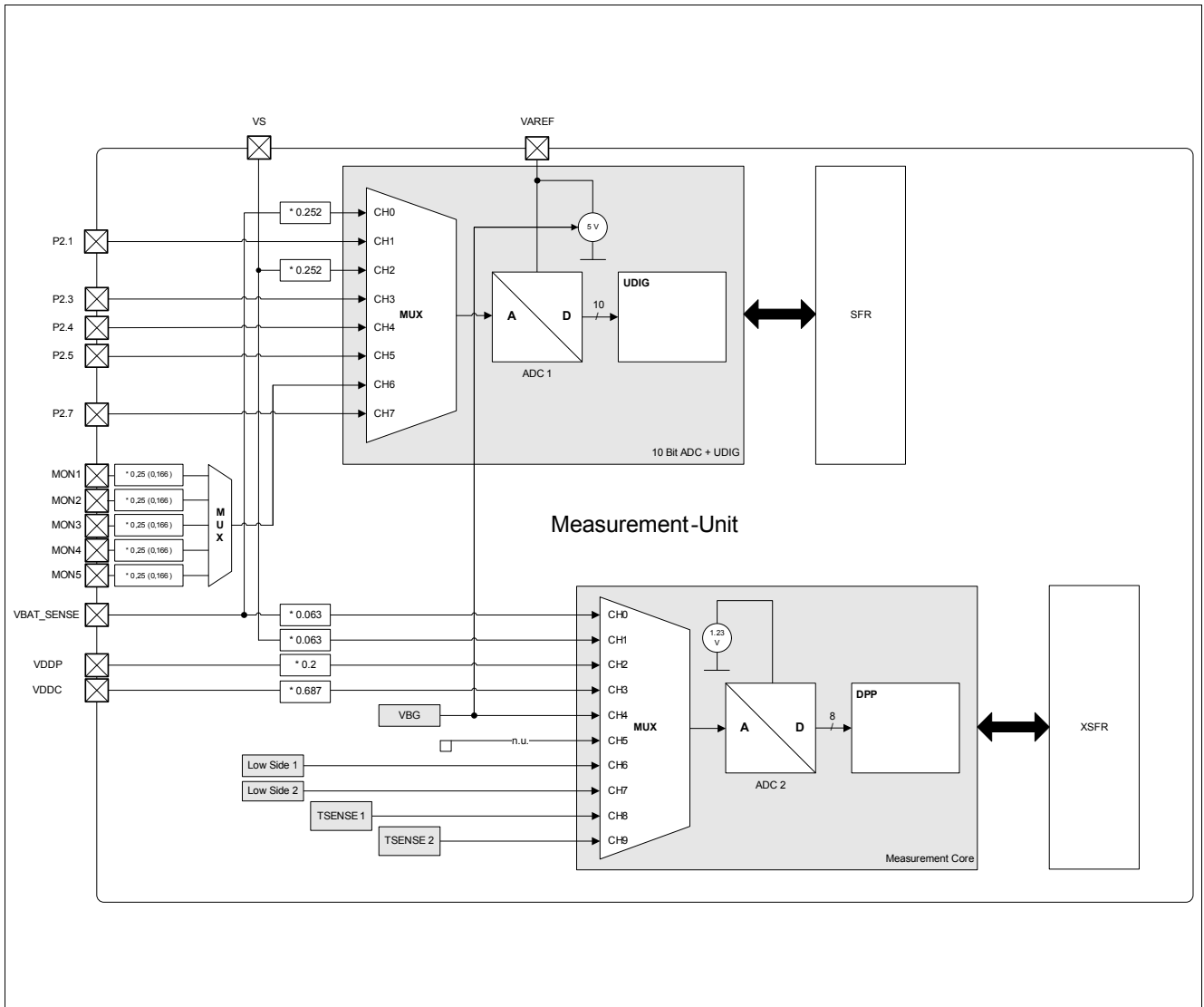


Figure 25 TLE9832-2 Measurement Unit-Overview

3.19 Measurement Core Module (incl. ADC2)

The basic function of this block is the digital postprocessing of several analog digitized measurement signals by means of filtering, level comparison and interrupt generation. The measurement postprocessing block is built of ten identical channel units attached to the outputs of the 10-channel 8-Bit ADC (ADC2). It processes ten channels, where the channel sequence and prioritization is programmable within a wide range.

Features

- 10 individually programmable channels split into two groups of user configurable and non user configurable
- Individually programmable channel prioritization scheme for measurement unit
- Two independent filter stages with programmable low-pass and time filter characteristics for each channel
- Two channel configurations:
 - Programmable upper- and lower trigger thresholds comprising a fully programmable hysteresis
 - Two individually programmable trigger thresholds with limit hysteresis settings
- Individually programmable interrupts and status for all channel thresholds

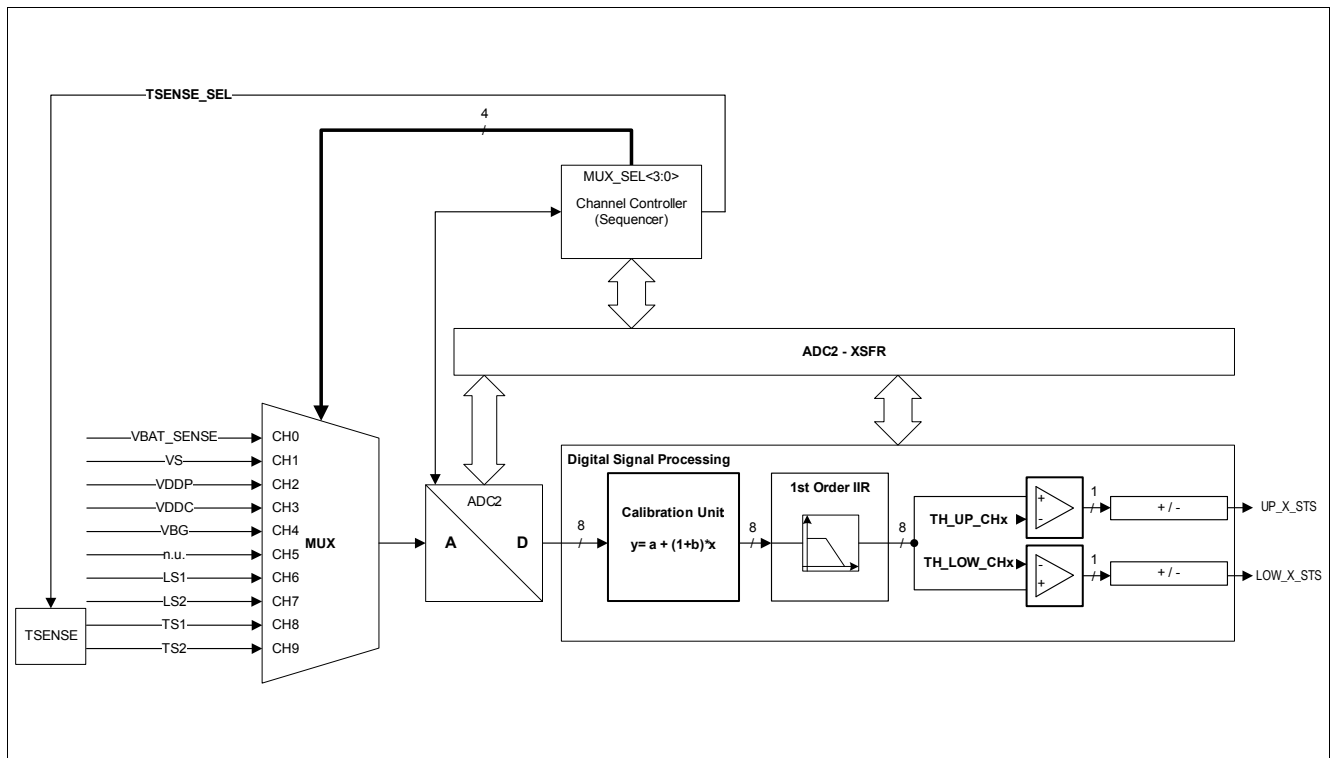


Figure 26 Measurement Core Module Block Diagram

3.20 Analog Digital Converter (ADC1)

The TLE9832-2 includes a high-performance 10-Bit Analog-to-Digital Converter (ADC1) with eight multiplexed analog input channels. The ADC1 uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC1 are available at AN1, AN3 - AN5, AN7.

Features

- Successive approximation
- 8-Bit or 10-Bit resolution
- 8 analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.21 High Voltage Monitor Input

This module is dedicated to monitor external voltage levels above or below a specified threshold or it can be used to detect a wake-up event at each high-voltage MON_IN pin in low-power mode. Each input is sensitive to an input level monitoring. It is available when the module is switched to Active Mode via the MON_int (internal signal name) output with a small filter delay of typical 2 μ s.

Features

- High-voltage input with $V_S/2$ threshold voltage
- Edge sensitive wake capability for power saving modes
- Level sensitive wake-up feature configurable for transitions from low to high, high to low or both directions
- MON inputs can also be evaluated with ADC1 in Active Mode, using adjustable threshold values (see also [Chapter 3.20](#)).

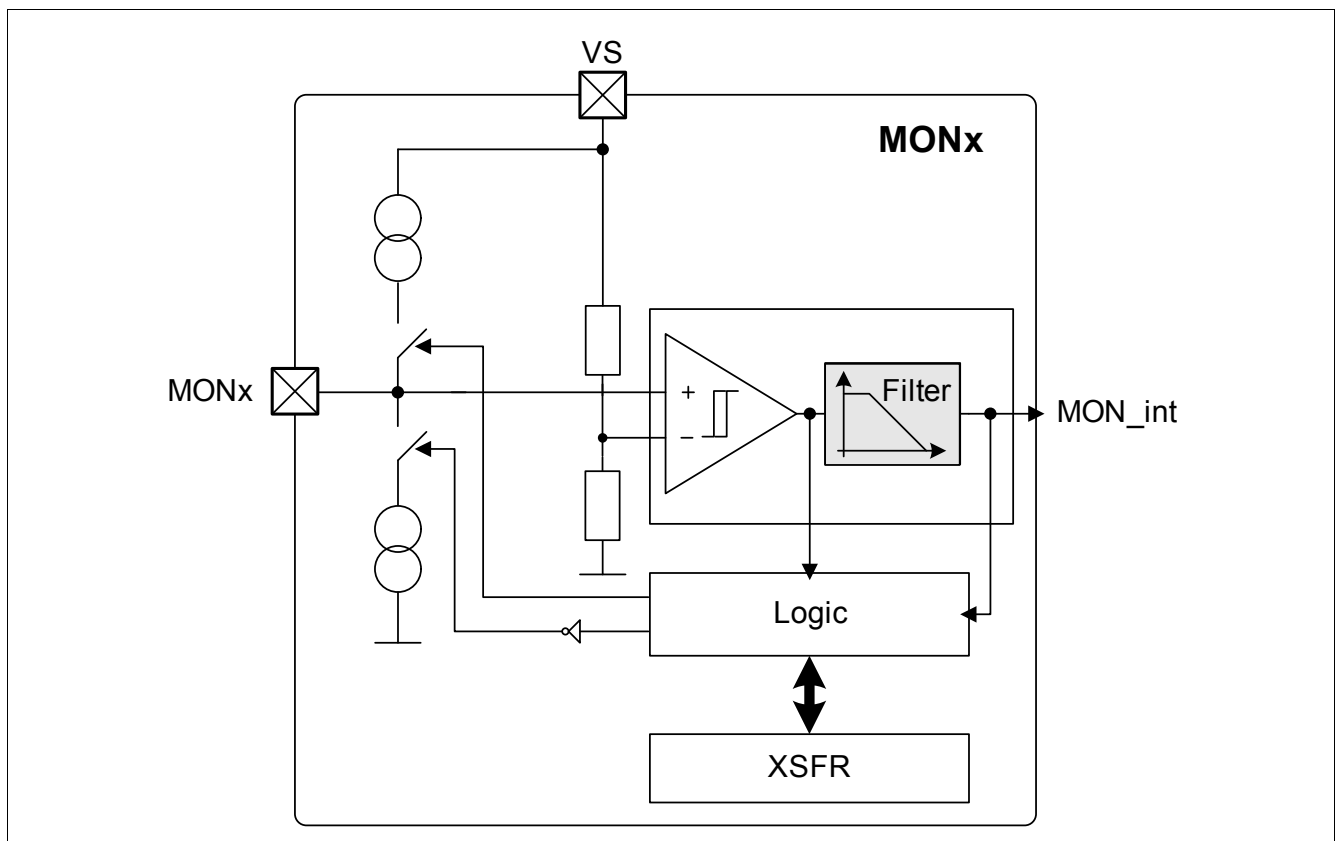


Figure 27 Monitoring Input Block Diagram

3.22 High Side Switches

The High Side Switches are intended for resistive load connections (only small line inductance are allowed) leaving the ECU board. Typical applications are single or multiple LEDs of a dashboard or switch illumination or other loads that require a High Side Switch.

A cyclic switch activation during Sleep Mode or Stop Mode of the system is also available.

Features

- Multi purpose High Side Switch for resistive load connections (only small line inductances are allowed)
- Over-current detection with thresholds: 8 mA (also used for on-state Open Load detection), 50 mA, 100 mA, 150 mA
- Cyclic switch activation in Sleep Mode and Stop Mode for cyclic sense support with reduced driver capability: max. 40 mA
- Open load detection in off mode with two different thresholds: Ground (0 V, for functional safety) and $0.67 \cdot V_S$
- Off-state open load detection operates with two different test currents: 75 μA and 750 μA
- PWM capability up to 25 kHz (with disabled slew rate control only)
- Robust output for off ECU connection
- Slew rate control
- Selectable PWM source: PWM-Unit or CCU6

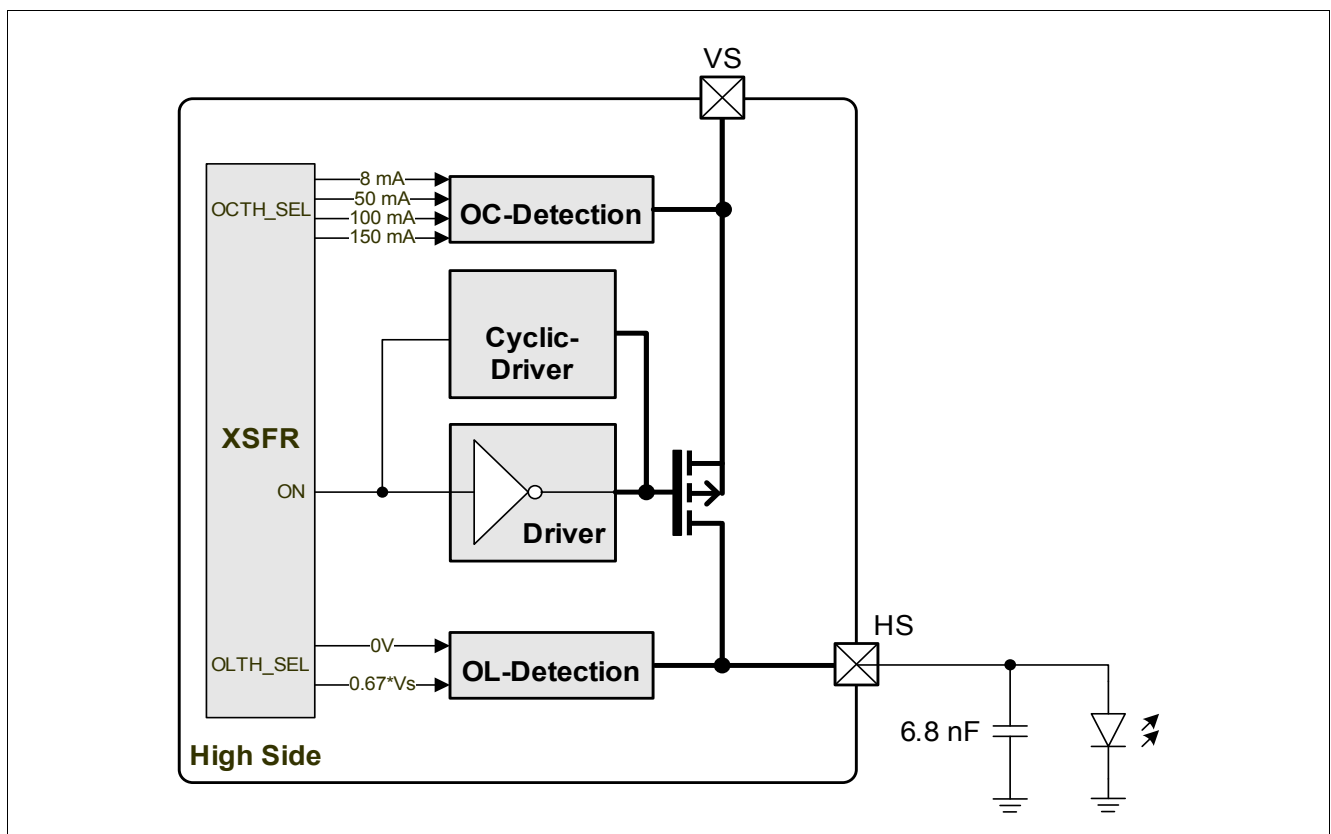


Figure 28 High Side Switch Module Block Diagram

3.23 Low Side Switches

The general purpose Low Side Switches are intended to control an on-board relay. They include an over-current detection function. The module is designed for on-board connections.

Features

- Multi purpose Low Side Switch
 - configurable over-current protection with automatic shutdown
 - configurable over-temperature protection with automatic shutdown
- Intended for relay driver
 - PWM relay driver
 - simple relay driver
- Integrated clamping
- PWM capability up to 25 kHz
- Selectable PWM source: PWM-Unit or CCU6

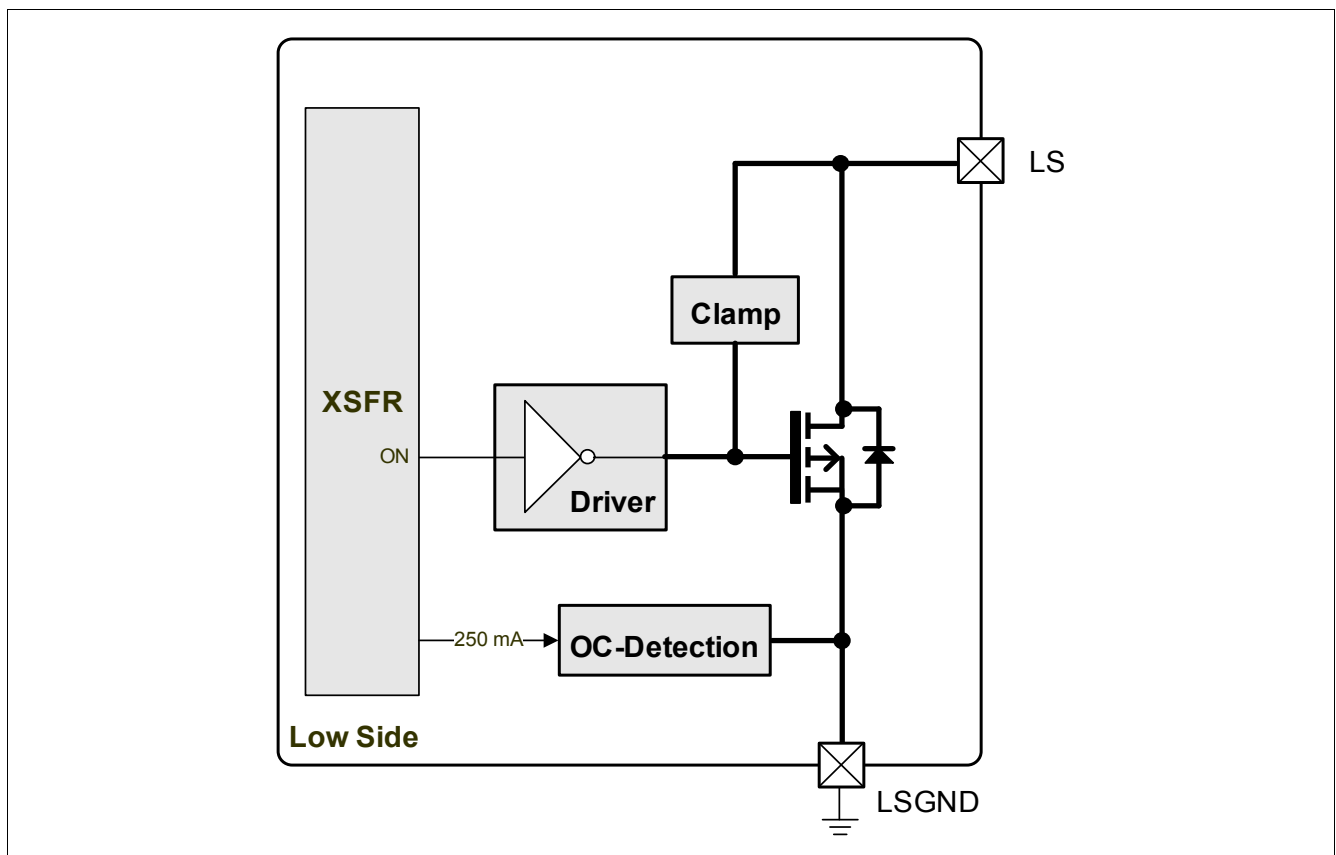


Figure 29 Module Block Diagram

3.24 PWM Generator

The PWM generator provides up to two configurable PWM channels in order to drive the Low Side Switches LS1, LS2 and the High Side Switches HS1 and HS2 in a PWM mode.

Features

- Programmable modulation frequency per channel
- Programmable duty-cycle per channel with glitch-free reprogramming
- PWM frequency up to 25 kHz
- Duty-cycle resolution from 0 % ... 100 % in steps of 0.5 %

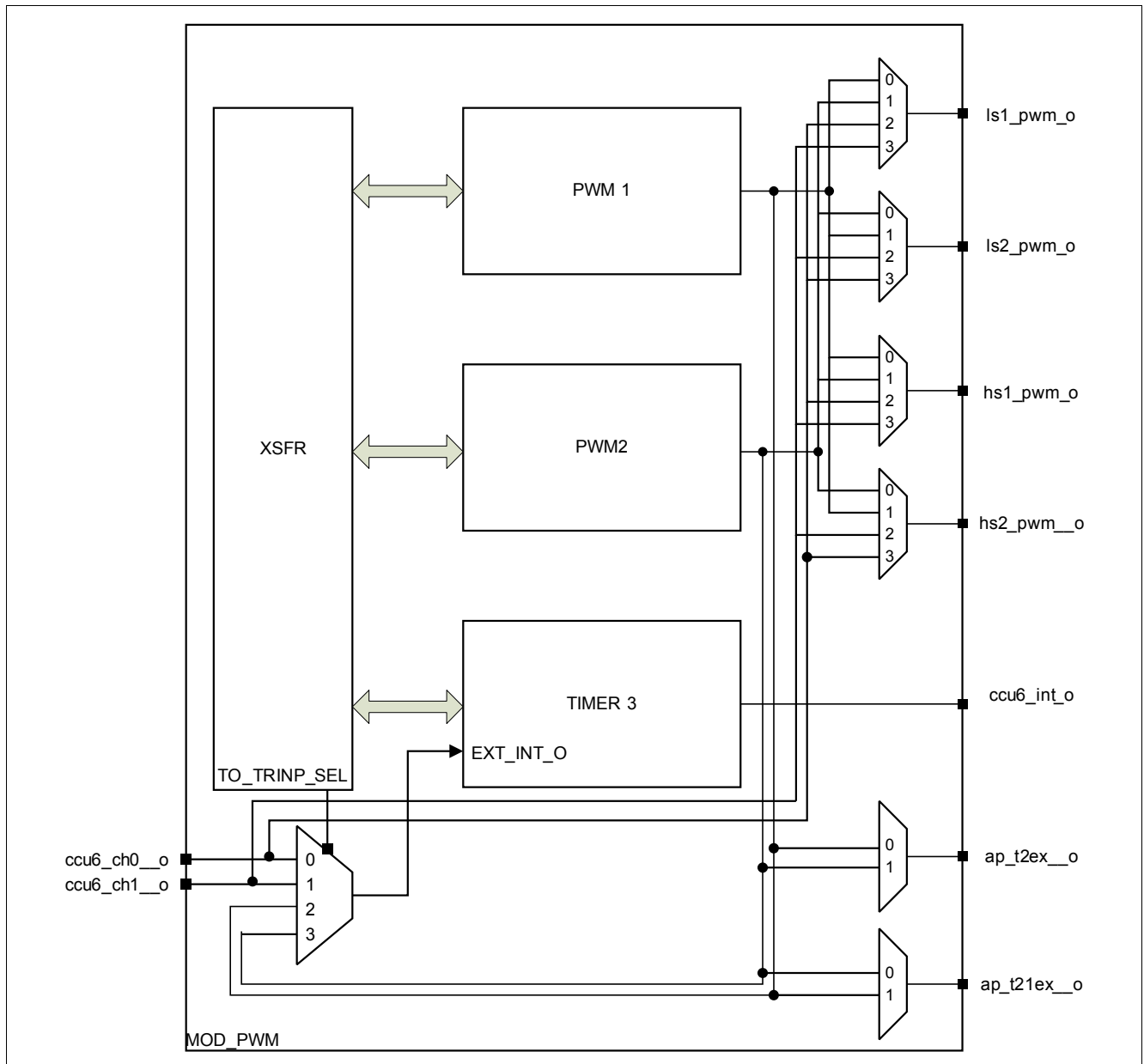


Figure 30 Module Block diagram of PWM module and included PWM switching matrix

3.25 Debug System

The On-Chip Debug Support (OCDS) provides the basic functionality required for software development and debugging of XC800 based systems. The OCDS design is based on the following principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a monitor program
- Use standard interfaces to communicate with the Host (a debugger)

Features

- Set breakpoints on instruction address and on address range within the program memory
- Set breakpoints on internal RAM address range
- Support unlimited amount of software breakpoints in Flash / RAM code region
- Step through the program code

The Monitor Mode Control (MMC) block at the center of the OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals. After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work data and monitor stack). The OCDS system is accessed through the DAP, which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated TMS pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after TLE9832-2 has been started in OCDS mode.

4 Application Information

4.1 Electric Drive Application

Figure 31 shows the TLE9832-2 in an electric drive application setup controlling a DC-brush motor. The two Low Side Switches are controlling a relay each. An external FET allows to control the window lift motor with a PWM signal as generated with the CCU6 module of the microcontroller.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

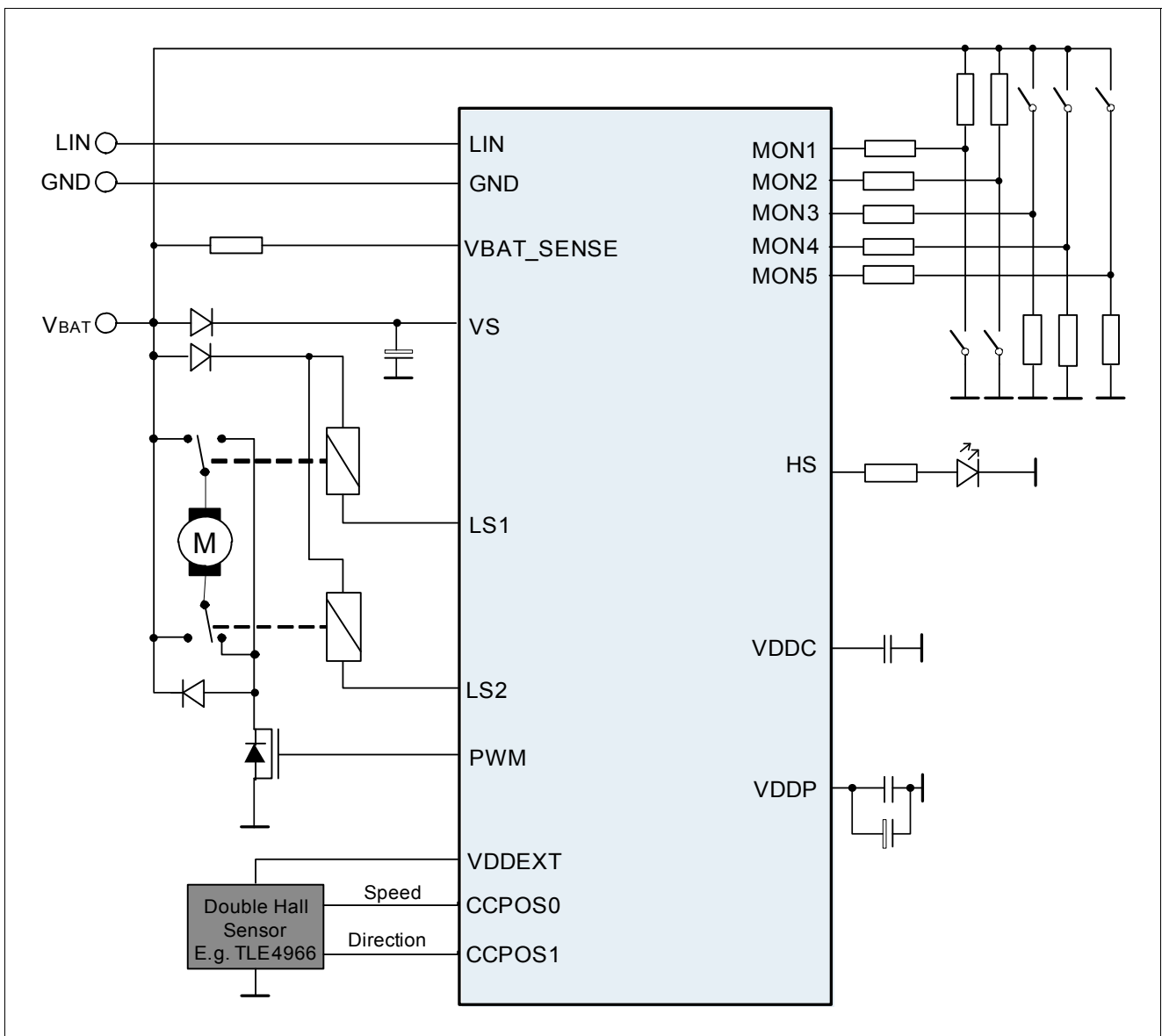


Figure 31 Simplified Application Diagram

4.2 Connection of N.C. Pins

It is recommended to connect N.C. pins to GND unless otherwise specified. Since pins 10 and 46 are located next to high voltage pins (VS, MON5, LS1) these 2 N.C. pins can be also left unconnected in order to avoid huge current flow and damage of the system in case of short-circuit.

4.3 Connection of ADCGND Pin

The ADCGND pin is chip-internal connected to reference ground. In order to provide full offset compensation and achieve full accuracy of ADC1 the ADCGND pin must not be connected to board ground. ADCGND pin should be connected with a capacitor (100 nF) to VAREF only.

4.4 Connection of Exposed Pad

It is recommended to connect the exposed pad to GND.

4.5 Voltage Regulators-Blocking Capacitors

Table 11 External Component Recommendation

| Symbol | Function | Comment |
|--------------|----------------------------------|--|
| C_{VS} | blocking capacitor at VS pin | > 20 μ F Elco + 100 nF Ceramic, ESR < 1 Ω |
| C_{VDDP} | blocking capacitor at VDDP pin | 1 μ F typ. + 100 nF Ceramic, ESR < 1 Ω |
| C_{VDDEXT} | blocking capacitor at VDDEXT pin | 100 nF typ., ESR < 1 Ω |
| C_{VDDC} | blocking capacitor at VDDC pin | > 330 nF + 100 nF Ceramic, ESR < 1 Ω |
| C_{VAREF} | blocking capacitor at VAREF pin | > 100 nF, ESR < 1 Ω |

4.6 Additional External Components

Table 12 External Component Recommendation

| Symbol | Function | Comment |
|--------------|----------------------------------|--------------|
| C_{HSx} | HF blocking capacitor at HSx pin | 6.8 nF |
| R_{MONx} | resistor at MONx pin | 1 k Ω |
| $R_{VBAT_}$ | resistor at VBAT_SENSE pin | 1 k Ω |

4.7 ESD Tests

Note: Test for ESD robustness to IEC61000-4-2 “gun test” (150pF, 330Ω) will be performed. The result and test condition can be provided in a test report

Table 13 ESD “Gun Test”

| Performed Test | Result | Unit | Remarks |
|----------------------------|--------|------|------------------------------|
| ESD at pin LIN, versus GND | > 6 | kV | ¹⁾ positive pulse |
| ESD at pin LIN, versus GND | < -6 | kV | ¹⁾ negative pulse |

1) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3 (IEC 61000-4-2). Tested by external test house (IBEE Zwickau).

5 Electrical Characteristics

This chapter includes all relevant Electrical Characteristics of the product TLE9832-2.

5.1 General Characteristics

5.1.1 Absolute Maximum Ratings

Table 14 Absolute Maximum Ratings ¹⁾

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|-----------------------------------|-----------------------|--------|------|-----------------|------------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Voltages Supply Pins | | | | | | | |
| Supply voltage VS | V_S | -0.3 | – | 40 | V | – | P_5.1.1 |
| Voltage VDDP | V_{DDP} | -0.3 | – | 5.5 | V | – | P_5.1.2 |
| Voltage VDDP | V_{DDP} | -0.3 | – | 6.0 | V | $t < 100\text{ms}$, in Stop Mode only | P_5.1.50 |
| Output voltage VDDEXT | V_{DDEXT} | -0.3 | – | 5.5 | V | – | P_5.1.3 |
| Voltage VDDC | V_{DDC} | -0.3 | – | 1.6 | V | – | P_5.1.4 |
| Voltages High Voltage Pins | | | | | | | |
| Battery Voltage VBAT_SENSE | V_{BAT_SENSE} | -27 | – | 40 | V | – | P_5.1.5 |
| Output voltage HS | V_{HS} | -0.3 | – | 40 | V | – | P_5.1.6 |
| Input voltage at LIN | V_{LIN} | -27 | – | 40 | V | – | P_5.1.7 |
| Input voltage MON_x | $V_{MON_X_maxrate}$ | -40 | – | 40 | V | – | P_5.1.8 |
| Input voltage LS | V_{LS} | -0.3 | – | 40 | V | – | P_5.1.9 |
| Voltages GPIOs | | | | | | | |
| Voltage on any port pin | V_{in} | -0.3 | – | $V_{DDP} + 0.3$ | V | $V_{IN} < 5.4\text{V}$ | P_5.1.10 |
| Voltages Others | | | | | | | |
| Input voltage VAREF | V_{AREF} | -0.3 | – | 5.3 | V | – | P_5.1.11 |
| Temperatures | | | | | | | |
| Junction Temperature | T_j | -40 | – | 150 | $^\circ\text{C}$ | – | P_5.1.12 |
| Storage Temperature | T_{stg} | -55 | – | 150 | $^\circ\text{C}$ | – | P_5.1.13 |
| ESD Resistivity | | | | | | | |
| ESD Resistivity HBM all pins | V_{ESD1} | -2 | – | 2 | kV | EIA/JESD 22-A114B (1.5k Ω , 100pF) | P_5.1.14 |

Table 14 Absolute Maximum Ratings ¹⁾

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|-------------------|--------|------|------|------|--|----------|
| | | Min. | Typ. | Max. | | | |
| ESD Resistivity HBM pins HS, MON1, MON2, MON3, MON4, MON5, VS, VBATSENSE vs.GND | V_{ESD2} | -4 | – | 4 | kV | EIA/JESD 22-A114B (1.5k Ω , 100pF) | P_5.1.15 |
| ESD Resistivity HBM pins LIN vs. LINGND | V_{ESD2} | -6 | – | 6 | kV | EIA/JESD 22-A114B (1.5k Ω , 100pF) | P_5.1.16 |

1) Not subject to production test, specified by design.

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

5.1.2 Functional Range

Table 15 Functional Range

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|--------------------------------|--------|------|------|------------------|-----------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Supply voltage in Active Mode | $V_{\text{S_AM}}$ | 5.5 | – | 27 | V | – | P_5.1.17 |
| Min. Supply voltage in Active Mode with reduced functionality (Microcontroller / Flash with full operation) | $V_{\text{S_AMmin}}$ | 3.0 | – | 5.5 | V | ¹⁾ | P_5.1.18 |
| Supply voltage in | $V_{\text{S_PD}}$ | 3.0 | – | 27 | V | – | P_5.1.19 |
| Supply voltage in Sleep Mode | $V_{\text{S_Sleep}}$ | 3.0 | – | 27 | V | – | P_5.1.20 |
| Supply Voltage transients slew rate | dV_{S}/dt | -1 | – | 1 | V/ μs | ²⁾ | P_5.1.21 |
| Output sum current for all GPIO pins | $I_{\text{GPIO,sum}}$ | – | – | 60 | mA | – | P_5.1.22 |
| Operating frequency | f_{sys} ³⁾ | 5 | – | 40 | MHz | – | P_5.1.23 |
| Junction Temperature | T_j | -40 | – | 150 | $^\circ\text{C}$ | – | P_5.1.24 |

1) Reduced functionality (e.g. cranking pulse) - not part of production test

2) Not subject to production test, specified by design

3) Specified function not guaranteed when limits are exceeded

5.1.3 Current Consumption

Table 16 Electrical Characteristics ¹⁾

$V_s = 5.5V$ to $18V$, $T_J = -40^\circ C$ to $85^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|------------------|--------|------|------|---------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Current Consumption @VS pin | | | | | | | |
| Current Consumption in Active Mode | I_{Active} | – | 30 | 40 | mA | $f_{sys} = 40$ MHz no loads on pins, LIN in recessive state, LS1, LS2, HS1 and HS2 off | P_5.1.25 |
| Current consumption in Stop Mode | $I_{Powerdown}$ | – | 85 | 95 | μA | microcontroller in Stop Mode, LIN recessive state, MON1-5 disabled, GPIOs open (no loads) | P_5.1.26 |
| Current consumption in Stop Mode with cyclic sense enabled | $I_{Powerdown2}$ | – | – | 110 | μA | microcontroller in Stop Mode, LIN recessive state, GPIOs open (no loads) | P_5.1.27 |
| Current consumption in Sleep Mode | I_{Sleep} | – | – | 25 | μA | system in Sleep Mode, microcontroller not powered, LIN recessive state, MON1-5 disabled and GPIOs open (no loads) | P_5.1.28 |

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.1.4 Thermal Resistance

Table 17 Thermal Resistance

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---------------------|------------|--------|------|------|------|-----------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Junction to Ambient | R_{thJA} | – | 23.9 | – | K/W | ¹⁾ | P_5.1.29 |

1) EIA/JESD 52_2, FR4, 76.2 x 114.3 x 1.5 mm; 35 μ Cu, 5 μ Sn; 300 mm²

5.1.5 Timing Characteristics

The transition times between the system modes are specified here. Generally the timings are defined from the time when the corresponding Bits in register PMCON0 are set until the sequence is terminated.

Table 18 System Timing¹⁾

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|----------------------|----------------------------|--------|------|------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Wake-up over battery | t_{start} | – | – | 1 | ms | Battery ramp-up till MCU reset is released; $V_S > 3\text{V}$ and RESET = '1' | P_5.1.30 |
| Sleep Mode Exit | $t_{\text{sleep - exit}}$ | – | – | 1 | ms | rising/falling edge of any wake-up signal (LIN, MONs) till MCU reset is released; | P_5.1.31 |
| Sleep Mode Entry | $t_{\text{sleep - entry}}$ | – | – | 330 | μs | – | P_5.1.32 |
| Stop Mode Exit | $t_{\text{stop - exit}}$ | – | – | 300 | μs | rising/falling edge of any wake-up signal (LIN, MONs, GPIOs) | P_5.1.33 |
| Stop Mode Entry | $t_{\text{stop - entry}}$ | – | – | 300 | μs | – | P_5.1.34 |

1) Not subject to production test, specified by design.

5.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

5.2.1 PMU I/O Supply Parameters VDDP

Table 19 Electrical Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|------------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | I_{VDDP} | 0 | – | 60 | mA | ¹⁾ | P_5.2.1 |
| Required Output Capacitance | C_{VDDP} | 0.1 | – | 10 | μF | ¹⁾ ESR < 1 Ω | P_5.2.2 |
| Output Voltage including line regulation | V_{DDPOUT} | 4.9 | 5.0 | 5.1 | V | $I_{load} < 90\text{mA}; V_S > 5.5\text{V}$ | P_5.2.3 |
| Output Drop | $V_{S\ VDDPout}$ | – | – | +400 | mV | $I_{load} < 70\text{mA}; 3\text{V} < V_S < 5.5\text{V}$ | P_5.2.4 |
| Dynamic Load Regulation | $V_{VDDPLOR}$ | -50 | – | 50 | mV | ¹⁾ 2 ... 70mA; C=470nF; dI/dt=100mA/ μs | P_5.2.5 |
| Dynamic Line Regulation | $V_{VDDPLIR}$ | -25 | – | 25 | mV | ¹⁾ $V_S = 5.5 \dots 20\text{V}$; dV/dt=5V/ μs | P_5.2.6 |
| Power Supply Ripple Rejection | $P_{SSRVDDP}$ | 50 | – | – | dB | ¹⁾ $V_S = 13.5\text{V}$; f=0 ... 1KHz; Vr=2Vpp | P_5.2.7 |
| Over Voltage Detection | V_{DDPOV} | 5.05 | – | 5.4 | V | $V_S > 5.5\text{V}$; Overvoltage leads to SUPPLY_NMI | P_5.2.8 |
| Under Voltage Reset | V_{DDPUV} | 2.4 | – | 2.7 | V | $V_S > 5.5\text{V}$ | P_5.2.9 |
| Over Current Shutdown | I_{VDDPOC} | 90 | – | 180 | mA | – | P_5.2.10 |

¹⁾ Not subject to production test, specified by design

5.2.2 PMU Core Supply Parameters VDDC

Table 20 Electrical Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|--------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Specified Output Current | I_{VDDC} | 0 | – | 30 | mA | ¹⁾ only used as internal core supply | P_5.2.11 |
| Required Output Capacitance | C_{VDDC} | 0.1 | – | 10 | μF | ²⁾ ESR < 1 Ω | P_5.2.12 |
| Output Voltage including line regulation @ Active Mode | V_{DDCOUT} | 1.44 | 1.5 | 1.56 | V | $I_{load} < 40\text{mA}$ | P_5.2.13 |
| Output Voltage including line regulation @ Stop Mode | V_{DDCOUT} | 0.89 | 0.95 | 1.15 | V | $I_{load} < 200\mu\text{A}$ | P_5.2.14 |
| Dynamic Load Regulation | V_{DDCLOR} | -50 | – | 50 | mV | ²⁾ 2 ... 30mA; C=330nF; dI/dt=100mA/ μs | P_5.2.15 |
| Dynamic Line Regulation | V_{DDCLIR} | -25 | – | 25 | mV | ²⁾ $V_{DDP} = 2.5 \dots 5.5\text{V}$; dV/dt=5V/ μs | P_5.2.16 |
| Over Voltage Detection | V_{DDCOV} | 1.61 | – | 1.68 | V | Overvoltage leads to SUPPLY_NMI | P_5.2.17 |
| Under Voltage Reset | V_{DDVUV} | 1.10 | – | 1.19 | V | – | P_5.2.18 |
| Over Current Shutdown | I_{VDDCOC} | 35 | – | 80 | mA | – | P_5.2.19 |

1) VDDC is not intended to be used as external voltage regulator

2) Not subject to production test, specified by design

5.2.3 VDDEXT Voltage Regulator 5.0V

Table 21 Electrical Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|-------------------|--------|------|------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Output Current | I_{VDDEXT} | 0 | – | 20 | mA | ¹⁾ | P_5.2.20 |
| Output Capacitance | C_{VDDEXT} | 10 | – | 1000 | nF | ¹⁾ ESR < 1 Ω | P_5.2.21 |
| Output Voltage including line regulation | V_{DDEXT} | 4.9 | 5.0 | 5.1 | V | $I_{load} < 20\text{mA}; V_S > 5.5\text{V}$ | P_5.2.22 |
| Output Drop | $V_S - V_{DDEXT}$ | | – | +400 | mV | ¹⁾ $I_{load} < 20\text{mA}; 3\text{V} < V_S < 5.5\text{V}$ | P_5.2.23 |
| Dynamic Load Regulation | $V_{DDEXTLOR}$ | -50 | – | 50 | mV | ¹⁾ 2 ... 20mA; C=10nF; dl/dt=10mA/ μ s | P_5.2.24 |
| Dynamic Line Regulation | $V_{VDDEXTLIR}$ | -25 | – | 25 | mV | $V_S = 5.5 \dots 20\text{V}; dV/dt=5\text{V}/\mu\text{s}$ | P_5.2.25 |
| Power Supply Ripple Rejection ¹⁾ | $P_{SSRVDDEXT}$ | 50 | – | – | dB | $V_S = 13.5\text{V}; f=0 \dots 1\text{KHz}; V_r=2\text{Vpp}$ | P_5.2.26 |
| Over Voltage Detection | $V_{VDDEXTOV}$ | 5.05 | – | 5.4 | V | $V_S > 5.5\text{V}$ | P_5.2.27 |
| Under Voltage Detection | $V_{VDDEXTUV}$ | 2.6 | – | 2.9 | V | ²⁾ $V_S > 3.0\text{V}$ | P_5.2.28 |
| Over Current Diagnostic | $I_{VDDEXTOC}$ | 25 | – | 70 | mA | – | P_5.2.29 |

1) Not subject to production test, specified by design

2) When the condition is met, the Bit VDDEXT_CTRL.VDDEXT_SHORT will be set

5.3 System Clocks

5.3.1 Oscillators and PLL

Table 22 Electrical Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|-----------------|---------|------|-------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| PMU Oscillators (Power Management Unit) | | | | | | | |
| Frequency of LP_CLK | f_{LP_CLK1} | 14 | 18 | 22 | MHz | this clock is used at startup and can be used in case the PLL fails | P_5.3.1 |
| Frequency of LP_CLK2 | f_{LP_CLK2} | 70 | 100 | 130 | kHz | this clock is used for cyclic wake and cyclic sense | P_5.3.2 |
| CGU Oscillator (Clock Generation Unit Microcontroller) | | | | | | | |
| Short term frequency deviation | f_{TRIMST} | -1.5% | 5 | +1.5% | MHz | ¹⁾ with respect to nominal configured system frequency within one LIN message (< 10ms ... 100ms) | P_5.3.3 |
| Long term frequency deviation | f_{TRIMLT} | -3.0% | 5 | +3.0% | MHz | with respect to nominal configured system frequency over lifetime and temperature | P_5.3.4 |
| CGU-OSC Start-up time | T_{OSC} | – | – | 10 | μs | startup time OSC from Sleep Mode and Stop Mode, power supply stable | P_5.3.5 |
| PLL (Clock Generation Unit Microcontroller) | | | | | | | |
| VCO frequency range Mode 0 | f_{VCO-0} | 48 | – | 112 | MHz | VCOSEL = "0" | P_5.3.6 |
| VCO frequency range Mode 1 | f_{VCO-1} | 96 | – | 160 | MHz | VCOSEL = "1" | P_5.3.7 |
| Input frequency range | f_{OSC} | 4 | – | 16 | MHz | – | P_5.3.8 |
| XTAL1 input freq. range | f_{OSC} | 4 | – | 16 | MHz | – | P_5.3.9 |
| Output freq. range | f_{PLL} | 0.04687 | – | 80 | MHz | – | P_5.3.10 |
| Free-running frequency Mode 0 | $f_{VCOfree_0}$ | – | – | 38 | MHz | VCOSEL = "0" | P_5.3.11 |
| Free-running frequency Mode 1 | $f_{VCOfree_1}$ | – | – | 76 | MHz | VCOSEL = "1" | P_5.3.12 |
| Input clock high/low time | $t_{high/low}$ | 10 | – | – | ns | – | P_5.3.13 |
| Peak period jitter | t_{jp} | -500 | – | 500 | ps | for K=1 | P_5.3.14 |

Table 22 Electrical Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--------------------|--------|--------|------|------|---------------|-----------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Accumulated jitter | jacc | – | – | 5 | ns | for K=1 | P_5.3.15 |
| lock-in time | T_L | – | – | 200 | μs | – | P_5.3.16 |

1) $V_{DDC} = 1.5\text{ V}$, $T_j = 25^\circ\text{C}$

5.3.2 External Clock Parameters XTAL1, XTAL2

Table 23 Functional Range

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|---------------|----------------------|------|----------|---------------|---------------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Input voltage range limits for signal on XTAL1 | V_{IX1_SR} | $-1.7 + V_{DDC}$ | – | 1.7 | V | 1) | P_5.3.17 |
| Input voltage (amplitude) on XTAL1 | V_{AX1_SR} | $0.3 \times V_{DDP}$ | – | – | V | 2) Peak-to-peak voltage | P_5.3.18 |
| XTAL1 input current | I_{IL} | – | – | ± 20 | μA | $0\text{ V} < V_{IN} < V_{DDC}$ | P_5.3.19 |
| Oscillator frequency | f_{OSC} | 4 | – | 24 | MHz | Clock signal | P_5.3.20 |
| Oscillator frequency | f_{OSC} | 4 | – | 16 | MHz | Crystal or Resonator | P_5.3.21 |
| High time | t_1 | 6 | – | – | ns | – | P_5.3.22 |
| Low time | t_2 | 6 | – | – | ns | – | P_5.3.23 |
| Rise time | t_3 | – | 8 | 8 | ns | – | P_5.3.24 |
| Fall time | t_4 | – | 8 | 8 | ns | – | P_5.3.25 |

1) Overload conditions must not occur on pin XTAL1.

2) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .

5.4 Flash Parameters

This chapter includes the parameters for the 36 kByte embedded flash module.

Table 24 Flash Characteristics ¹⁾

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|-----------|--------|-----------------|------|---------|------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Programming time per 128 Byte page | t_{PR} | – | ²⁾ 3 | 3.5 | ms | – | P_5.4.1 |
| Erase time per sector/page | t_{ER} | – | ²⁾ 4 | 4.5 | ms | – | P_5.4.2 |
| Data retention time | t_{RET} | 20 | – | – | years | 1,000 erase / program cycles | P_5.4.3 |
| Flash erase endurance for user sectors | N_{ER} | 30 | – | – | kcycles | Data retention time 5 years | P_5.4.4 |

1) Not subject for production test, specified by design

2) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.

5.5 Parallel Ports (GPIO)

5.5.1 Functional Range

Table 25 Functional Range

$V_S = 5.5\text{ V to }27\text{ V}$, $T_J = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|----------------------------------|------------------|--------|------|------|------|-----------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Output current on any pin | I_{OH}, I_{OL} | – | – | 20 | mA | 1) 2) | P_5.5.1 |
| Max output current for all GPIOs | I_{max} | – | – | 60 | mA | 1) 2) | P_5.5.2 |

1) One of these limits must be kept.

2) Not subject to production test, specified by design

5.5.2 DC Parameters

These parameters apply to the IO voltage range, $4.5\text{ V} \leq V_{DDP} \leq 5.5\text{ V}$.

Note: Operating Conditions apply.

Keeping signal levels within the limits specified in this table ensures operation without overload conditions.

For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Table 26 DC Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_J = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|-----------|-----------------------|------|----------------------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Input low voltage (all except XTAL1) | V_{IL} | -0.3 | – | $0.3 \times V_{DDP}$ | V | – | P_5.5.3 |
| Input high voltage (all except XTAL1) | V_{IH} | $0.7 \times V_{DDP}$ | – | $V_{DDP} + 0.3$ | V | – | P_5.5.4 |
| Input Hysteresis ¹⁾ | HYS | $0.11 \times V_{DDP}$ | – | – | V | Series resistance = $0\ \Omega$ | P_5.5.5 |
| Output low voltage | V_{OL} | – | – | 1.0 | V | ²⁾ $I_{OL} \leq I_{OLmax}$ | P_5.5.6 |
| Output low voltage | V_{OL} | – | – | 0.4 | V | ²⁾ $I_{OL} \leq$ ³⁾ I_{OLnom} | P_5.5.7 |
| Output high voltage ⁴⁾ | V_{OH} | $V_{DDP} - 1.0$ | – | – | V | ²⁾ $I_{OH} \geq I_{OHmax}$ | P_5.5.8 |
| Output high voltage | V_{OH} | $V_{DDP} - 0.4$ | – | – | V | ²⁾³⁾ $I_{OH} \geq I_{OHnom}$ | P_5.5.9 |
| Input leakage current (Port 2) | I_{OZ1} | -400 | – | +400 | nA | $T_J \leq 85^\circ\text{C}$, $0\text{ V} < V_{IN} < V_{DDP}$ | P_5.5.10 |
| Input leakage current (all other) ⁵⁾ | I_{OZ2} | -5 | – | +5 | μA | $T_J \leq 85^\circ\text{C}$, $0.45\text{ V} < V_{IN} < V_{DDP}$ | P_5.5.11 |

Table 26 DC Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|-----------|--------|------|------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Input leakage current (all other) | I_{OZ2} | -15 | – | +15 | μA | $T_j \leq 150^\circ\text{C}$, $0.45\text{ V} < V_{IN}$ < V_{DDP} | P_5.5.12 |
| Pull level keep current | I_{PLK} | -240 | – | +240 | μA | ⁶⁾ $V_{PIN} \geq V_{IH}$ (up) $V_{PIN} \leq V_{IL}$ (dn) | P_5.5.13 |
| Pull level force current | I_{PLF} | -1.5 | – | +1.5 | mA | ⁶⁾ $V_{PIN} \leq V_{IL}$ (up) $V_{PIN} \geq V_{IH}$ (dn) | P_5.5.14 |
| Pin capacitance (digital inputs/outputs) | C_{IO} | – | – | 10 | pF | – | P_5.5.15 |

- 1) Not subject to production test, specified by design.
- 2) The maximum deliverable output current of a port driver depends on the selected output driver mode. The limit for pin groups must be respected.
- 3) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow GND$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
- 4) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 5) The given values are worst-case values. In production test, this leakage current is only tested at 125°C ; other values are ensured by correlation. For derating, please refer to the following descriptions:
 Leakage derating depending on temperature ($T_j =$ junction temperature [$^\circ\text{C}$]):
 $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times T_j)}$ [μA]. For example, at a temperature of 95°C the resulting leakage current is $3.2\ \mu\text{A}$.
 Leakage derating depending on voltage level ($\Delta V = V_{DDP} - V_{PIN}$ [V]):
 $I_{OZ} = I_{OZtempmax} - (1.6 \times \Delta V)$ [μA]
 This voltage derating formula is an approximation which applies for maximum temperature.
- 6) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
 Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.
 These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

Table 27 Current Limits for Port Output Drivers¹⁾

| Port Output Driver Mode | Maximum Output Current (I_{OLmax} , - I_{OHmax}) | | Nominal Output Current (I_{OLnom} , - I_{OHnom}) | | Number |
|-------------------------|---|-------------|---|-------------|----------|
| | VDDP \geq 4.5V | VDDP < 4.5V | VDDP \geq 4.5V | VDDP < 4.5V | |
| Strong Driver | 7.5 mA | 7.5 mA | 2.5 mA | 2.5 mA | P_5.5.16 |
| Medium Driver | 4 mA | 2.5 mA | 1.0 mA | 1.0 mA | P_5.5.17 |
| Weak Driver | 0.5 mA | 0.5 mA | 0.1 mA | 0.1 mA | P_5.5.18 |

1) Not subject to production test, specified by design.

Note: Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.

During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < GND$) the voltage on V_{DDP} pins with respect to ground (GND) must not exceed the values defined by the absolute maximum ratings.

5.6 LIN Transceiver

5.6.1 Electrical Characteristics

Table 28 Electrical Characteristics LIN Transceiver

$V_S = 5.5V - 18V$, $T_j = -40^\circ C$ to $+150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|----------------------|--------------------|-------------------|--------------------|------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Bus Receiver Interface | | | | | | | |
| Receiver threshold voltage, recessive to dominant edge | V_{th_dom} | $0.4 \times V_S$ | $0.45 \times V_S$ | $0.53 \times V_S$ | V | SAE J2602 | P_5.6.1 |
| Receiver dominant state | V_{BUSdom} | -27 | – | $0.4 \times V_S$ | V | LIN Spec 2.1 (Par. 17) | P_5.6.2 |
| Receiver threshold voltage, dominant to recessive edge | V_{th_rec} | $0.47 \times V_S$ | $0.55 \times V_S$ | $0.6 \times V_S$ | V | SAE J2602 | P_5.6.3 |
| Receiver recessive state | V_{BUSrec} | $0.6 \times V_S$ | – | $1.15 \times V_S$ | V | ¹⁾ LIN Spec 2.1 (Par. 18) | P_5.6.4 |
| Receiver center voltage | V_{BUS_CN} T | $0.475 \times V_S$ | $0.5 \times V_S$ | $0.525 \times V_S$ | V | ²⁾ LIN Spec 2.1 (Par. 19) | P_5.6.5 |
| Receiver hysteresis | V_{HYS} | $0.07 V_S$ | $0.12 \times V_S$ | $0.175 \times V_S$ | V | ³⁾ LIN Spec 2.1 (Par. 20) | P_5.6.6 |
| Wake-up threshold voltage | $V_{BUS,wk}$ | $0.4 \times V_S$ | $0.5 \times V_S$ | $0.6 \times V_S$ | V | – | P_5.6.7 |
| Dominant time for bus wake-up | $t_{WK,bus}$ | 3 | – | 15 | μs | To achieve the required wake-up time from 30 μs to 150 μs according to LIN spec., an additional digital filter is added (see PMU chapter) | P_5.6.8 |
| Bus Transmitter Interface | | | | | | | |
| Bus recessive output voltage | $V_{BUS,ro}$ | $0.8 \times V_S$ | – | V_S | V | $V_{TxD} = \text{high Level}$ | P_5.6.9 |
| Bus short circuit current | $I_{BUS,sc}$ | 40 | 100 | 150 | mA | $V_{BUS} = 13.5 V$ | P_5.6.10 |
| Leakage current | $I_{BUS_NO_GND}$ | -1000 | -70 | – | μA | $V_S = 0 V$; $V_{BUS} = -12 V$; LIN Spec 2.1 (Par. 15) | P_5.6.11 |
| Leakage current | $I_{BUS_NO_BAT}$ | – | 10 | 20 | μA | $V_S = 0 V$; $V_{BUS} = 18 V$; LIN Spec 2.1 (Par. 16) | P_5.6.12 |
| Leakage current | $I_{BUS_PAS_dom}$ | -1 | – | – | mA | $V_S = 18 V$; $V_{BUS} = 0 V$; LIN Spec 2.1 (Par. 13) | P_5.6.13 |
| Leakage current | $I_{BUS_PAS_rec}$ | – | – | 20 | μA | $V_S = 8 V$; $V_{BUS} = 18 V$; LIN Spec 2.1 (Par. 14) | P_5.6.14 |
| Bus pull-up resistance | R_{BUS} | 20 | 30 | 47 | k Ω | Normal mode LIN Spec 2.1 (Param. 26) | P_5.6.15 |
| LIN input capacity | C_{LIN_IN} | – | 15 | 30 | pF | ⁴⁾ | P_5.6.80 |

Table 28 Electrical Characteristics (cont'd) LIN Transceiver
 $V_S = 5.5V - 18V$, $T_j = -40^\circ C$ to $+150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|--------------|--------|------|-------|---------|--|----------|
| | | Min. | Typ. | Max. | | | |
| AC Characteristics - Transceiver Normal Slope Mode | | | | | | | |
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R}$ | 0.1 | 1 | 6 | μs | (LIN Spec 2.1; Param. 31) | P_5.6.16 |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R}$ | 0.1 | 1 | 6 | μs | (LIN Spec 2.1; Param. 31) | P_5.6.17 |
| Receiver delay symmetry | $t_{sym,R}$ | -2 | - | 2 | μs | $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; (LIN Spec 2.1; Param. 31) | P_5.6.18 |
| Duty cycle D1 Normal Slope Mode (for worst case at 20 kBit/s) | t_{duty1} | 0.396 | - | - | | ⁵⁾ duty cycle 1 $TH_{Rec(max)} = 0.744 \times V_S$; $TH_{Dom(max)} = 0.581 \times V_S$; $V_S = 5.5 \dots 18 V$; $t_{bit} = 50 \mu s$; $D1 = t_{bus_rec(min)}/2 t_{bit}$; LIN Spec 2.1 (Par. 27) | P_5.6.19 |
| Duty cycle D2 Normal Slope Mode (for worst case at 20 kBit/s) | t_{duty2} | - | - | 0.581 | | ⁶⁾ duty cycle 2 $TH_{Rec(max)} = 0.422 \times V_S$; $TH_{Dom(max)} = 0.284 \times V_S$; $V_S = 5.5 \dots 18 V$; $t_{bit} = 50 \mu s$; $D2 = t_{bus_rec(max)}/2 t_{bit}$; LIN Spec 2.1 (Par. 28) | P_5.6.20 |
| AC Characteristics - Transceiver Low Slope Mode | | | | | | | |
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R}$ | 0.1 | 1 | 6 | μs | (LIN Spec 2.1; Param. 31) | P_5.6.21 |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R}$ | 0.1 | 1 | 6 | μs | (LIN Spec 2.1; Param. 31) | P_5.6.22 |
| Receiver delay symmetry | $t_{sym,R}$ | -2 | - | 2 | μs | $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; (LIN Spec 2.1; Param. 32) | P_5.6.23 |

Electrical Characteristics

Table 28 Electrical Characteristics (cont'd) LIN Transceiver
 $V_S = 5.5V - 18V$, $T_j = -40^\circ C$ to $+150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|-------------|--------|------|-------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Duty cycle D3 (for worst case at 10,4 kBit/s) | t_{duty1} | 0.417 | – | – | | ⁷⁾ duty cycle 3 $TH_{Rec}(max) = 0.778 \times V_S$; $TH_{Dom}(max) = 0.616 \times V_S$; $V_S = 5.5 \dots 18 V$; $t_{bit} = 96 \mu s$; $D3 = t_{bus_rec(min)}/2 t_{bit}$; LIN Spec 2.1 (Par. 29) | P_5.6.24 |
| Duty cycle D4 (for worst case at 10,4 kBit/s) | t_{duty2} | – | – | 0.590 | | duty cycle 4 $TH_{Rec}(max) = 0.389 \times V_S$; $TH_{Dom}(max) = 0.251 \times V_S$; $V_S = 5.5 \dots 18 V$; $t_{bit} = 96 \mu s$; $D4 = t_{bus_rec(max)}/2 t_{bit}$; LIN Spec 2.1 (Par. 30) | P_5.6.25 |

AC Characteristics - Transceiver Fast Slope Mode

| | | | | | | | |
|--|--------------|-------|---|-------|---------|--|----------|
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R}$ | 0.1 | 1 | 6 | μs | – | P_5.6.26 |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R}$ | 0.1 | 1 | 6 | μs | – | P_5.6.27 |
| Receiver delay symmetry | $t_{sym,R}$ | -1 | – | 1 | μs | $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; | P_5.6.28 |
| Duty cycle D5 (for worst case at 40 kBit/s) | t_{duty1} | 0.395 | – | – | | ⁶⁾ duty cycle 5 $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; $V_S = 5.5 \dots 18 V$; $t_{bit} = 25 \mu s$; $D1 = t_{bus_rec(min)}/2 t_{bit}$; | P_5.6.29 |
| Duty cycle D6 (for worst case at 40 kBit/s) | t_{duty2} | – | – | 0.581 | | ⁶⁾ duty cycle 6 $TH_{Rec}(max) = 0.422 \times V_S$; $TH_{Dom}(max) = 0.284 \times V_S$; $V_S = 5.5 \dots 18 V$; $t_{bit} = 25 \mu s$; $D2 = t_{bus_rec(max)}/2 t_{bit}$; LIN Spec 2.1 (Par. 28) | P_5.6.30 |

AC Characteristics - Flash Mode

| | | | | | | | |
|--|--------------|-----|-----|---|---------|---|----------|
| Propagation delay bus dominant to RxD LOW | $t_{d(L),R}$ | 0.1 | 0.5 | 6 | μs | – | P_5.6.31 |
|--|--------------|-----|-----|---|---------|---|----------|

Electrical Characteristics

Table 28 Electrical Characteristics (cont'd) LIN Transceiver

$V_s = 5.5V - 18V$, $T_j = -40^\circ C$ to $+150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---------------|--------|------|-------|---------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Propagation delay bus recessive to RxD HIGH | $t_{d(H),R}$ | 0.1 | 0.5 | 6 | μs | – | P_5.6.32 |
| Receiver delay symmetry | $t_{sym,R}$ | -1.0 | – | 1.0 | μs | $t_{sym,R} = t_{d(L),R} - t_{d(H),R}$; | P_5.6.33 |
| Duty cycle D7 (for worst case at 115 kBit/s) for +1 μs Receiver delay symmetry | t_{duty1} | 0.399 | – | – | | ⁸⁾ duty cycle D7 $TH_{Rec}(max) = 0.744 \times V_s$; $TH_{Dom}(max) = 0.581 \times V_s$; $V_s = 13.5 V$; $t_{bit} = 8.7 \mu s$; $D7 = t_{bus_rec(min)}/2 t_{bit}$; | P_5.6.34 |
| Duty cycle D8 (for worst case at 115 kBit/s) for +1 μs Receiver delay symmetry | t_{duty2} | – | – | 0.578 | | ⁶⁾ duty cycle 8 $TH_{Rec}(max) = 0.422 \times V_s$; $TH_{Dom}(max) = 0.284 \times V_s$; $V_s = 13.5 V$; $t_{bit} = 8.7 \mu s$; $D8 = t_{bus_rec(max)}/2 t_{bit}$; | P_5.6.35 |
| TxD dominant time out | $t_{timeout}$ | 6 | 12 | 20 | ms | ⁸⁾ $V_{TxD} = 0 V$ | P_5.6.36 |

- 1) Maximum limit specified by design.
- 2) $V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$
- 3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
- 4) This parameter is not subject to production test
- 5) Bus load concerning LIN Spec 2.1:
 Load 1 = 1 nF / 1 k Ω = C_{BUS} / R_{BUS}
 Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
 Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
- 6) Bus loads:
 Load 1 = 1 nF / 1 k Ω = C_{BUS} / R_{BUS}
- 7) Bus load concerning LIN Spec 2.1:
 Load 1 = 1 nF / 1 k Ω = C_{BUS} / R_{BUS}
 Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
 Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
- 8) Timeout can be disabled optional

5.7 High-Speed Synchronous Serial Interface

The table below provides the SSC timing in the TLE9832-2.

Table 29 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|----------------------|--------|-----------------------------|------|------|------|-----------------------|---------|
| | | Min. | Typ. | Max. | | | |
| SCLK clock period | t_0 | ¹⁾ $2 * T_{SSC}$ | – | – | | – | P_5.7.1 |
| MTSR delay from SCLK | t_1 | 10 | – | – | ns | – | P_5.7.2 |
| MRST setup to SCLK | t_2 | 10 | – | – | ns | – | P_5.7.3 |
| MRST hold from SCLK | t_3 | 15 | – | – | ns | – | P_5.7.4 |

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24\text{ MHz}$, $t_0 = 83.3\text{ ns}$. T_{CPU} is the CPU clock period.

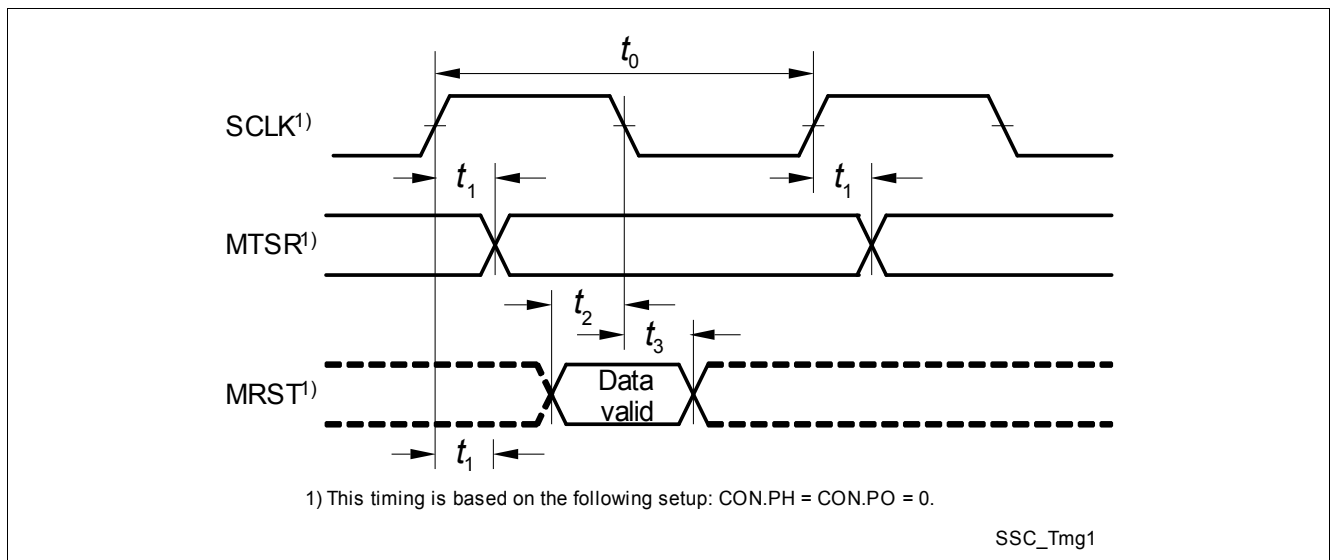


Figure 32 SSC Master Mode Timing

5.8 Measurement Unit

5.8.1 Analog Digital Converter 8-Bit

Table 30 DC Specifications ADC 8 Bit

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|----------------------|--------|-----------|-------------------|------|-------------------------------------|---------|
| | | Min. | Typ. | Max. | | | |
| Resolution | – | – | 8 | – | Bit | – | P_5.8.1 |
| Offset error | – | -10 | 4 | +10 | mV | – | P_5.8.2 |
| Gain single-ended input mode | GSE | – | 1 | – | | – | P_5.8.3 |
| Input voltage single-ended mode | V_{ainp}, V_{ainn} | 0 | – | V_{DD1V5_A} | V | – | P_5.8.4 |
| Gain differential input mode | GDF | | 1.24 | – | – | – | P_5.8.5 |
| Common input voltage in differential mode | V_{icm} | 0.5 | 0.6 | $V_{DDP}/2 + 0.1$ | – | $V_{icm} = (V_{ainp} + V_{ainn})/2$ | P_5.8.6 |
| Gain error | – | -5 | 1.5 | +5 | %FSR | – | P_5.8.7 |
| Differential nonlinearity (DNL) | – | -1.5 | 0.5 | +1.5 | LSB | – | P_5.8.8 |
| Integral Nonlinearity (INL) | – | -3 | ± 1.5 | 3 | LSB | – | P_5.8.9 |

5.8.2 Measurement Unit (VBAT_SENSE - Supply Voltage Attenuator)

Table 31 Supply voltage signal conditioning

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|--------------------------|--------|------|------|---------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Battery Voltage Measurement V_{BAT_SENSE} | | | | | | | |
| Nominal operating input voltage range ¹⁾ | V_{S/BAT_SENSE} | 3 | – | 20 | V | Max. value corresponds to typ. ADC full scale input | P_5.8.10 |
| Measurement input resistance | $R_{in,VS/VBAT_SENS E}$ | 200 | 289 | 380 | k Ω | PD_N=1 (on-state) | P_5.8.11 |
| Measurement input leakage current | I_{leak} | 0 | – | 1.0 | μA | PD_N=0 (off-state), $V_{BAT_SENSE}=13.5\text{ V}$ | P_5.8.12 |
| Overall (calibrated) measurement accuracy after A/D-conversion²⁾ | | | | | | | |
| V_{BAT_SENSE} / V_S 8-bit ADC | $\Delta V_{BATADC8B}$ | -250 | – | 250 | mV | $V_S = 5.5\text{ V to }18\text{ V}$, $T_j = 40..85^\circ\text{ C}$ | P_5.8.13 |
| V_{BAT_SENSE} / V_S 10-bit ADC | $\Delta V_{BATADC10B}$ | -200 | – | 200 | mV | $V_S = 5.5\text{ V to }18\text{ V}$, $T_j = 40..85^\circ\text{ C}$ | P_5.8.14 |

Table 31 Supply voltage signal conditioning
 $V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--------------------|-------------------------|--------|------|------|------|-----------------------|----------|
| | | Min. | Typ. | Max. | | | |
| V_{DD5_SENSE} | ΔV_{DDP_SENSE} | -150 | – | 150 | mV | – | P_5.8.15 |
| V_{DD1V5_SENSE} | ΔV_{DDC_SENSE} | -45 | – | 45 | mV | – | P_5.8.16 |

1) This parameter is not subject to production test

2) The device is calibrated based on an external 1k Ω resistor

5.8.3 Measurement Functions Monitoring Input Voltage Attenuator

Table 32 Monitoring input voltage attenuation
 $V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--------------------------------|----------|--------|------|------|------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Power Supply | | | | | | | |
| Input resistance ¹⁾ | R_{IN} | 300 | 400 | 500 | k Ω | PD_N=1 (on-state) $V_{MON_X}=0$ to 18V if VMON_SEN_SEL_INRANGE = 0 | P_5.8.17 |
| Input resistance | R_{IN} | 250 | – | – | k Ω | $V_{MON_X}=0$ to 28V if VMON_SEN_SEL_INRANGE = 1 >200 k Ω under all other conditions | P_5.8.18 |

Timing Characteristics

| | | | | | | | |
|----------------------------------|-----------------|---|---|----|---------------|---|----------|
| Analog Multiplexer Settling Time | $T_{MUXsettle}$ | – | – | 30 | μs | This time frame is valid from writing the corresponding selection register to proper settling of the voltage at channel 7 of the 10-Bit ADC | P_5.8.19 |
|----------------------------------|-----------------|---|---|----|---------------|---|----------|

Overall (calibrated) measurement accuracy after A/D-conversion

| | | | | | | | |
|-----------------------|-----------------------------|------|---|-----|----|--|----------|
| V_{MONx} 10-bit ADC | ΔV_{MONxAD} C10B | -200 | – | 200 | mV | $V_S=5.5\text{ V to }18\text{ V}$, $T_j = 40..85^\circ\text{ C}$ | P_5.8.20 |
|-----------------------|-----------------------------|------|---|-----|----|--|----------|

1) Not subject to production test, specified by design.

5.8.4 Temperature Sensor Module

Table 33 Electrical Characteristics Temperature Sensor Module

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|--------------------|--------|--------|------|------------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Linear temperature range | T_{RANGE} | -40 | | 175 | $^\circ\text{C}$ | – | P_5.8.21 |
| Output voltage V_{TEMP} at $T_0=273\text{ K (}0^\circ\text{C)}$ Mode 1 | a | – | 0.4893 | – | V | ¹⁾ DVBE_MODE=0 $T=273\text{ K (}0^\circ\text{C)}$ | P_5.8.22 |
| Output voltage V_{TEMP} at $T_0=273\text{ K (}0^\circ\text{C)}$ Mode 2 | a | – | 0.5365 | – | V | DVBE_MODE=1 $T_0=273\text{ K (}0^\circ\text{C)}$ | P_5.8.23 |
| Temperature sensitivity b in Mode 1 | b | – | 1.685 | – | mV/K | ¹⁾ DVBE_MODE=0 | P_5.8.24 |
| Temperature sensitivity b Mode 2 | b | – | 1.834 | – | mV/K | DVBE_MODE=1 | P_5.8.25 |
| Accuracy_1 ²⁾ | Acc_1 | -10 | – | 10 | $^\circ\text{C}$ | $-40^\circ\text{C} < T_j < 125^\circ\text{C}$ | P_5.8.26 |
| Accuracy_2 | Acc_2 | -15 | – | 15 | $^\circ\text{C}$ | $125^\circ\text{C} < T_j < 175^\circ\text{C}$ | P_5.8.27 |

1) Not subject to production test, specified by design

2) Accuracy with reference to on-chip temperature calibration measurement

5.9 ADC - 10-Bit

5.9.1 VAREF

5.9.1.1 Functional Range

Table 34 Functional Range

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---------------------|-----------------------|--------|------|----------------------|------|-----------------------|---------|
| | | Min. | Typ. | Max. | | | |
| VAREF input voltage | $V_{\text{AREF_IN}}$ | 0 | – | $V_{\text{DDP}}+0.3$ | V | – | P_5.9.1 |

5.9.1.2 Electrical Characteristics

Table 35 10-Bit ADC - VAREF

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---------------------------------|------------------------|--------|------|------|---------------|--|---------|
| | | Min. | Typ. | Max. | | | |
| Output Capacitance | C_{VAREF} | 0.1 | – | 1 | μF | ESR < 1 Ω | P_5.9.2 |
| Reference output voltage | V_{AREF} | 4.95 | 5 | 5.05 | V | $V_S > 5.5\text{V}$ | P_5.9.3 |
| DC Supply voltage rejection | DC_{PSRVAREF} | 30 | – | – | dB | ¹⁾ | P_5.9.4 |
| Supply voltage ripple rejection | AC_{PSRVAREF} | 26 | – | – | dB | ¹⁾ $V_S = 13.5\text{V}$; $f=0 \dots 1\text{KHz}$; $V_r=2\text{Vpp}$ | P_5.9.5 |
| Turn ON time | t_{so} | – | – | 200 | μs | ¹⁾ $C_{\text{ext}}=100\text{nF}$ PD_N to 99.9% of final value (test setup: measure 1 τ , calculate 5 τ .) | P_5.9.6 |

1) Not subject to production test, specified by design.

5.9.2 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 36 A/D Converter Characteristics

$V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|---------------|---|---|---|---------------|--------------------------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Analog reference supply | V_{AREFSR} | $V_{AGND} + 1.0$ | – | $V_{DDPA} + 0.05$ | V | 1) | P_5.9.7 |
| Analog reference ground | V_{AGNDSR} | $GND - 0.05$ | – | 1.5 | V | 2) | P_5.9.8 |
| Analog input voltage range | V_{AIN} | V_{AGND} | – | V_{AREF} | V | 3) | P_5.9.9 |
| Analog clock frequency | f_{ADCI} | 0.5 | – | 20 | MHz | 4) | P_5.9.10 |
| Conversion time for 10-bit result ⁵⁾ | t_{C10} | (13 + STC) $\times t_{ADCI}$ $+ 2 \times t_{SYS}$ | (13 + STC) $\times t_{ADCI}$ $+ 2 \times t_{SYS}$ | (13 + STC) $\times t_{ADCI}$ $+ 2 \times t_{SYS}$ | – | – | P_5.9.11 |
| Conversion time for 8-bit result | t_{C8} | (11 + STC) $\times t_{ADCI}$ $+ 2 \times t_{SYS}$ | (11 + STC) $\times t_{ADCI}$ $+ 2 \times t_{SYS}$ | (11 + STC) $\times t_{ADCI}$ $+ 2 \times t_{SYS}$ | – | – | P_5.9.12 |
| Wake-up time from analog Stop Mode, fast mode | t_{WAF} | – | – | 4 | μs | 6) | P_5.9.13 |
| Wake-up time from analog Stop Mode, slow mode | t_{WAS} | – | – | 15 | μs | 6) | P_5.9.14 |
| Total unadjusted error ⁷⁾ | TUE | -15 | – | + 15 | LSB | 1) $V_{AREF} = 5.0\text{ V} \pm 1\%$ | P_5.9.15 |
| DNL error | $EA_{DNL}EA$ | -2 | – | + 2 | LSB | – | P_5.9.16 |
| INL error | $EA_{INL}EA$ | -5 | – | + 5 | LSB | – | P_5.9.17 |
| Gain error | $EA_{GAIN}EA$ | -10 | – | + 10 | LSB | – | P_5.9.18 |
| Offset error | $EA_{OFF}EA$ | -2 | – | + 2 | LSB | – | P_5.9.19 |
| Total capacitance of an analog input | C_{AINT} | – | – | 10 | pF | 6)8) | P_5.9.20 |
| Switched capacitance of an analog input | C_{AINS} | – | – | 4 | pF | 6)8) | P_5.9.21 |
| Resistance of the analog input path | R_{AIN} | – | – | 2 | k Ω | 6)8) | P_5.9.22 |
| Total capacitance of the reference input | C_{AREFT} | – | – | 15 | pF | 6)8) | P_5.9.23 |
| Switched capacitance of the reference input | C_{AREFS} | – | – | 7 | pF | 6)8) | P_5.9.24 |
| Resistance of the reference input path | R_{AREF} | – | – | 2 | k Ω | 6)8) | P_5.9.25 |

1) TUE is tested at $V_{AREF} = 5V \pm 1\%$, $V_{AGND} = 0V$. It is verified by design for all other voltages within the defined voltage range.

The specified TUE is valid only if V_{AREF} and V_{AGND} remain stable during the measurement time.

- 2) Only valid in case of external supplied reference voltage.
- 3) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be 000_H or 3FF_H, respectively.
- 4) The limit values for f_{ADCl} must not be exceeded when selecting the peripheral frequency and the prescaler setting.
- 5) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result.
- 6) Not subject to production test, specified by design.
- 7) The total unadjusted error TUE is the maximum deviation from the ideal ADC transfer curve, not the sum of individual errors. All error specifications are based on measurement methods standardized by IEEE 1241.2000.
- 8) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used:

$$C_{AINtyp} = 12 \text{ pF}, C_{AINStyp} = 5 \text{ pF}, R_{AINtyp} = 1.0 \text{ k}\Omega, C_{AREFTtyp} = 15 \text{ pF}, C_{AREFStyp} = 10 \text{ pF}, R_{AREFtyp} = 1.0 \text{ k}\Omega.$$

5.10 High-Voltage Monitor Input

Table 37 Electrical Characteristics

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|------------------------|------------------|------------------|------------------|---------------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Input Pin characteristics | | | | | | | |
| Wake-up/monitoring threshold voltage | V_{MONth} | $0.4 \cdot V_S$ | $0.5 \cdot V_S$ | $0.6 \cdot V_S$ | V | without external serial resistor R_S (with R_S : $\Delta V = I_{\text{PD/PU}} \cdot R_S$); | P_5.10.1 |
| Threshold hysteresis | $V_{\text{MONth,hys}}$ | $0.02 \cdot V_S$ | $0.06 \cdot V_S$ | $0.12 \cdot V_S$ | V | in all modes; without external serial resistor R_S (with R_S : $\Delta V = I_{\text{PD/PU}} \cdot R_S$); | P_5.10.2 |
| Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = low | $I_{\text{PU, MONx}}$ | -20 | -10 | -1 | μA | $0 \text{ V} < V_{\text{MON_IN}} < V_S - 2 \text{ V}$ | P_5.10.3 |
| Pull-up current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high | $I_{\text{PU, MONx}}$ | -20 | -10 | -1 | μA | $0.6 \cdot V_S < V_{\text{MON_IN}} < V_S - 2 \text{ V}$ | P_5.10.4 |
| Pull-down current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = high | $I_{\text{PD, MONx}}$ | 4 | 10 | 18 | μA | $2 \text{ V} < V_{\text{MON_IN}} < V_S$ | P_5.10.5 |
| Pull-down current MONx_CTRL_STS.MONx_PU = high MONx_CTRL_STS.MONx_PD = high | $I_{\text{PD, MONx}}$ | 4 | 10 | 18 | μA | $2 \text{ V} < V_{\text{MON_IN}} < 0.4 \cdot V_S$ | P_5.10.6 |
| Input leakage current MONx_CTRL_STS.MONx_PU = low MONx_CTRL_STS.MONx_PD = low | $I_{\text{LK,I}}$ | -2 | – | 2 | μA | $0 \text{ V} < V_{\text{MON_IN}} < 28 \text{ V}$ | P_5.10.7 |

The Parameters of the analog measurement are listed in the chapter Measurement Interface.

5.11 High Side Switches

5.11.1 Functional Range

Table 38 Functional Range

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---|-------------------------------|--------|------|------------------|------|---|----------|
| | | Min. | Typ. | Max. | | | |
| Nominal Operating Voltage | V_S | 5.5 | – | 27 | V | – | P_5.11.1 |
| Current range for Sleep Mode / Stop Mode | $I_{\text{HS max sleep_pd}}$ | – | – | 40 | mA | Cyclic Sense Mode | P_5.11.2 |
| PWM frequency of HS with Slew Rate Control | $f_{\text{PWM_W_SR}}$ | 0 | – | 10 | kHz | ¹⁾ Frequency must be configured in the PWM Generator | P_5.11.3 |
| PWM frequency of HS without Slew Rate Control | $f_{\text{PWM_W/O_SR}}$ | 0 | – | 25 ²⁾ | kHz | ¹⁾ Frequency must be configured in the PWM Generator | P_5.11.4 |

1) Not subject to production test, specified by design.

2) referring to a 47ohm series resistor to charge an external power mos gate

5.11.2 Electrical Characteristics

Table 39 Electrical Characteristics

$V_S = 5.5\text{V}$ to 27V , $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|----------------------------|--------|------|-------|------------------|--|----------|
| | | Min. | Typ. | Max. | | | |
| Maximum ratings | | | | | | | |
| Output voltage | V_{HSxOUT} | -0.3 | – | V_S | V | min. value referred to GND_A | P_5.11.5 |
| Output HS | | | | | | | |
| ON-State Resistance | R_{ON} | – | – | 20 | Ω | $V_S = 5.5$ to 27V , $I_{\text{ds}} = 100\text{mA}$, higher resistance below $V_S = 5.5\text{V}$ | P_5.11.6 |
| Output leakage Current | I_{leakage} | – | – | 2 | μA | Output OFF $0\text{V} < V_{\text{XLO}} < V_S$; $T_j < 85^\circ\text{C}$ | P_5.11.7 |
| Output Slew Rate (rising) with Slew Rate Control | $SR_{\text{raise_w_SR}}$ | 1 | – | 10 | V/ μs | 10% to 90% of V_S $V_S = 9$ to 18V $R_L = 300\Omega$ ¹⁾ | P_5.11.8 |

Electrical Characteristics
Table 39 Electrical Characteristics (cont'd)
 $V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|------------------------------|--------|------|------|------------------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Output Slew Rate (falling) with Slew Rate Control | $SR_{\text{fall_w_SR}}$ | -10 | – | -1 | V/ μs | 90% to 10% of V_S $V_S = 9\text{ to }18\text{V}$ $R_L = 300\Omega^1$ | P_5.11.9 |
| Output Slew Rate (rising) without Slew Rate Control | $SR_{\text{raise_w/o_SR}}$ | 25 | – | 60 | V/ μs | 10% to 90% of V_S $V_S = 9\text{ to }18\text{V}$ $R_L = 300\Omega^1$ | P_5.11.10 |
| Output Slew Rate (falling) without Slew Rate Control | $SR_{\text{fall_w/o_SR}}$ | -30 | – | -10 | V/ μs | 90% to 10% of V_S $V_S = 9\text{ to }18\text{V}$ $R_L = 300\Omega^1$ | P_5.11.11 |
| Turn ON Delay time | $t_{\text{IN-HS}}$ | – | – | 3 | μs | ON = 1 to 10% of V_S $R_L = 300\Omega$ | P_5.11.12 |
| Turn ON time | t_{ON} | 1 | – | 15 | μs | $V_S = 13.5\text{V}$ HS_ON=1 to 90% of V_S $R_L = 300\Omega$ $T_j = 25^\circ\text{C}$ | P_5.11.13 |
| Turn OFF time | t_{OFF} | 1 | – | 15 | μs | $V_S = 13.5\text{V}$ HS_ON= 0 to 10% of V_S $R_L = 300\Omega$; $T_j = 25^\circ\text{C}$ | P_5.11.14 |
| Load current limitation | I_{short} | -1.2 | – | – | A | ¹⁾ $V_S = 27\text{V}$, $V_{\text{HS}} = 0\text{V}$, max duration 200 μs | P_5.11.15 |

Over-current detection

| | | | | | | | |
|------------------------------------|-------------------------------|-----|---|-----|---------------|--|-----------|
| Overcurrent threshold 0 | $I_{\text{oct}0}$ | 4 | – | 18 | mA | ¹⁾ HSx_OC_SEL =00 | P_5.11.16 |
| Overcurrent threshold 0 hysteresis | $I_{\text{oct}0,\text{hyst}}$ | 2 | – | 5 | mA | ¹⁾ HSx_OC_SEL =00 | P_5.11.17 |
| Overcurrent threshold 1 | $I_{\text{oct}1}$ | 50 | – | 75 | mA | HSx_OC_SEL =01 | P_5.11.18 |
| Overcurrent threshold 1 hysteresis | $I_{\text{oct}1,\text{hyst}}$ | 5 | – | 15 | mA | ¹⁾ HSx_OC_SEL =01 | P_5.11.19 |
| Overcurrent threshold 2 | $I_{\text{oct}2}$ | 100 | – | 150 | mA | HSx_OC_SEL =10 | P_5.11.20 |
| Overcurrent threshold 2 hysteresis | $I_{\text{oct}2,\text{hyst}}$ | 10 | – | 30 | mA | ¹⁾ HSx_OC_SEL =10 | P_5.11.21 |
| Overcurrent threshold 3 | $I_{\text{oct}3}$ | 150 | – | 220 | mA | HSx_OC_SEL =11 | P_5.11.22 |
| Overcurrent threshold 3 hysteresis | $I_{\text{oct}3,\text{hyst}}$ | 20 | – | 50 | mA | ¹⁾ HSx_OC_SEL =11 | P_5.11.23 |
| Overall over-current filter time | t_{octf} | 8 | – | 80 | μs | ¹⁾ $V_S = 13.5\text{V}$, $R_L = 100\Omega$, HS_ON to OC_SD (including switch- on time) | P_5.11.24 |

ON-state open load detection

| | | | | | | | |
|---------------------|---------------------|---|---|----|----|------------------------------------|-----------|
| Open load threshold | I_{OLONth} | 4 | – | 18 | mA | ¹⁾ OL_EN = 1; HS_ON = 1 | P_5.11.25 |
|---------------------|---------------------|---|---|----|----|------------------------------------|-----------|

Table 39 Electrical Characteristics (cont'd)
 $V_S = 5.5\text{ V to }27\text{ V}$, $T_j = -40^\circ\text{ C to }+150^\circ\text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--------------------------------------|------------------|---------------|-----------------|----------------|------------------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Hysteresis | $I_{OLONhys}$ | 1 | – | 4 | mA | ¹⁾ OL_EN = 1; HS_ON = 1 | P_5.11.26 |
| Off-state open load detection | | | | | | | |
| Open load voltage threshold | V_{OLth1} | 0.5* V_S | 0.67 * V_S | 0.85* V_S | V | I_{OL_test} ; open load activated; OLTH_SEL = 1 | P_5.11.27 |
| Hysteresis | V_{OLhys} | 0.1* V_S | – | 0.3* V_S | V | IOL_SEL = 1 | P_5.11.28 |
| Open load output current | I_{OL_test} | -150 | – | -25 | μA | IOL_SEL = 0 | P_5.11.29 |
| Open load output current | I_{OL_test} | -1.5 | – | -0.5 | mA | IOL_SEL = 1 | P_5.11.30 |
| Cyclic sense mode | | | | | | | |
| ON-State Resistance | $R_{ON,static}$ | – | – | 40 | Ω | Definition: differential resistance or resistance at 40 mA | P_5.11.31 |
| Output Slew Rate (rising) | $SR_{rise}^{1)}$ | 1 | – | – | V/ μs | 10% to 90% of V_S $V_S = 9\text{ to }18\text{V}$ $R_L = 300\Omega^{1)}$ | P_5.11.32 |
| Output Slew Rate (falling) | $SR_{fall}^{1)}$ | – | – | -1 | V/ μs | 90% to 10% of V_S $V_S = 9\text{ to }18\text{V}$ $R_L = 300\Omega$ | P_5.11.33 |
| Delay Time CYCLIC_ON-HS | t_{IN-CYC} | – | – | 2 | μs | ON = 1 to 10% of V_S RL=300 Ω | P_5.11.34 |
| Turn-ON time | t_{ON} | – | – | 15 | μs | $V_S = 13.5\text{V}$ ON=1 to 90% $R_L = 300\Omega$ | P_5.11.35 |
| Turn-OFF time | t_{OFF} | – | – | 15 | μs | $V_S = 13.5\text{V}$ ON=0 to 10% of V_S $R_L = 300\Omega$; $T_j = 25^\circ\text{C}$ | P_5.11.36 |

¹⁾ Not subject to production test, specified by design.

5.12 Low Side Switches

5.12.1 Functional Range

Table 40 Functional Range

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|---------------------------|------------------|--------|------|------------------|------|-----------------------|----------|
| | | Min. | Typ. | Max. | | | |
| Nominal Operating Voltage | V_S | 5.5 | – | 27 | V | – | P_5.12.1 |
| PWM Frequency of LS | f_{PWM} | – | – | 25 ¹⁾ | kHz | 2) | P_5.12.2 |

1) referring to a 47ohm series resistor to charge an external power mos gate

2) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.12.2 Electrical Characteristics

Table 41 Electrical Characteristics

$V_S = 5.5\text{ V}$ to 27 V , $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--------------------------------|-----------------------|--------|------|------|---------------|--|-----------|
| | | Min. | Typ. | Max. | | | |
| Overcurrent Limitation | I_{LSTyp} | 175 | 250 | 325 | mA | | P_5.12.3 |
| ON-State Resistance 150°C | R_{ON} | – | – | 10 | Ω | $V_S > 5.5\text{ V}$, $I_{\text{ds}} = 100\text{mA}$, $T_j = 150^\circ\text{C}$ | P_5.12.4 |
| ON-State Resistance 25°C | | – | 4 | – | Ω | $T_j = 25^\circ\text{C}$ | P_5.12.5 |
| Leakage Current | I_{leakage} | – | – | 2 | μA | $0\text{ V} < V_{\text{LS}} < V_S$; $T_j < 85^\circ\text{C}$ | P_5.12.6 |
| Turn ON Delay time, slow mode | $t_{\text{dOn-LS}}$ | – | – | 50 | μs | ¹⁾ LS_ON=1 to 0.9*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$ | P_5.12.7 |
| Turn ON Delay time, PWM mode | $t_{\text{dOn,f-LS}}$ | – | – | 0.5 | μs | LS_ON=1 to 0.9*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$ | P_5.12.8 |
| Turn ON fall time, PWM mode | $t_{\text{ONf,PWM}}$ | – | 1 | 1.25 | μs | $V_{\text{LS}} = 0.9*Vs$ to $0.1*Vs$ $V_S = 13.5\text{V}$, $R_L = 270\Omega$ | P_5.12.9 |
| Turn ON fall time, slow mode | $t_{\text{ONf,Slow}}$ | – | 100 | 150 | μs | ¹⁾ VLS 0.9*Vs to 0.1*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$ | P_5.12.10 |
| Turn OFF Delay time, slow mode | $t_{\text{dOff-LS}}$ | – | – | 50 | μs | ¹⁾ LS_ON=0 to 0.1*Vs $V_S = 13.5\text{V}$, $R_L = 270\Omega$ | P_5.12.11 |

Table 41 Electrical Characteristics (cont'd)

$V_S = 5.5 \text{ V to } 27 \text{ V}$, $T_j = -40^\circ \text{ C to } +150^\circ \text{ C}$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition | Number |
|--|-----------------|--------|------|------|---------------|---|-----------|
| | | Min. | Typ. | Max. | | | |
| Turn OFF Delay time, PWM mode | $t_{dOff,f-LS}$ | – | – | 2 | μs | LS_ON=0 to $0.1 \cdot V_S$ $V_S=13.5\text{V}$, $R_L=270\Omega$ | P_5.12.12 |
| Turn OFF Rise time, PWM mode | $t_{OFFR,PWM}$ | – | 1 | 1.25 | μs | $V_{LS} 0.1 \cdot V_S$ to $0.9 \cdot V_S$; $V_S=13.5\text{V}$, $R_L=270\Omega$ | P_5.12.13 |
| Turn OFF Rise time, slow mode | $t_{OFFR,Slow}$ | – | 100 | 150 | μs | ¹⁾ $V_{LS} 0.9 \cdot V_S$ to $0.9 \cdot V_S$; $V_S=13.5\text{V}$, $R_L=270\Omega$ | P_5.12.14 |
| Minimum Duty Cycle Pulse Width variation | ton_{MIN} | 1.5 | 2 | 3.5 | μs | $ton(dig) = 2\mu\text{s}^2$ | P_5.12.15 |
| Typical (systematic) Pulse Width increase LS_ON to VLS | $d ton_{TYP}$ | – | 1.25 | – | μs | $ton(dig) = 2\mu\text{s}^2$ | P_5.12.16 |
| Zener Clamp Voltage | V_{AZ} | – | 50 | – | V | values are valid at $T_j = 25^\circ\text{C}$ | P_5.12.17 |
| Clamping Energy (repetitive) | E_{clamp} | – | – | 2 | mJ | ²⁾ 1.000.000 cycles | P_5.12.18 |
| Clamping Energy | E_{clamp} | – | – | 14 | mJ | ²⁾ $T_{start} = 25^\circ\text{C}$ | P_5.12.19 |
| Clamping Energy (single), hot | E_{clamp} | – | – | 7 | mJ | ²⁾ 10 cycles, $T_{start} = 85^\circ\text{C}$ | P_5.12.20 |

1) Static ON mode (no PWM)

2) Not subject to production test, specified by design

6 Package Outlines

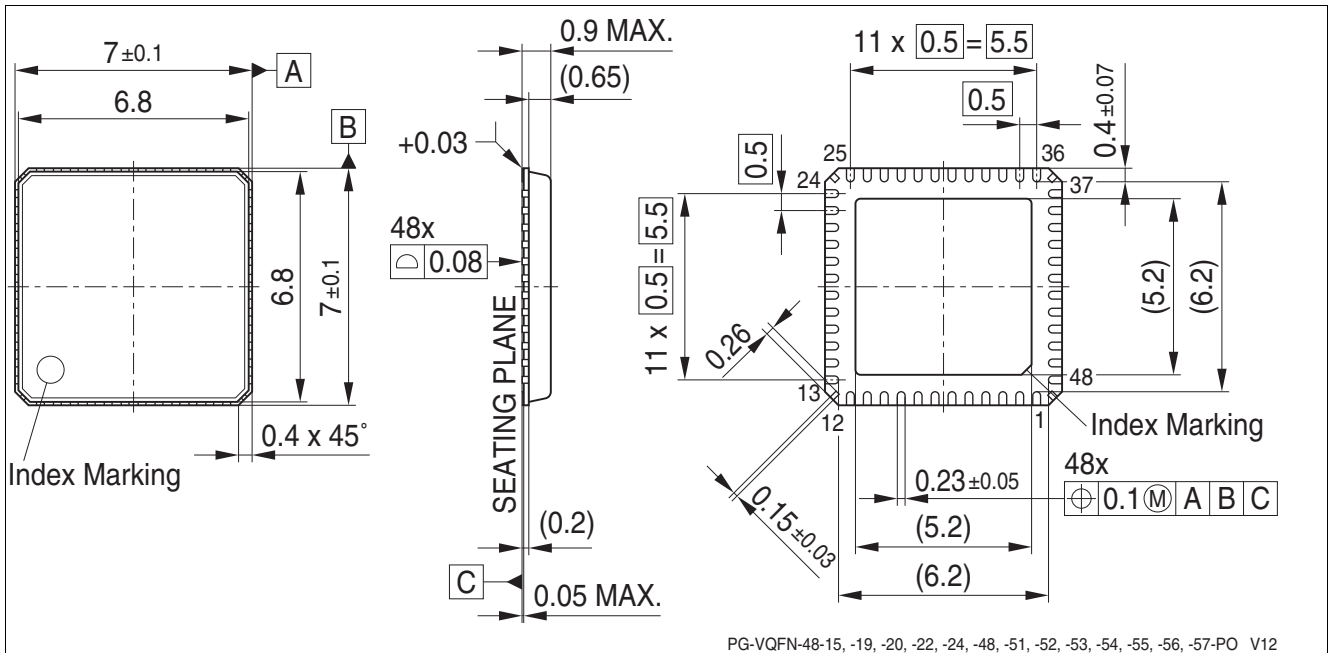


Figure 33 Package outline TLE9832-2QV, VQFN-48-22

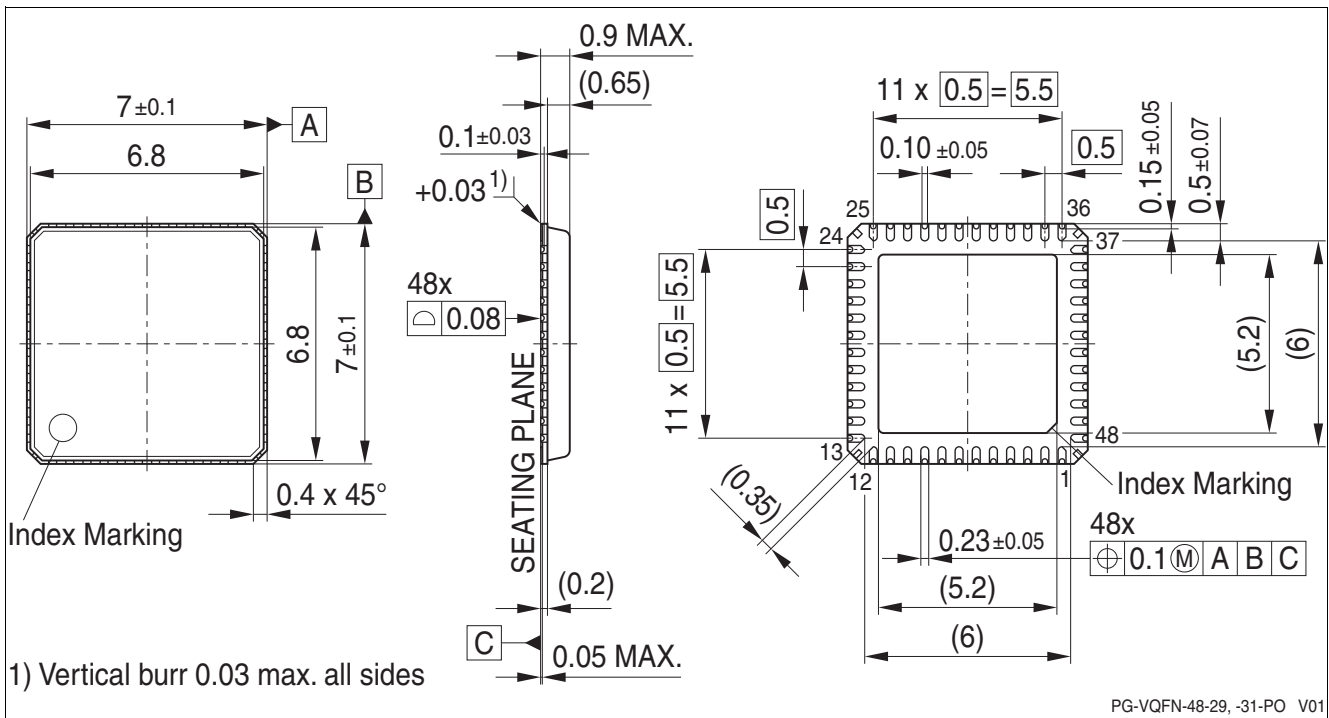


Figure 34 Package outline TLE9832-2QX, VQFN-48-29

Notes

1. You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.
2. Dimensions in mm.

7 Revision History

| Revision | Date | Changes |
|----------|------------|---|
| 1.1 | 2012-03-08 | Editorial Changes |
| 1.1 | 2012-03-08 | Added full package name (VQFN-48-22) |
| 1.1 | 2012-03-08 | Table 4: VDD1V5P: Power Mode configurations: added comment: "Power Down Supply" |
| 1.1 | 2012-03-08 | Table 5: Description of PMU Submodules: PMU-CYCMU description added and PMU-CMU changed from "cyclic" to "clock" management |
| 1.1 | 2012-03-08 | Table 30: Changed Value Max. from parameter "Common input voltage in differential mode" from V_{DD} to V_{DDP} |
| 1.1 | 2012-03-08 | Table 23: Changed Value Min. from parameter "Input voltage (amplitude) on XTAL1" from $0.3xV_{DDI}$ to $0.3xV_{DDP}$ |
| 1.1 | 2012-03-08 | Table 41: for "Turn ON..., Turn OFF..." Parameters changed Test condition from $R_L = 1k\Omega$ to $R_L = 270\Omega$ |
| 1.1 | 2012-03-08 | Table 14: - Removed "max" from the symbol suffixes - Corrected Symbol of Parameter "Input voltage at LIN" from V_{MONx} to V_{LIN} |
| 1.1 | 2012-03-08 | Table 41: Parameter "Overcurrent Limitation": - Renamed Parameter from "Typical on-state current" to "Overcurrent Limitation". - Added min. (175mA) and max (325mA) values - Removed Parameter "Overcurrent threshold accuracy". This information is added in the "Note/Test" Condition of the Parameter "Overcurrent Limitation" |
| 1.1 | 2012-03-08 | Table 19: - Renamed Parameter "Output Current" to "Specified Output Current" - Renamed Parameter "Output Capacitance" to "Required Output Capacitance" |
| 1.1 | 2012-03-08 | Table 20: - Renamed Parameter "Output Current" to "Specified Output Current" - Renamed Parameter "Output Capacitance" to "Required Output Capacitance" - Parameter "Dynamic Line Regulation": Correct typo in "Note/Test Condition" from V_{DDC} to V_{DDP} - Parameter "Output Voltage including line regulation @ Stop Mode": Value Max. changed from 1.01 to 1.15 |
| 1.1 | 2012-03-08 | Figure 31: Application Diagram updated |
| 1.1 | 2012-03-08 | Figure 29: Modul Block Diagram updated (replaced 500mA by 250mA) |
| 1.1 | 2012-03-08 | Table 27: Changed "Maximum Output Current" to "Nominal Output Current" in third row |
| 1.1 | 2012-03-08 | Table 14: Added "Output voltage VDDP" for $t < 100ms$, in Stop Mode only |
| 1.1 | 2012-03-08 | Chapter 4.1: Added disclaimer note |
| 1.1 | 2012-03-08 | Table 11: Changed value C_{VDDEXT} of blocking capacitor at VDDEXT pin to 100nF (from 10nF) |
| 1.1 | 2012-03-08 | Table 11 and Table 12: Changed headline from "External Component Requirements" to "External Component Recommendation" |

Revision History

| Revision | Date | Changes |
|----------|------------|---|
| 1.1 | 2012-03-08 | Table 14: - Renamed Parameter "Output voltage VDDP" to "Voltage VDDP" (2x) - Renamed Parameter "Output voltage VDDC" to "Voltage VDDC" |
| 1.1 | 2012-03-08 | Table 28: Added value LIN input capacity C_{LIN_IN} |

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2011-02-24

www.infineon.com