# EK79007

*Rev. 1.0*

PRELIMINARY DATA SHEET

## 1536-Output Source Driver with TCON MIPI/LVDS Interface

*fitipower integrated technology Inc.*

## Table of Contents

# Single Chip 1536 Channel Source Driver with Timing Controller for 1024(RGB) × 600 TFT LCD

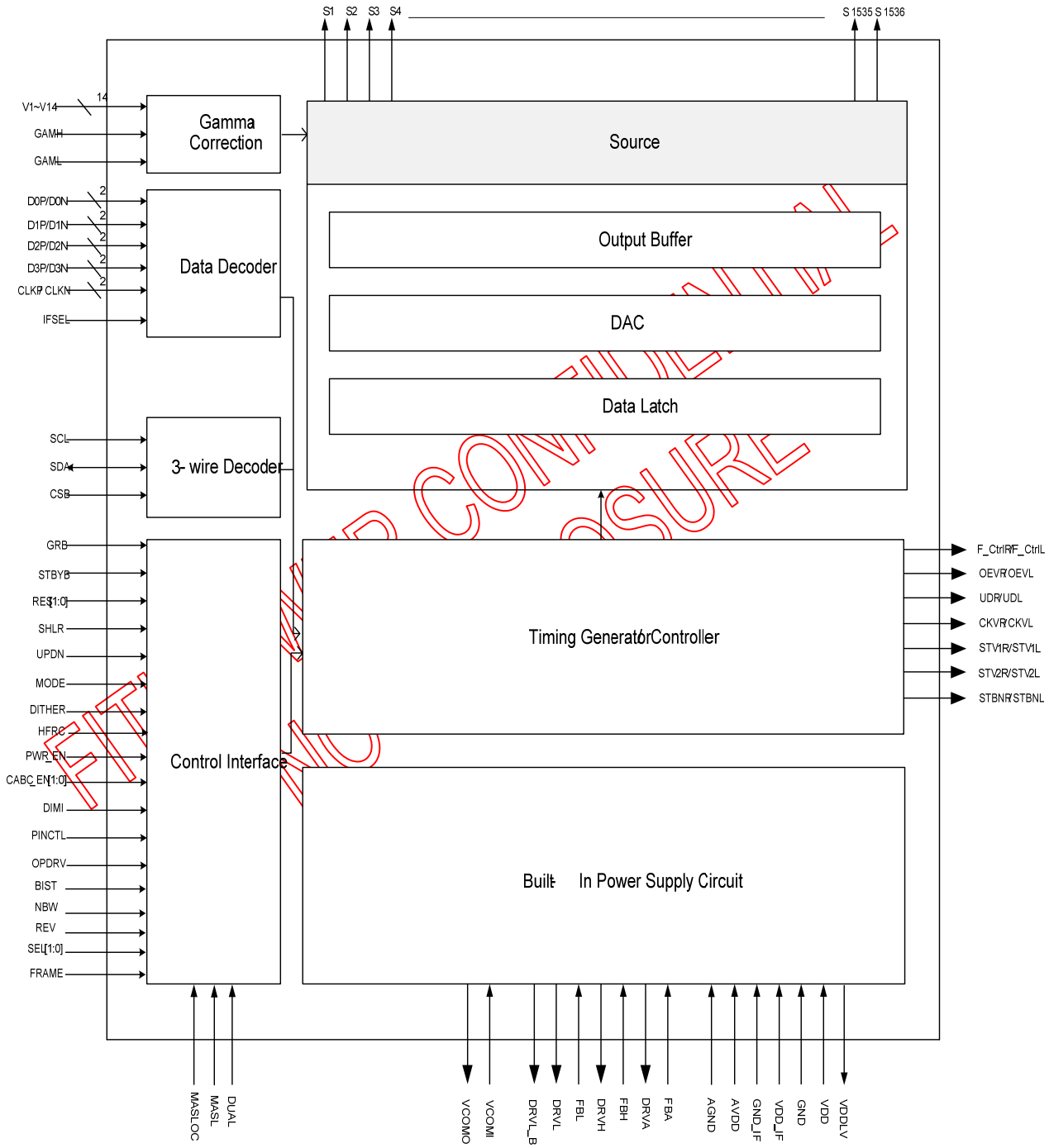
## 1. GENERAL DESCRIPTION

The EK79007is a highly integrated solution for small size to middle size a-Si TFT-LCD panels. This chip integrates 1536ch source driver with MIPI and LVDS input interface.

## 2. FEATURES

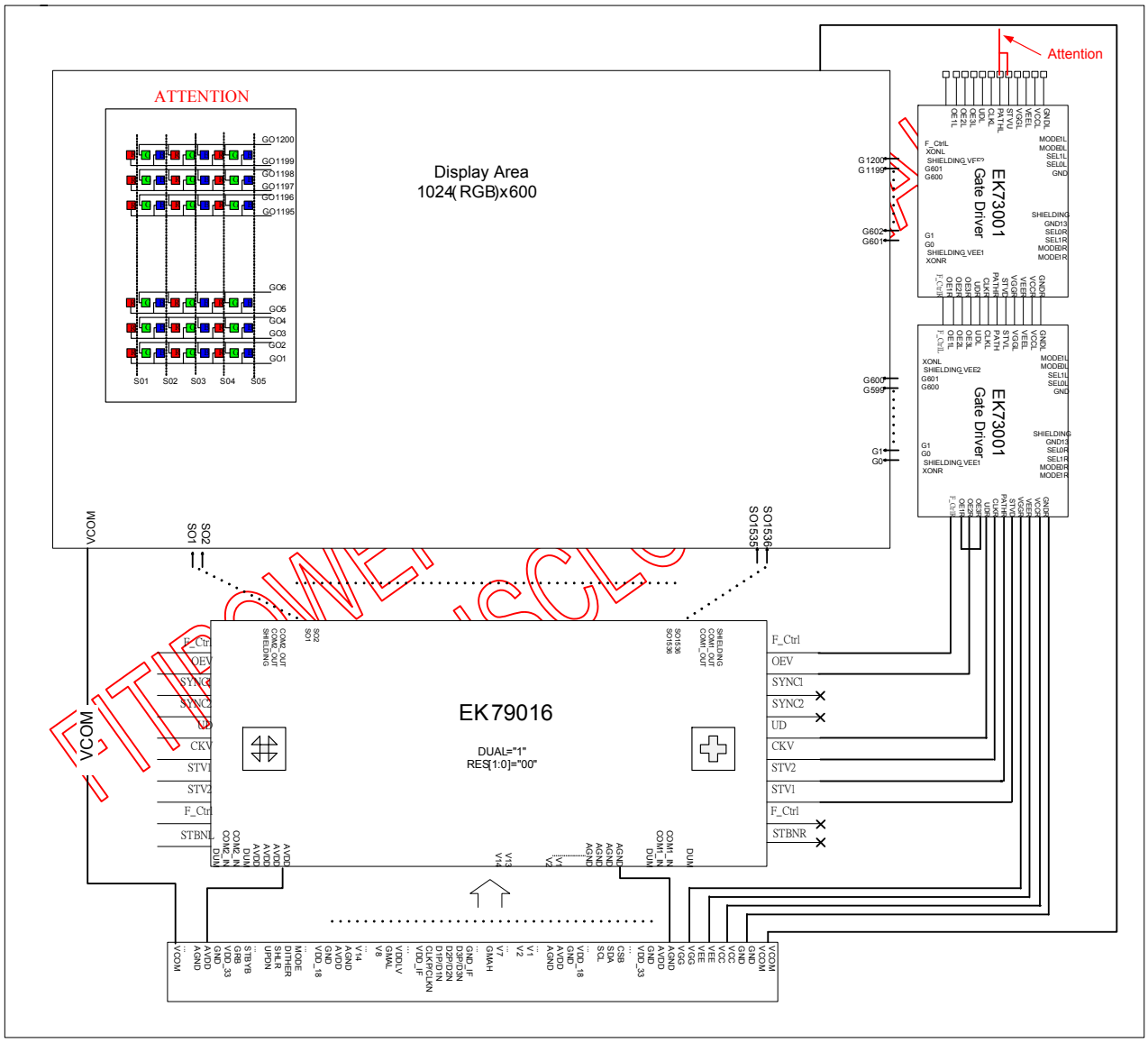
- Special design for middle size TFT LCD Panel with MIPI/LVDS interface
- Integrate 1536 channel source driver and timing controller with dual gate function
- Support cascade function with bidirectional shift control(CMOS signal)
- Support panel resolution (HxV):1024(RGB)x768, 1024(RGB)x600, 800(RGB)x600,800(RGB)x480
- 8-bit resolution 256 gray-scale with dithering(6-bits DAC +2 bits FRC or HFRC)
- Power for MIPI circuit(VDD_IF): 1.8V
- Power for digital circuit(VDD): 1.8V
- Power for analog circuit(AVDD): 8.0V ~ 13.5V
- Operating frequency: MIPI: 500Mbps (Max.) / LVDS: 71MHz (Max.)
- Embedded Gamma Table for special customer request
- V1~V14 for adjusting Gamma correction
- 1+2 dot inversion architecture
- Built-In PWM controller for AVDD, Charge pump for VGH / VGL , and VCOM buffer
- Built-In CABC function
- Built-In AUTO pattern
- Built-In SDRRS function
- Support no_clock detection
- Support GIP mode
- COG package
- Chip size = 25000um * 730um
- Output bump pitch = 15um

## 3. BLOCK DIAGRAM

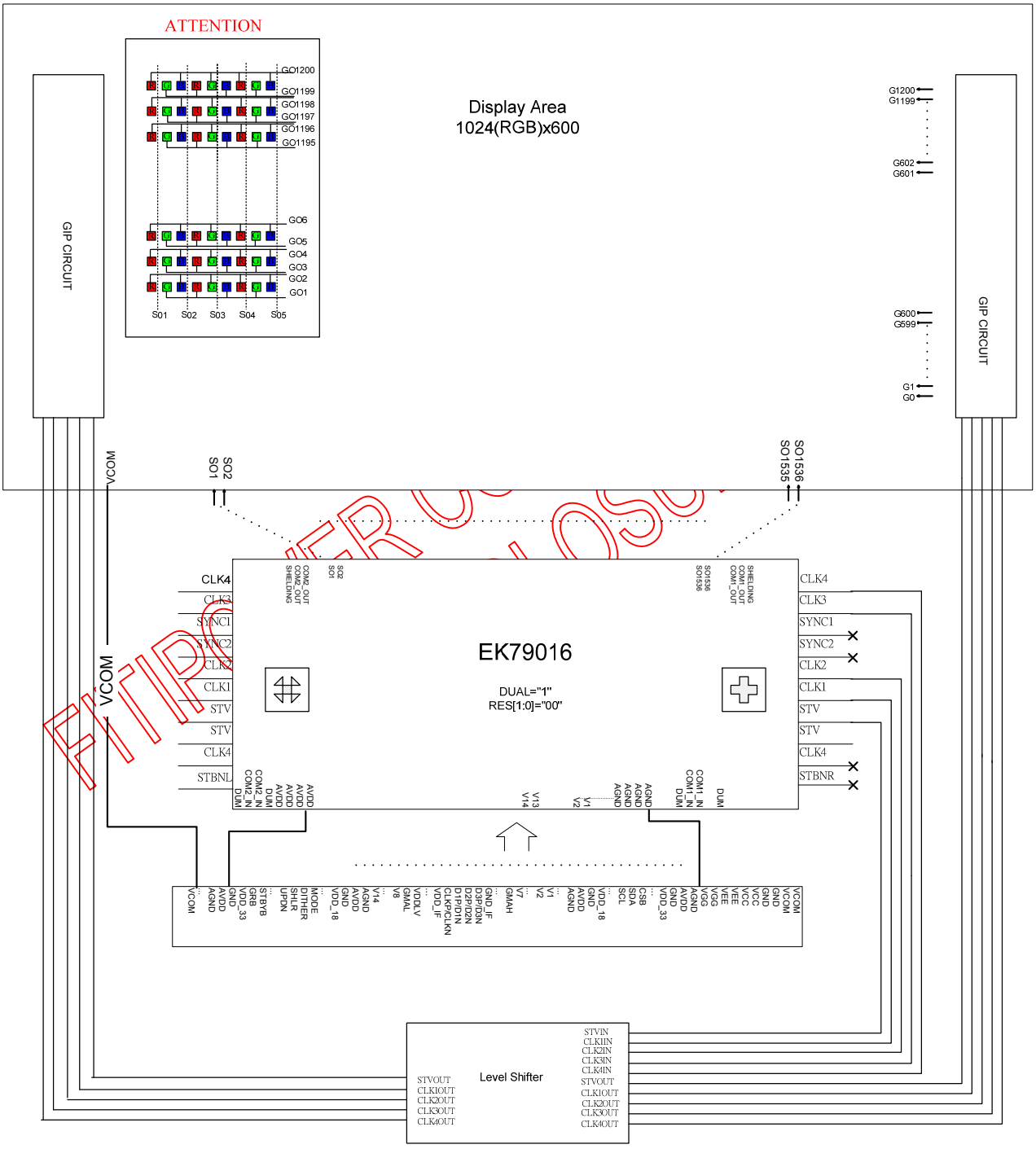


## 4. APPLICATION BLOCK DIAGRAM

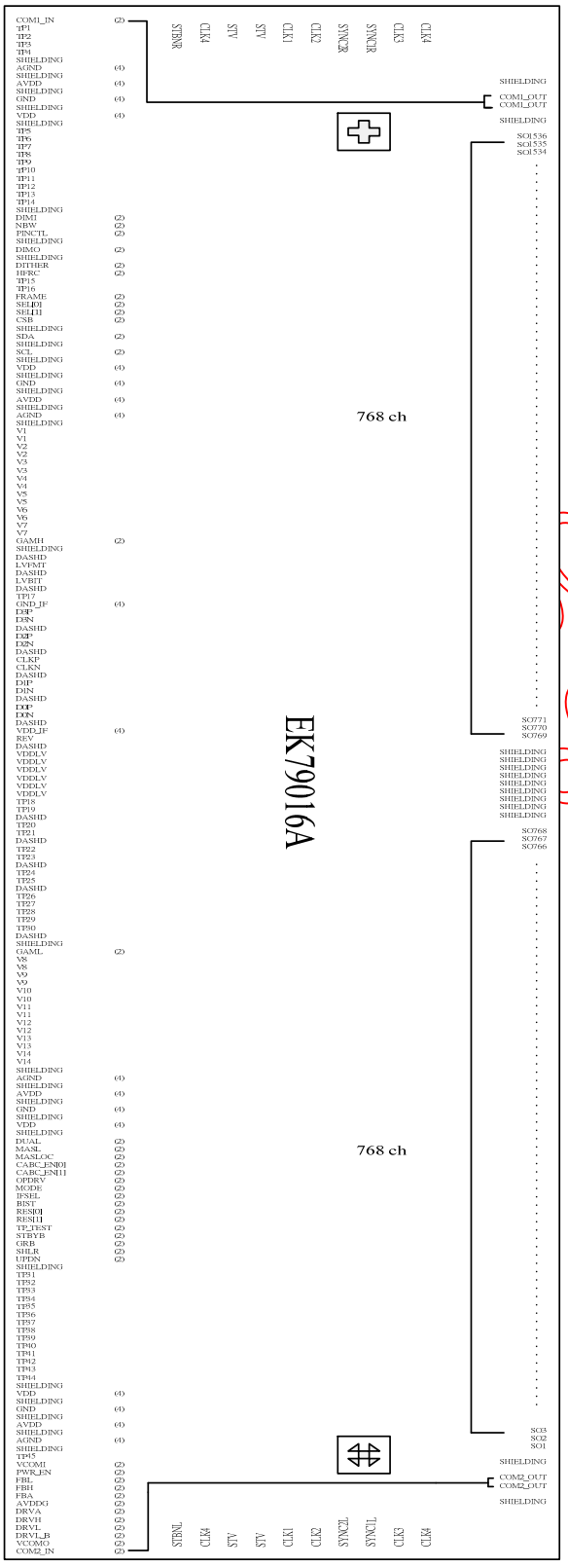
### 4.1. Dual Gate (1024RGB x 600)-non GIP panel



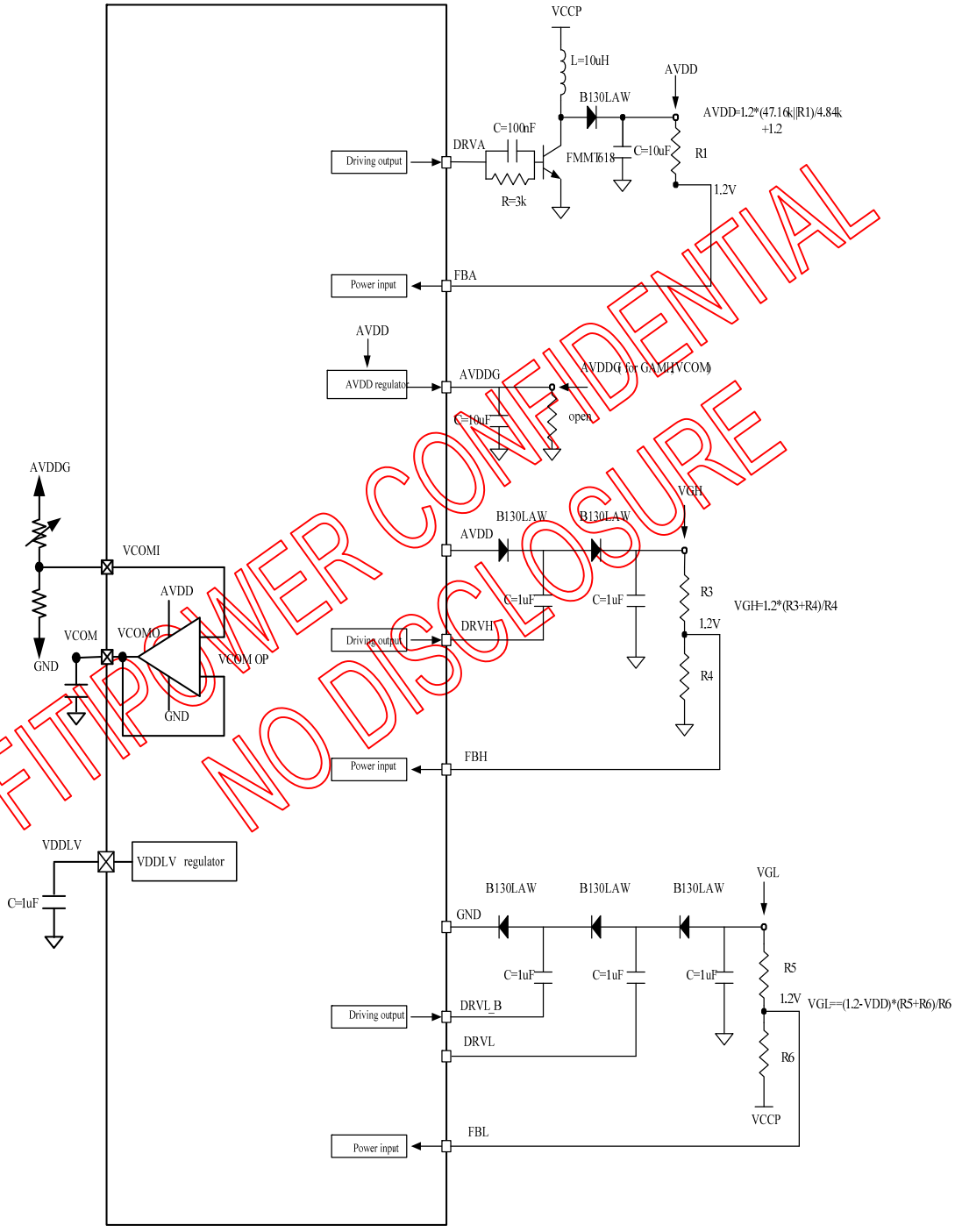
### 4.2. Dual Gate (1024RGB x 600)-GIP panel



## 5. PAD SEQUENCE



## 6. APPLICATION POWER CIRCUIT



## 7. PIN DESCRIPTION

| Pin Name | Pin Type | Description |
|---|---|---|
| D0P/D0N<br>D1P/D1N<br>D2P/D2N<br>D3P/D3N | Input | MIPI or LVDS data input. Select by “IFSEL” pin. |
| CLKP/CLKN | Input | MIPI or LVDS clock input. Select by “IFSEL” pin. |
| LVBIT | Input | 6-bit / 8-bit input select for LVDS mode.<br>LVBIT = ”L”, 6-bit.<br>LVBIT = ”H”, 8-bit.(default) |
| LVFMT | Input | 8-bit input format select for LVDS mode.<br>LVFMT = ”L”, VESA format.(default)<br>LVFMT = ”H”, JEIDA format. |
| MODE | Input | DE / HV mode select for LVDS mode.<br>MODE = ”H”,DE mode.(deafult)<br>MODE = ”L”,HV mode. |
| GIP_MODE | Input | GIP_MODE=”L”,External gate driver mode(default)<br>GIP_MODE=”H”,GIP_MODE. |
| IFSEL | Input | MIPI and LVDS Interface selection.<br>IFSEL = ”H”, LVDS interface.<br>IFSEL = ”L”, MIPI interface.(default) |
| RES[1:0] | Input | RES[1:0]=“01”,for 1024(RGB)*768 display resolution<br>RES[1:0]=“00”,for1024(RGB)*600 display resolution (default)<br>RES[1:0]=“10”,for 800(RGB)*600 display resolution<br>(601~936 channel disable )<br>RES[1:0]=“11”, for 800(RGB)*480 display resolution<br>(601~936 channel disable ) |
| DITHER | Input | Dithering function enable control.<br>DITHER = ”H”, Enable internal dithering function<br>DITHER = ”L”, Disable internal dithering function.(default). |
| HFRC | Input | H-FRC selection.<br>HFRC = ”L” : H-FRC disable(default)<br>HFRC = ”H” : H-FRC enable<br>If “DITHER”=”L”, disable dithering function(HFRC and FRC disable) |
| DUAL | Input | Dual Gate function enables control. Normally pull high<br>DUAL = ”H”, Enable Dual Gate Function. (Default)<br>DUAL = ”L”, TBD |
| V1~V14 | Input | When INTERNAL Gamma Table is used. GAMH tied to AVDDG , GAML tied to GND and V1~V14 pad are un-used.<br>When using external gamma voltage, GAMH and GAML are floating , and V1~V14 are the external gamma correction points. The voltage of these pins must be:<br>AGND<V14<V13<V12<V11<V10<V9<V8;V7<V6<V5<V4<V3<V2<V1< AVDD . |
| GAMH | Input | GMAH tied to AVDDG via when PWR_EN=H(enable internal PWM) or GMAH tied to AVDD via when PWR_EN=L(disable internal PWM) |
| GAML | Input | GMAL tied to GND via resistor. |
| GRB | Input | Global reset pin. Active Low to enter Reset State. Normally pull high.<br>Connecting with an RC reset circuit for stability. |

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>STBYB</td><td>Input</td><td>Standby mode.<br>STBYB = ”H”,normal operation(default)<br>STBYB = ”L”, timing controller, source driver will turn off, all output are High-Z.</td></tr>
<tr><td>SHLR</td><td>Input</td><td>Source right or left sequence control.<br>SHLR = ”L”, shift left: last data = S1←S2←S3…….←S1536 = first data.<br>SHLR = ”H”, shift right: first data = S1→S2→S3……..→S1536 = last data.(default)</td></tr>
<tr><td>UPDN</td><td>Input</td><td>Gate up or down scan control.<br>UPDN = ”L”, STV2 output vertical start pulse and UD pin output logical “L” to Gate driver. (default)<br>UPDN = ”H”, STV1 output vertical start pulse and UD pin output logical “H” to Gate driver</td></tr>
<tr><td>BIST</td><td>Input</td><td>Normal Operation/BIST pattern select.<br>BIST = ”H”: BIST(DCLK input is not needed)<br>BIST = ”L”: Normal Operation(default)</td></tr>
<tr><td>NBW</td><td>Input</td><td>Normally black or normally white setting.<br>NBW = ”H”: Normally black<br>NBW = ”L”: Normally white(default)</td></tr>
<tr><td>REV</td><td>Input</td><td>Controls whether the data of R[7:0]/G[7:0]/B[7:0] are inverted or not, normally pulled low.<br>When REV=”H”these data will be inverted. EX. “00”→“ 3F”, “07”→“ 38”, “15” →“2A”, and so on.</td></tr>
<tr><td>FRAME</td><td>Input</td><td>Frame inverse or not select. Normally pull low.<br>FRAME = ”H”, Uniform<br>FRAME = ”L”, Frame inverse (Default)</td></tr>
<tr><td>SEL[1:0]</td><td>Input</td><td>Gate on sequence select. Normally pull low
<table>
<tr><th>SEL[1]</th><th>SEL[0]</th><th>Pin control function</th></tr>
<tr><td>1</td><td>1</td><td>Z+2</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td>0</td><td>0</td><td>Z(default)</td></tr>
</table>
</td></tr>
<tr><td>OEVR/OEVL</td><td>Output</td><td>Gate driver control signal<br>When GIP_MODE =”H”,OEVR=OEVL=CLK3.</td></tr>
<tr><td>UDR/UDL</td><td>Output</td><td>Gate driver control signal<br>When GIP_MODE =”H”,UDR=UDL=CLK2.</td></tr>
<tr><td>CKVR/CKVL</td><td>Output</td><td>Gate driver control signal<br>When GIP_MODE =”H”,CKVR=CKVL=CLK1.</td></tr>
<tr><td>STV1R/STV1L</td><td>Output</td><td>Gate driver control signal<br>When GIP_MODE =”H”,STV1R=STV1L=STV.</td></tr>
<tr><td>STV2R/STV2L</td><td>Output</td><td>Gate driver control signal<br>When GIP_MODE =”H”,STV2R=STV2L=STV.</td></tr>
<tr><td>STBNR/STBNL</td><td>Output</td><td>Gate driver control signal</td></tr>
<tr><td>F_CtrlR/F_CtrlL</td><td>Output</td><td>Gate driver control signal (For special Gate on sequence).<br>In Dual Gate structure , connect this pin to gate driver’s F_Ctrl.<br>When GIP_MODE =”H”,F_CtrlR=F_CtrlL=CLK4.</td></tr>
<tr><td>CABC_EN[1:0]</td><td>Input</td><td>CABC H/W enable pin.<br>When CABC_EN=”00”, CABC OFF. (default)<br>When CABC_EN=”01”, User interface Image.<br>When CABC_EN=”10”, Still Picture.<br>When CABC_EN=”11”, Moving Image.</td></tr>
<tr><td>DIMI</td><td>Input</td><td>Brightness control signal. Normally pull high.</td></tr>
</table>

| Pin Name | Pin Type | Description |
|---|---|---|
| DIMO | Output | Backlight dimmer signal for external controller.<br>DIMO = ”L”, Turn off external backlight controller<br>DIMO = ”H”, Logical control signal to turn on external backlight controller<br>NOTE : If CABC OFF , DIMO = DIMI .<br>Else DIMO is controlled by CABC |
| PINCTL | Input | Enable pin control function. (for MIPI/LVDS IF)<br>PINCTL=”L”, Disable pin control function. The following pin will be inactive:<br>LVDS IF: SHLR,UPDN,MODE,LVFMT,LVBIT,HFRC,DITHER,BIST, RES[1:0],OPDRV,NBW,PWR_EN,REV,CABC_EN[1:0], FRAME.<br>MIPI IF:SHLR,UPDN,HFRC,DITHER,BIST,RES[1:0],,OPDRV,NBW, PWR_EN,CABC_EN[1:0], REV, FRAME.<br>PINCTL=”H”, Enable pin control function.(default)<br>NOTE: The related 3-wire control register bit control will be disabled under PINCTL=”H”. |
| OPDRV | Input | Source OP driving selection.<br>OPDRV = ”H” : 133%<br>OPDRV = ”L” : normal (default) |
| CSB | Input | Serial communication chip select for LVDS IF. Normally pull high |
| SDA | Input/Output | Serial communication data input for LVDS IF.. Normally pull low |
| SCL | Input | Serial communication clock input for LVDS IF.. Normally pull low |
| AVDD | PI | Power supply for analog circuits |
| AGND | PI | Ground pins for analog circuits |
| GND | PI | Ground pins for digital circuits |
| VDD | PI | Power supply for digital circuits |
| VDD_IF | PI | MIPI/LVDS power |
| GND_IF | PI | MIPI/LVDS ground |
| VDDLV | PO | VDDLP LDO output for MIPI LP mode TX use.<br>VDDLP LDO enable on MIPI Interface (IFSEL = ”L”).<br>VDDLP LDO disable on LVDS Interface (IFSEL = ”H”). |
| PWR_EN | Input | PWR_EN = ”H”, enable PWM, Charge pump and VCOM buffer<br>PWR_EN = ”L” , disable PWM, Charge pump and VCOM buffer(default) |
| FBA | VI | PWM controller feedback input. (for AVDD) |
| DRVA | Output | PWM output driver signal for the boost converter (for AVDD) |
| FBH | VI | Charge Pump controller feedback input. (for VGH) |
| DRVH | Output | Charge Pump driver signal for the boost converter (for VGH) |
| FBL | VI | Charge Pump controller feedback input. (for VGL) |
| DRVL | Output | Charge Pump driver signal for the boost converter (for VGL) |
| DRVL_B | Output | Inverse of DRVL(for VGL) |
| VCOMI | Input | VCOM buffer in |
| VCOMO | Output | VCOM buffer out |
| AVDDG | Output | AVDD regulator output |
| SO1~SO1536 | Output | Source Driver Output Signals<br>All outputs will be of unknown values under stand-by mode. |
| COM1_IN<br>COM1_OUT | S | Internal link together between input side and output side |
| COM2_IN<br>COM2_OUT | S | Internal link together between input side and output side. |
| SHIELDING | SH | Those pins are internally connected to the AGND.<br>DO NOT connect to any WOA on the panel.<br>Data Bus Shielding pad |

| Pin Name | Pin Type | Description |
|---|---|---|
| DASHD | SH | Those pins are internally connected to the GND.<br>RECOMMAND to add shielding lines on the FPC to reduce EMI. |
| TP1~TP45 | T | DO NOT connect to any WOA on the panel and floating on panel. |

Note:
P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output,
T: Testing, SH: Shielding, PS: Power Setting, C: Capacitor pin.

Pass Line Description:

| Pass Line No. | Pad Name | |
|---|---|---|
| 1 | COM1_IN | COM1_OUT |
| 2 | COM2_IN | COM2_OUT |



### 7.1. Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Source wiring:

| Pin name | Wiring resistance value(Ω) | Pin name | Wiring resistance value(Ω) |
|---|---|---|---|
| AVDD | <5 | FRAME | <100 |
| AGND | <5 | SEL[1:0] | <100 |
| VDD_IF | <5 | CSB | <100 |
| VDD | <5 | SDA | <100 |
| GND_IF | <5 | SCL | <100 |
| VDDLV | <5 | REV | <100 |
| GND | <5 | CABC_EN[1:0] | <100 |
| V1~V14 | <5 | OPDRV | <100 |
| DRVX | <5 | BIST | <100 |
| FBX | <5 | RES[1:0] | <100 |
| VCOMI | <5 | DCLKPOL | <100 |
| VCOMO | <5 | STBYB | <100 |
| D0P/D0N | <5 | GRB | <100 |
| D1P/D1N | <5 | SHLR | <100 |
| D2P/D2N | <5 | UPDN | <100 |
| D3P/D3N | <5 | PINCTL | <100 |
| CLKP/CLKN | <5 | DUAL(Reserved) | <100 |
| DIMI | <100 | MASL(Reserved) | <100 |
| DIMO | <100 | MASLOC(Reserved) | <100 |
| NBW | <100 | MODE(Reserved) | <100 |
| PINCTL | <100 | LVBIT | <100 |
| DITHER | <100 | LVFMT | <100 |
| IFSEL | <100 | | |
| HFRC | <100 | | |

Gate wiring:

| Pin name | Wiring resistance value(Ω) | Pin name | Wiring resistance value(Ω) |
|---|---|---|---|
| VGH | <50 | OEVX | <100 |
| VGL | <30 | UDX | <100 |
| VCC | <50 | CKVX | <100 |
| GND | <40 | STBNX | <100 |
| STV1X/STV2X | <100 | F_CtrlX | <100 |

## 8. MIPI INTERFACE (MOBILE INDUSTRY PROCESSING INTERFACE)

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

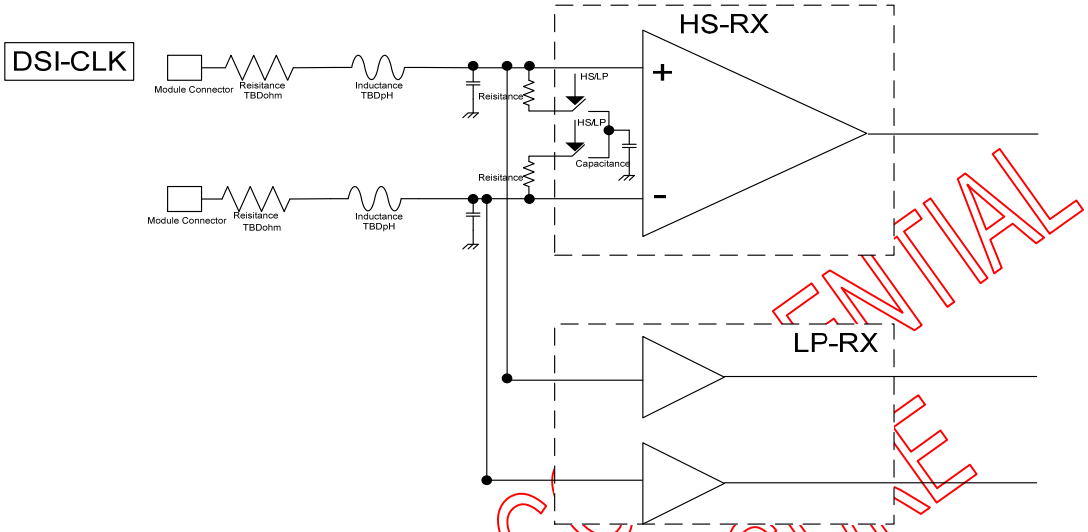
Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

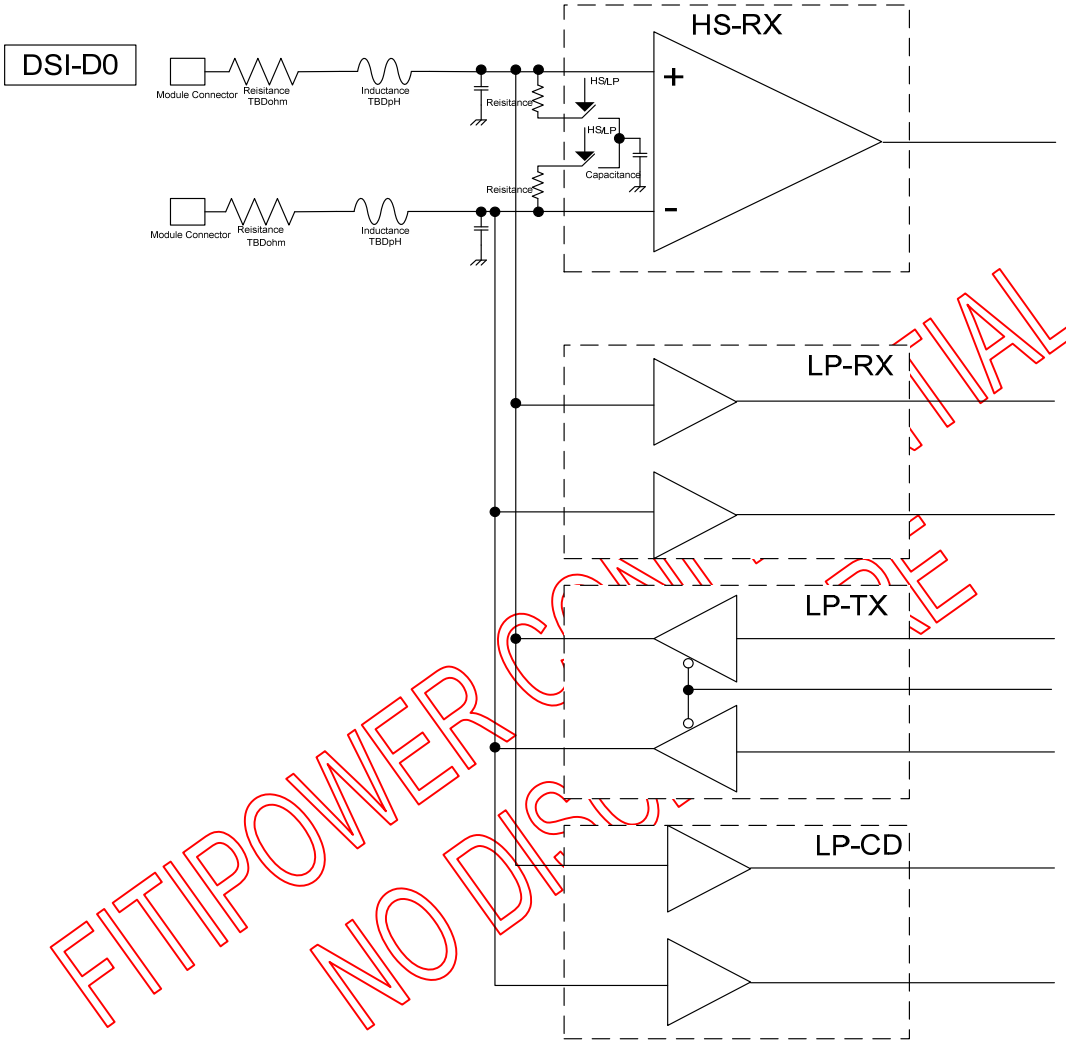
Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

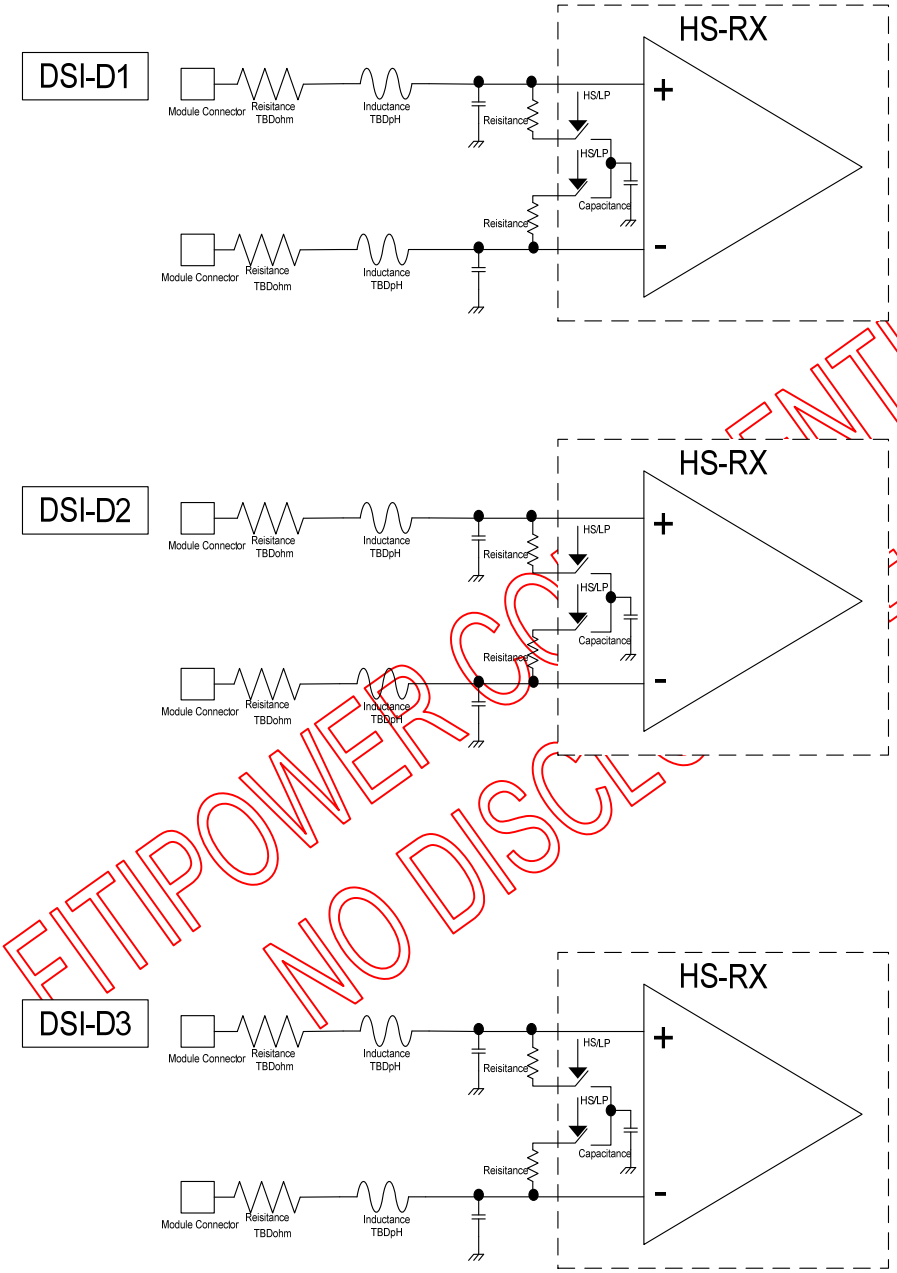
MIPI Lane Configuration:

| | MCU (Master) Display Module (Slave) |
|---|---|
| Clock Lane | Unidirectional Lane<br>• Clock Only<br>• Escape Mode(ULPS Only) |
| Data Lane0 | Bi-directional Lane<br>● Forward High-Speed<br>● Bi-directional Escape Mode<br>● Bi-directional LPDT |
| Data Lane1 | Unidirectional<br>● Forward High speed |
| Data Lane2 | Unidirectional<br>● Forward High speed |
| Data Lane3 | Unidirectional<br>● Forward High speed |

### 8.1. Display Module Pin Configuration for DSI







## 8.2. Display Serial Interface (DSI)

### 8.2.1. Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

**Transmission Packet Sequences**

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. These terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scanline during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero.

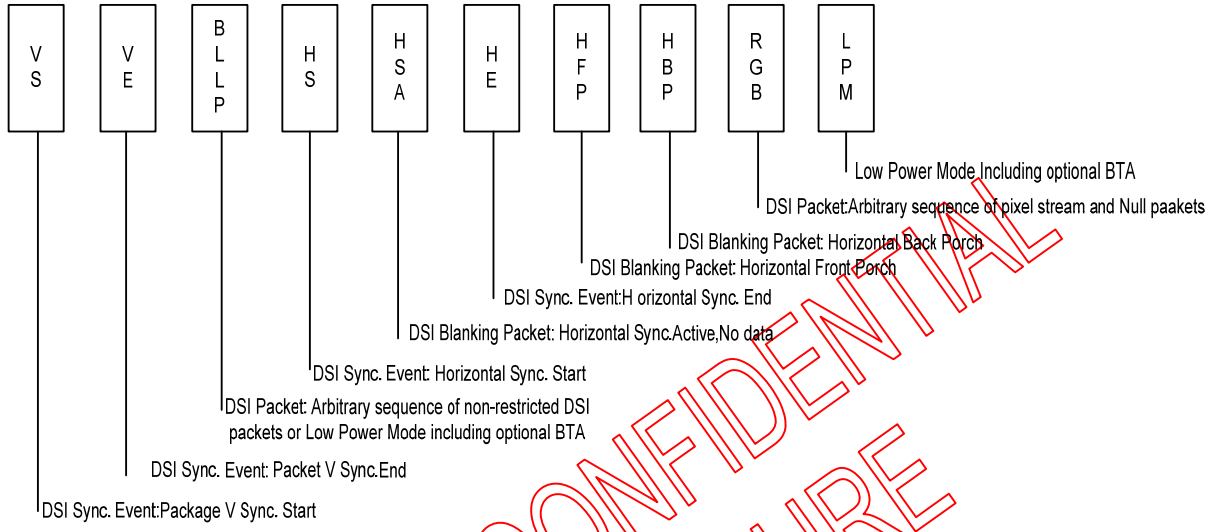
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX.
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode.
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode.
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode.
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID.

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. Individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.




**DSI Video Mode Interface Timing Legend**

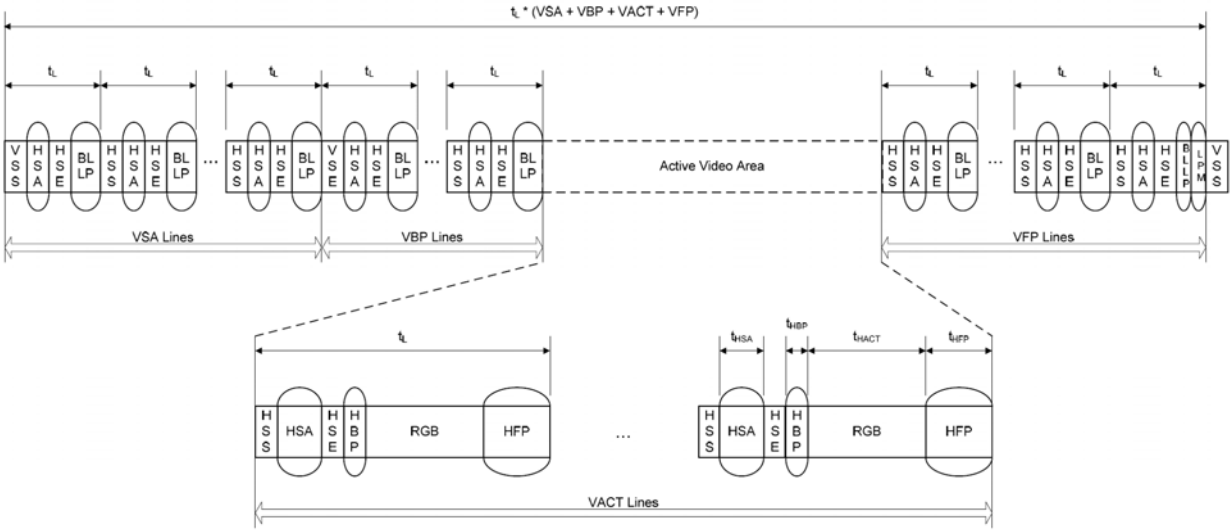
If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

**Clock Requirements**

A DSI host processor shall support continuous clock on the Clock Lane for display module that require it, so the host processor needs to keep the HS serial clock running.

**●Non-Burst Mode with Sync Pulses**

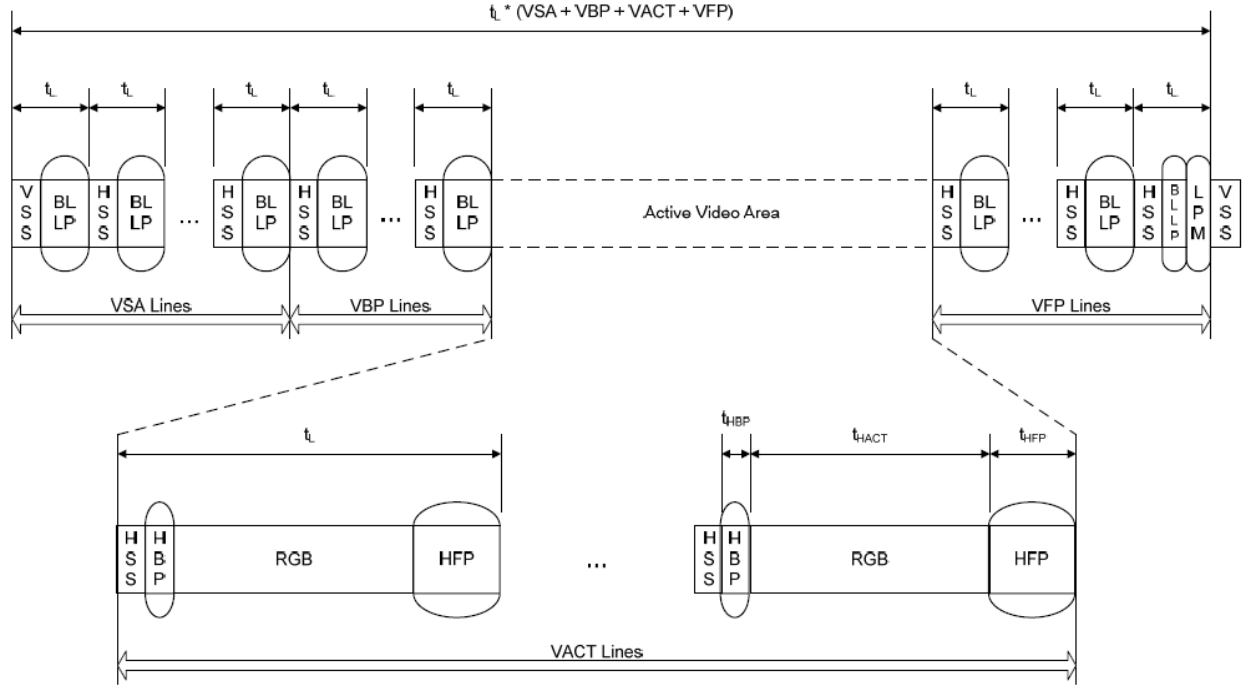
With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.




Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

**●Non-Burst Mode with Sync Events**

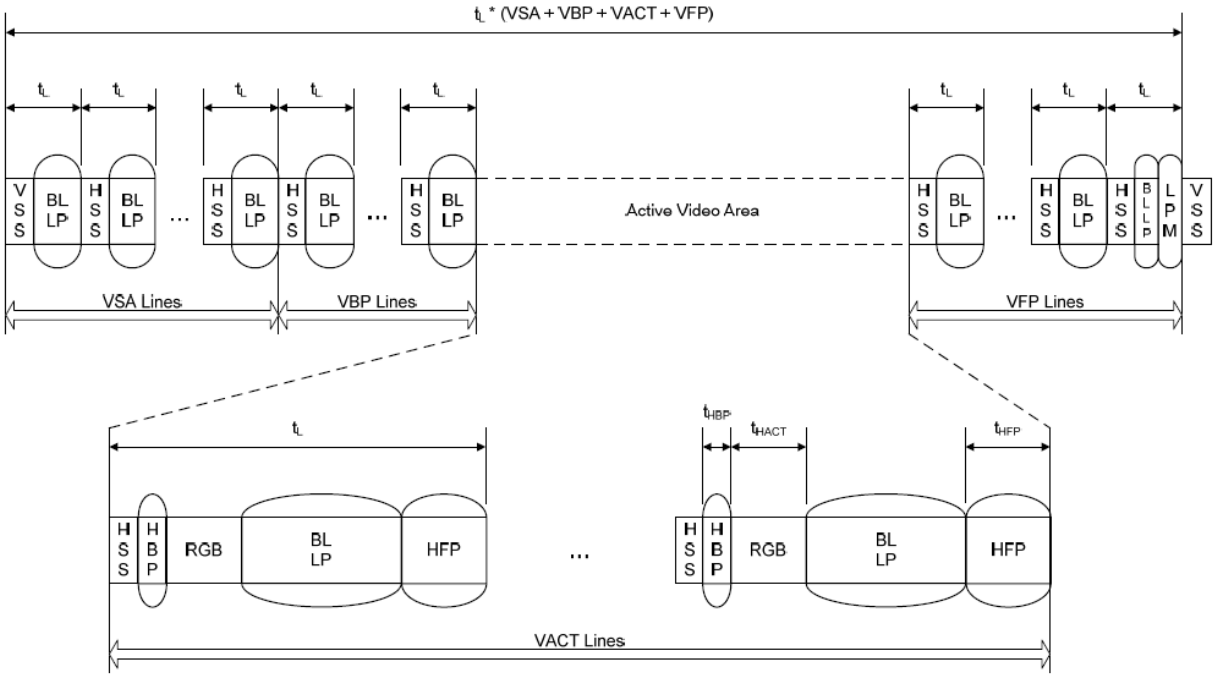
This mode is a simplification of the format described in section “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.




As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

- **Burst Mode**

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.




Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

## 9. COMMAND DESCRIPTION

### 9.1. MIPI Control Register

Following table list all the MIPI control registers and bit name definition for EK79007A. Refer to the next section for detail register function description, please.

Setting of all the MIPI registers will take effect at the coming valid Vsync signal except GRB bit.

All the MIPI control registers and bit name definition:

| | Register address | | | | | | | | | MSB | | | | | | | LSB | Default (hex) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | D7 | D6 | D5 | D4 | D3 | D2 | DI | DO | _ |
| R00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NOP | | | | | | | | _ |
| R01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | GRB | | | | | | | | _ |
| R05h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | RDNUMED(TBD) | | | | | | | | _ |
| R0Ah | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | GET_POWER_Mode | | | | | | | | _ |
| R0Dh | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | GET_DISPLAY_Mode | | | | | | | | _ |
| R0Eh | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | GET_SIGNAL_Mode(TBD) | | | | | | | | _ |
| R0Fh | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | RDDSDR(TBD) | | | | | | | | _ |
| R10h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | ENTER_SLEEP_MODE | | | | | | | | _ |
| R11h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | EXIT_SLEEP_MODE | | | | | | | | _ |
| R20h | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | EXIT_INVERT_MODE | | | | | | | | _ |
| R21h | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | ENTER_INVERT_MODE | | | | | | | | _ |
| R36h | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1/0 | 0 | 0 | 0 | 0 | 0 | 0 | UPDN(0) | SHLR(1) | 01 |
| R78h | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1/0 | GipStvDly_Len[7:0] | | | | | | | | C8 |
| R79h | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1/0 | GIPStvDly_Len[12:8] | | | | | | | | 00 |
| R7Ah | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1/0 | GipCkvDly_Len[7:0] | | | | | | | | 64 |
| R7Bh | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1/0 | GipCkvDly_Len[12:8] | | | | | | | | 00 |
| R80h | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1/0 | G2R[3:0] (1000) | | | | G1R[3:0] (1000) | | | | 88 |
| R81h | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1/0 | G4R[3:0] (1000) | | | | G3R[3:0] (1000) | | | | 88 |
| R82h | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1/0 | G6R[3:0] (1000) | | | | G5R[3:0] (1000) | | | | 88 |
| R83h | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1/0 | G8R[3:0] (1000) | | | | G7R[3:0] (1000) | | | | 88 |
| R84h | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1/0 | G10R[3:0] (1000) | | | | G9R[3:0] (1000) | | | | 88 |
| R85h | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1/0 | G12R[3:0] (1000) | | | | G11R[3:0] (1000) | | | | 88 |
| R86h | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1/0 | G14R[3:0] (1000) | | | | G13R[3:0] (1000) | | | | 88 |
| RB0h | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1/0 | PWR_EN(0) | – | – | – | – | – | – | – | 00 |
| RB1h | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1/0 | CABC_EN[1:0](00) | | HFRC(0) | DITHER(0) | BIST(0) | RES[1:0] (00) | | – | 00 |
| RB2h | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1/0 | – | NBW(0) | – | 2Lane_EN(0) | – | – | – | – | 00 |
| RB3h | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1/0 | – | – | – | – | – | FRAME(0) | SEL[1:0] | | 00 |

R00h: NOP ( No Operation)

| Address (MIPI I/F) | 00h | | | | | Access Attribute | | | W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 0 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | No Argument | | | | | | | | N/A |
| Description | This command performs no operation and is ignored by the device. | | | | | | | | |

R01h: GRB (Software Reset)

| Address (MIPI I/F) | 01h | | | | | Access Attribute | | | W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 0 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | No Argument | | | | | | | | N/A |
| Description | When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset register values and all source are set to GND (display off). | | | | | | | | |
| Restriction | (1)It will be necessary to wait 20 msec before sending new command following software reset.<br>(2)The display module loads all display supplier's factory default values to the registers during 5 msec. | | | | | | | | |

R05h: RDNUMED (reserved)

R0Ah: GET_POWER_MODE (Read Display Power Mode)

| Address (MIPI I/F) | 0Ah | | | | | Access Attribute | | | R |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00h |
| Description | D[4 ]:Sleep In/Out<br>"0" =Sleep Out, "1" =Sleep In | | | | | | | | |

R0Dh: GET_DISPLAY_MODE ( Read the Current Display Mode)

| Address (MIPI I/F) | 0Dh | | | | | Access Attribute | | | R |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00h |
| Description | D[5 ]:Inversion On/Off<br>"0" =Inversion off, "1" =Inversion on | | | | | | | | |

R0Eh: GET_SIGNAL_MODE (TBD)

| Address (MIPI I/F) | 0Fh | | | | | Access Attribute | | | R |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | No Argument | | | | | | | | 00h |
| Description | D[0]:Error on DSI<br>”1” :error, ”0” =no error | | | | | | | | |
| Restriction | - | | | | | | | | |

R0Fh:RDDSDR ( Read Display Self-Diagnostic Result)(TBD)

R10h: ENTER_SLEEP_MODE (Enter the Sleep-In Mode)

| Address (MIPI I/F) | 10h | | | | | Access Attribute | | | W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 0 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | No Argument | | | | | | | | Sleep In |
| Description | This command initiates the power-down sequence. The Sleep In profile will be executed when this command is received. | | | | | | | | |
| Restriction | This command has no effect when the display module is already in Sleep Mode. | | | | | | | | |

R11h: EXIT_SLEEP_MODE (Exit the Sleep-In Mode)

| Address (MIPI I/F) | 11h | | | | | Access Attribute | | | W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 0 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | No Argument | | | | | | | | Sleep In |
| Description | This command initiates the power-up sequence. The Sleep Out will load register value. It will be necessary to wait 5 msec before sending next command. | | | | | | | | |
| Restriction | This command will not cause any visible effect on the display when the display is not in Sleep. | | | | | | | | |

R20h:EXIT_INVERT_MODE (Display Inversion Off)

| Address (MIPI I/F) | 20h | | | | | Access Attribute | | | W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 0 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | No Argument | | | | | | | | Inversion Off |
| Description | This command is used to recover from display reverse mode and does not change any other status. | | | | | | | | |
| Restriction | This command has no effect when the module is already in inversion off mode. | | | | | | | | |

R21h: ENTER_INVERT_MODE (Display Inversion On)

| Address (MIPI I/F) | 21h | | | | | Access Attribute | | | W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 0 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default value |
| | No Argument | | | | | | | | Inversion Off |
| Description | This command is used to enter display Inversion mode and does not change any other status. To exit from Display Inversion on, the Display Inversion off command (20h) should be written. | | | | | | | | |
| Restriction | This command has no effect when the module is already in inversion on mode. | | | | | | | | |

R36h: SET_ADDRESS_MODE (Data Access Control)

| Address (MIPI I/F) | 36h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | 0 | 0 | 0 | 0 | 0 | 0 | UPDN | SHLR | 01h |
| Description | UPDN: Gate up or down scan control.<br>UPDN = "0" , STV2 output vertical start pulse and UD pin output logical "0" to Gate driver.(default)<br>UPDN = "1" , STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.<br>SHLR: Source right or left sequence control.<br>SHLR = "0" , shift left: last data = S1←S2←S3…….←S1200 = first data.<br>SHLR = "1" , shift right: first data = S1→S2→S3…….→S1200 = last data. (default) | | | | | | | | |

R78h/R79h/R7Ah/R7Bh :GIP timing control register

| Address | Description | | Default(hex) |
|---|---|---|---|
| R78h | GipStvDly_Len[7:0] | | C8 |
| R79h | – | GIPStvDly_Len[12:8] | 00 |
| R7Ah | GipCkvDly_Len[7:0] | | 64 |
| R7Bh | – | GipCkvDly_Len[12:8] | 00 |

R80h: Gamma Control Register

| Address (MIPI I/F) | 80h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G2R | | | | G1R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

R81h: Gamma Control Register

| Address (MIPI I/F) | 81h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G4R | | | | G3R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

R82h: Gamma Control Register

| Address (MIPI I/F) | 82h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G6R | | | | G5R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

R83h: Gamma Control Register

| Address (MIPI I/F) | 83h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G8R | | | | G7R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

R84h: Gamma Control Register

| Address (MIPI I/F) | 84h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G10R | | | | G9R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

R85h: Gamma Control Register

| Address (MIPI I/F) | 85h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G12R | | | | G11R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

R86h: Gamma Control Register

| Address (MIPI I/F) | 86h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | G14R | | | | G13R | | | | 88h |
| Description | Gamma voltage setting. | | | | | | | | |

RB0h: Panel Control Register

| Address (MIPI I/F) | B0h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | PWR_EN (0) | – | – | – | – | – | – | – | 00h |
| Description | PWR_EN: POWER enable.<br>PWR_EN = "1" , enable PWM , Charge pump and VCOM buffer<br>PWR_EN = "0" , disable PWM , Charge pump and VCOM buffer (Default) | | | | | | | | |

RB1h: Panel Control Register

| Address (MIPI I/F) | B1h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | CABC_EN[1:0] (00) | | HFRC (0) | DITHER (0) | BIST (0) | RES[1:0] (00) | | – | 00h |
| Description | CABC_EN[1:0]:CABC H/W enable pin.<br>When CABC_EN=”00” , CABC OFF. (Default mode)<br>When CABC_EN=”01” , User interface Image.<br>When CABC_EN=”10” , Still Picture.<br>When CABC_EN=”11” , Moving Image<br>HFRC: H-FRC selection.<br>HFRC = ”1” : H-FRC enable<br>HFRC = ”0” : H-FRC disable (Default)<br>If DITHER=”0” ,disable dithering function(H-FRC and FRC disable)<br>DITHER: Dithering function enable control.<br>DITHER = ”1” , Enable internal dithering function<br>DITHER = ”0” , Disable internal dithering function (Default)<br>BIST: Normal Operation/BIST pattern select.<br>BIST = ”1” : BIST(DCLK input is not needed)<br>BIST = ”0” : Normal Operation (Default)<br>RES[1:0]: = ”01” , for 1024(RGB)*768 display resolution<br>= ”00” , for 1024(RGB)*600 display resolution (default)<br>= ”10” , for 800(RGB)*600 display resolution<br>(601~936 channel disable )<br>= ”11” , for 800(RGB)*480 display resolution<br>(601~936 channel disable ) | | | | | | | | | |

RB2h: Panel Control Register

| Address (MIPI I/F) | B2h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | – | NBW (0) | – | 2Lane_EN (0) | – | – | – | – | 00h |
| Description | NBW: Normally black or normally white setting.<br>NBW=”1” : Normally black.<br>NBW=”0” : Normally white(default).<br>2Lane_EN: 2 lane/4 lane setting<br>2Lane_EN=”0”:4 lane(default)<br>2Lane_EN=”1”:2 lane | | | | | | | | |

RB3h: Panel Control Register(non GIP mode)

| Address (MIPI I/F) | B2h | | | | | Access Attribute | | | R/W |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Number of Parameter(s) | | | 1 |
| Parameter | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | Default Value |
| | – | – | – | – | – | FRAME (0) | SEL[1:0] (00) | | 00h |
| Description | FRAME: Frame inverse or not select.<br>FRAME = ”1” , Uniform<br>FRAME = ”0” , Frame inverse(Default)<br><br>SEL[1:0]:Gate on sequence select. | | | | | | | | |

| SEL[1] | SEL[0] | Pin control function |
|---|---|---|
| 1 | 1 | Z+2 |
| 1 | 0 | 2 |
| 0 | 1 | 2 |
| 0 | 0 | Z(default) |

### 9.2. 3-Wire Serial Port Interface (Only For LVDS Mode)

#### 9.2.1. 3-Wire Command Format

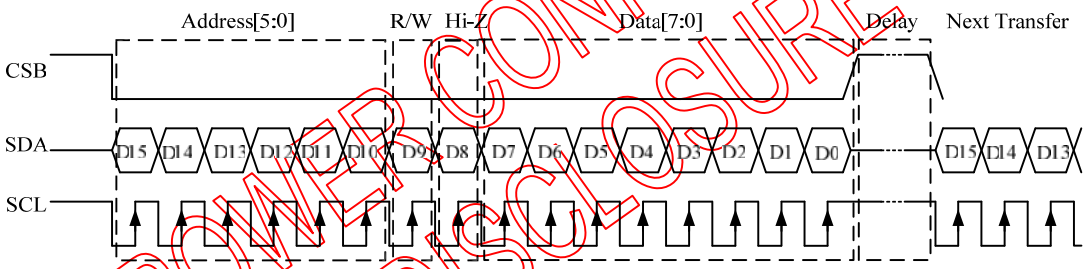
EK79007use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK790073-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register, Please refer to the section of “3-Wire Timing.




3-Wire Command Format:

| Bit | Description |
|---|---|
| D15~D10 | Register Address [5:0]. |
| D9 | W/R control bit. “0” for Write; “1” for Read |
| D8 | Hi-Z bit during read mode. Any data within this bits will be ignored during write mode |
| D7~D0 | Data for the W/R operation to the address indicated by Address phase |

3-Wire Write Format:

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Register Address[5:0] | | | | | | 0 | X | Data(Issue by external controller) | | | | | | | |

3-Wire Read Format:

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Register Address[5:0] | | | | | | 1 | Hi-Z | Data(Issue by 3-wire engine) | | | | | | | |

### 9.2.2. 3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for EK79007A. Refer to the next section for detail register function description please.
Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address (Hex) | Address | | | | | | R/W | Command Setting | | | | | | | | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 1/0 | PWR_EN (0) | – | SHLR(1) | UPDN(0) | STBYB(1) | GRB(1) | – | MODE(1) | 2d |
| 01 | 0 | 0 | 0 | 0 | 0 | 1 | 1/0 | CABC(00) | | HFRC(0) | DITHER(0) | BIST(0) | RES(00) | | – | 00 |
| 02 | 0 | 0 | 0 | 0 | 1 | 0 | 1/0 | – | NBW(0) | – | – | – | – | LVFMT(0) | LVBIT(1) | 01 |
| 03 | 0 | 0 | 0 | 0 | 1 | 1 | 1/0 | – | – | – | – | REV(0) | FRAME(0) | SEL[1:0](00) | | 00 |
| 16 | 0 | 1 | 0 | 1 | 1 | 0 | 1/0 | GipStvDly_Len[7:0] | | | | | | | | 80 |
| 17 | 0 | 1 | 0 | 1 | 1 | 1 | 1/0 | – | | | | GIPStvDly_Len[12:8] | | | | 00 |
| 18 | 0 | 1 | 1 | 0 | 0 | 0 | 1/0 | GipCkvDly_Len[7:0] | | | | | | | | 40 |
| 19 | 0 | 1 | 1 | 0 | 0 | 1 | 1/0 | – | | | | GipCkvDly_Len[12:8] | | | | 00 |
| 1E | 0 | 1 | 1 | 1 | 1 | 0 | 1/0 | G2R[3:0] (1000) | | | | G1R[3:0] (1000) | | | | 88 |
| 1F | 0 | 1 | 1 | 1 | 1 | 1 | 1/0 | G4R[3:0] (1000) | | | | G3R[3:0] (1000) | | | | 88 |
| 20 | 1 | 0 | 0 | 0 | 0 | 0 | 1/0 | G6R[3:0] (1000) | | | | G5R[3:0] (1000) | | | | 88 |
| 21 | 1 | 0 | 0 | 0 | 0 | 1 | 1/0 | G8R[3:0] (1000) | | | | G7R[3:0] (1000) | | | | 88 |
| 22 | 1 | 0 | 0 | 0 | 1 | 0 | 1/0 | G10R[3:0] (1000) | | | | G9R[3:0] (1000) | | | | 88 |
| 23 | 1 | 0 | 0 | 0 | 1 | 1 | 1/0 | G12R[3:0] (1000) | | | | G11R[3:0] (1000) | | | | 88 |
| 24 | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 | G14R[3:0] (1000) | | | | G13R[3:0] (1000) | | | | 88 |

R00h: System Control Register

| Designation | Address | Description |
|---|---|---|
| Mode | R00[0] | DE/SYNC mode select.<br>MODE = 0: HSD/VSD mode<br>MODE = 1: DE mode(default) |
| GRB | R00[2] | Global reset bit.<br>GRB = 0: The controller is in reset state<br>GRB = 1: Normal operation. (Default) |
| STBYB | R00[3] | Standby mode selection bit<br>STBYB= 0: Timing control, driver and DC-DC converter, are off, and all outputs are High-Z.<br>STBYB= 1: Normal operation. (Default) |
| UPDN | R00[4] | Gate Up or Down scan control.<br>UPDN = 0: STV2 output vertical start pulse and UD pin output logical “0” to Gate driver.<br>UPDN = 1: STV1 output vertical start pulse and UD pin output logical “1” to Gate driver. (Default) |
| SHLR | R00[5] | Right/Left sequence control of source driver.<br>SHLR= 0:Shift left: Last data = S1<S2<S3…<S1200=First data<br>SHLR= 1:Shift right: First data = S1<S2<S3…<S1200=Last data(Default) |
| PWR_EN | R00[7] | POWER enable.<br>PWR_EN =1: enable PWM , Charge pump and VCOM buffer<br>PWR_EN =0: disable PWM , Charge pump and VCOM buffer (Default) |

R01h: System Control Register

| Designation | Address | Description |
|---|---|---|
| RES[1:0] | R01[2:1] | RES[1:0] = 01: for 1024(RGB)*768 display resolution<br>RES[1:0] = 00: for 1024(RGB)*600 display resolution (default)<br>RES[1:0] = 10: for 800(RGB)*600 display resolution (601~936 channel disable)<br>RES[1:0] = 11: for 800(RGB)*480 display resolution (601~936 channel disable) |
| BIST | R01[3] | Normal Operation/BIST pattern select.<br>BIST = 1: BIST(DCLK input is not needed)<br>BIST = 0: Normal Operation (Default) |
| DITHER | R01[4] | Dithering function enable control.<br>DITHER = 1: Enable internal dithering function<br>DITHER = 0: Disable internal dithering function (Default) |
| HFRC | R01[5] | H-FRC selection.<br>HFRC = 1: H-FRC enable<br>HFRC = 0: H-FRC disable (Default)<br>If DITHER= 0:disable dithering function(H-FRC and FRC disable) |
| CABC_EN[1:0] | R01[7:6] | When CABC_EN =00: CABC OFF. (Default mode)<br>When CABC_EN =01: User interface Image.<br>When CABC_EN =10: Still Picture.<br>When CABC_EN=11: Moving Image |

R02h: System Control Register

| Designation | Address | Description |
|---|---|---|
| LVBIT | R02[0] | 6-bit / 8-bit input select for LVDS mode.<br>LVBIT = 0:6-bit.<br>LVBIT = 1: 8-bit.(default) |
| LVFMT | R02[1] | 8-bit input format select for LVDS mode.<br>LVFMT = 0: VESA format.(default)<br>LVFMT = 1: JEIDA format. |
| NBW | R02[6] | Normally black or normally white setting.<br>NBW =1: Normally black.<br>NBW =0: Normally white(default) |

R03h: System Control Register

| Designation | Address | Description |
|---|---|---|
| SEL[1:0] | R03[1:0] | Gate on sequence select.<br>SEL[1] / SEL[0] / Pin control function<br>1 / 1 / Z+2<br>1 / 0 / 2<br>0 / 1 / 2<br>0 / 0 / Z(default) |
| FRAME | R03[2] | Frame inverse or not select.<br>FRAME =1: Uniform<br>FRAME =0: Frame inverse(Default) |
| REV | R03[3] | Controls whether the data of R[7:0]/G[7:0]/B[7:0] are inverted or not.<br>When REV="0" these data will be inverted. EX. "00"→" 3F", "07"→" 38", "15"→ "2A", and so on. |

R16h/R17h/R18h/R19h: GIP Timing Control Register

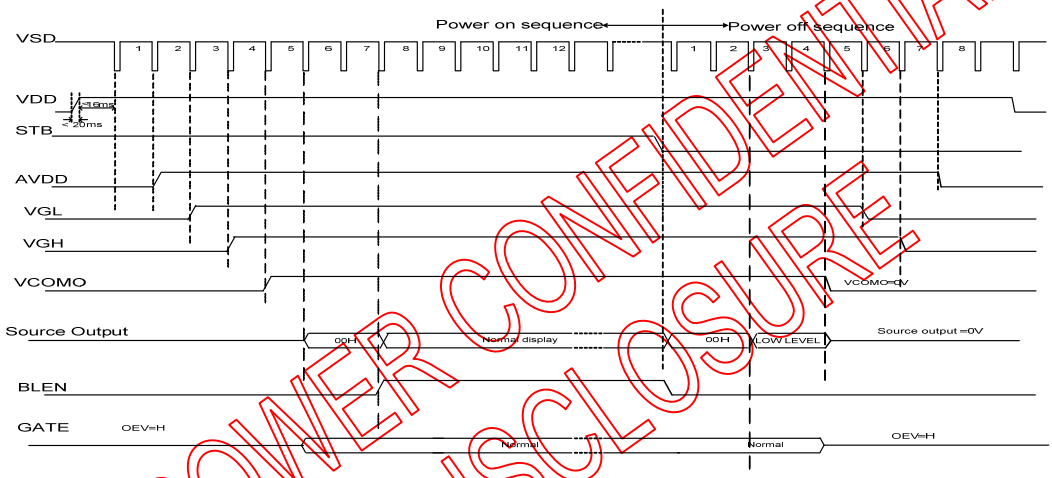
| Address | Description | | Default(hex) |
|---|---|---|---|
| R16h | GipStvDly_Len[7:0] | | 80h |
| R17h | – | GIPStvDly_Len[12:8] | 00h |
| R18h | GipCkvDly_Len[7:0] | | 40h |
| R19h | – | GipCkvDly_Len[12:8] | 00h |

## 10. FUNCTION DESCRIPTION

### 10.1. Power On/Off Sequence

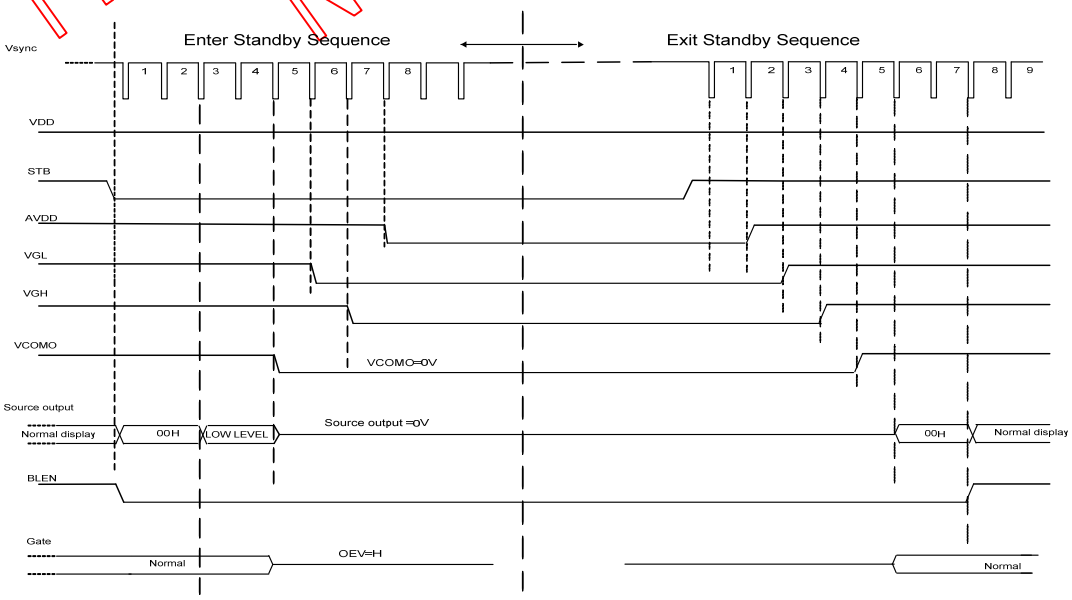
In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.

#### 10.1.1. Power On/Off Sequence





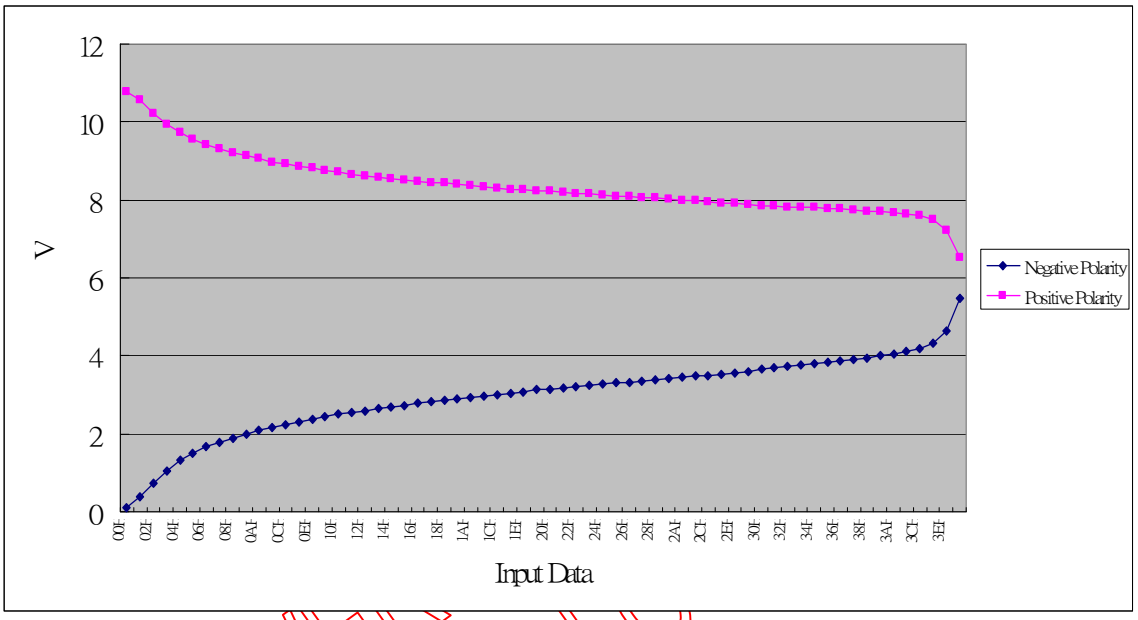

#### 10.1.2. Enter and Exit Sleep Mode Sequence




Note: Low Level=3Fh, when NBW=”L” (Normally white)
Low Level=00h, when NBW=”H” (Normally Black)

### 10.2. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.




Remark: AVDD-0.1 > V1 > V2> V3 > V4 > V5 > V6 > V7; V8 > V9 > V10 > V11 > V12 > V13 > V14 > AGND+0.1V

### 10.3. Input Data and Output Voltage Reference Table

**Input Data and Output Voltage Reference Table**

@AVDD=11V

| V1 | V2 | V3 | V4 | V5 | V6 | V7 | V8 | V9 | V10 | V11 | V12 | V13 | V14 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10.78 | 10.569 | 8.708 | 8.213 | 7.866 | 7.243 | 6.51 | 5.49 | 4.63 | 3.653 | 3.146 | 2.493 | 0.373 | 0.11 | V |

| Data | Positive |
|---|---|
| 00H | AVDD×0.980 |
| 01H | AVDD×0.961 |
| 02H | AVDD×0.930 |
| 03H | AVDD×0.905 |
| 04H | AVDD×0.885 |
| 05H | AVDD×0.870 |
| 06H | AVDD×0.857 |
| 07H | AVDD×0.847 |
| 08H | AVDD×0.838 |
| 09H | AVDD×0.830 |
| 0AH | AVDD×0.823 |
| 0BH | AVDD×0.816 |
| 0CH | AVDD×0.811 |
| 0DH | AVDD×0.806 |
| 0EH | AVDD×0.801 |
| 0FH | AVDD×0.796 |
| 10H | AVDD×0.792 |
| 11H | AVDD×0.788 |
| 12H | AVDD×0.784 |
| 13H | AVDD×0.781 |
| 14H | AVDD×0.778 |
| 15H | AVDD×0.775 |
| 16H | AVDD×0.772 |
| 17H | AVDD×0.769 |
| 18H | AVDD×0.766 |
| 19H | AVDD×0.763 |
| 1AH | AVDD×0.761 |
| 1BH | AVDD×0.758 |
| 1CH | AVDD×0.756 |
| 1DH | AVDD×0.753 |
| 1EH | AVDD×0.751 |
| 1FH | AVDD×0.748 |

| Data | Positive |
|---|---|
| 20H | AVDD×0.747 |
| 21H | AVDD×0.745 |
| 22H | AVDD×0.743 |
| 23H | AVDD×0.741 |
| 24H | AVDD×0.739 |
| 25H | AVDD×0.737 |
| 26H | AVDD×0.735 |
| 27H | AVDD×0.732 |
| 28H | AVDD×0.731 |
| 29H | AVDD×0.729 |
| 2AH | AVDD×0.727 |
| 2BH | AVDD×0.725 |
| 2CH | AVDD×0.723 |
| 2DH | AVDD×0.721 |
| 2EH | AVDD×0.719 |
| 2FH | AVDD×0.717 |
| 30H | AVDD×0.715 |
| 31H | AVDD×0.713 |
| 32H | AVDD×0.711 |
| 33H | AVDD×0.710 |
| 34H | AVDD×0.709 |
| 35H | AVDD×0.707 |
| 36H | AVDD×0.706 |
| 37H | AVDD×0.704 |
| 38H | AVDD×0.702 |
| 39H | AVDD×0.700 |
| 3AH | AVDD×0.697 |
| 3BH | AVDD×0.694 |
| 3CH | AVDD×0.690 |
| 3DH | AVDD×0.681 |
| 3EH | AVDD×0.658 |
| 3FH | AVDD×0.592 |

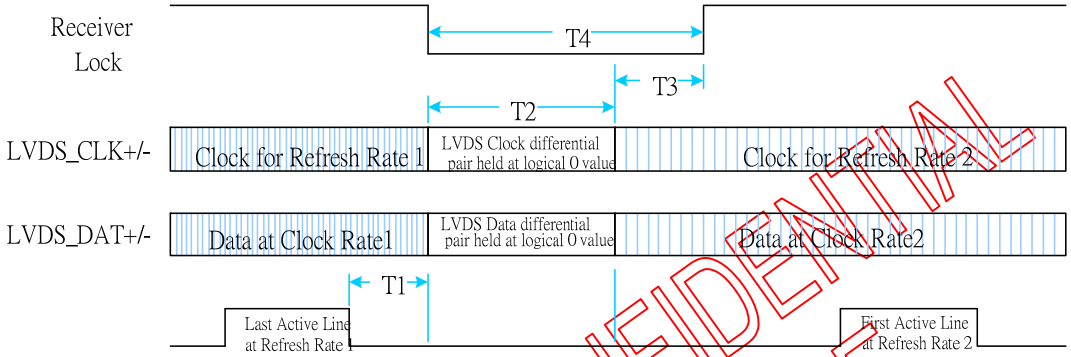
| Data | Negative |
|---|---|
| 00H | AVDD×0.010 |
| 01H | AVDD×0.034 |
| 02H | AVDD×0.068 |
| 03H | AVDD×0.096 |
| 04H | AVDD×0.119 |
| 05H | AVDD×0.136 |
| 06H | AVDD×0.151 |
| 07H | AVDD×0.162 |
| 08H | AVDD×0.172 |
| 09H | AVDD×0.182 |
| 0AH | AVDD×0.189 |
| 0BH | AVDD×0.197 |
| 0CH | AVDD×0.204 |
| 0DH | AVDD×0.210 |
| 0EH | AVDD×0.215 |
| 0FH | AVDD×0.221 |
| 10H | AVDD×0.227 |
| 11H | AVDD×0.231 |
| 12H | AVDD×0.236 |
| 13H | AVDD×0.240 |
| 14H | AVDD×0.245 |
| 15H | AVDD×0.248 |
| 16H | AVDD×0.253 |
| 17H | AVDD×0.256 |
| 18H | AVDD×0.260 |
| 19H | AVDD×0.263 |
| 1AH | AVDD×0.266 |
| 1BH | AVDD×0.270 |
| 1CH | AVDD×0.273 |
| 1DH | AVDD×0.277 |
| 1EH | AVDD×0.280 |
| 1FH | AVDD×0.284 |

| Data | Negative |
|---|---|
| 20H | AVDD×0.286 |
| 21H | AVDD×0.289 |
| 22H | AVDD×0.292 |
| 23H | AVDD×0.294 |
| 24H | AVDD×0.297 |
| 25H | AVDD×0.300 |
| 26H | AVDD×0.302 |
| 27H | AVDD×0.305 |
| 28H | AVDD×0.308 |
| 29H | AVDD×0.311 |
| 2AH | AVDD×0.314 |
| 2BH | AVDD×0.316 |
| 2CH | AVDD×0.318 |
| 2DH | AVDD×0.321 |
| 2EH | AVDD×0.325 |
| 2FH | AVDD×0.328 |
| 30H | AVDD×0.332 |
| 31H | AVDD×0.336 |
| 32H | AVDD×0.339 |
| 33H | AVDD×0.342 |
| 34H | AVDD×0.345 |
| 35H | AVDD×0.348 |
| 36H | AVDD×0.351 |
| 37H | AVDD×0.355 |
| 38H | AVDD×0.359 |
| 39H | AVDD×0.364 |
| 3AH | AVDD×0.369 |
| 3BH | AVDD×0.375 |
| 3CH | AVDD×0.382 |
| 3DH | AVDD×0.394 |
| 3EH | AVDD×0.421 |
| 3FH | AVDD×0.499 |

### 10.4. SDRRS Function

SDRRS(seamless display refresh rate switching)

When Showing the still picture. it is accept to refresh rate from 60Hz to low refresh rate (for example 40Hz).The purpose is mainly for power saving. INTEL defined a timing chart switch between different refresh rate. Following this timing chart, the switch between different refresh rates is seamless for end user.

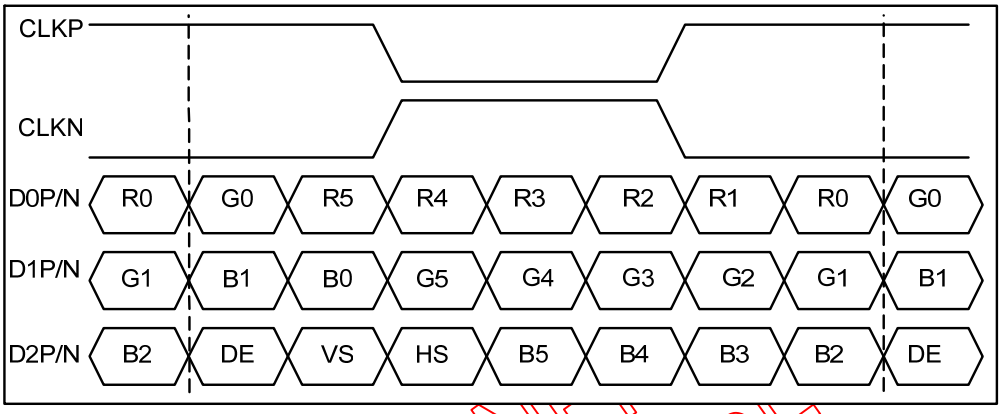



T1-Min delay from start of vertical blank to start of timing change:2 lines(HSYNC periods)
T2-Max delay for clock to transition to new frequency:100us
T3-Max receiver lock delay from stable clock: Display specific
T4-Max period during which panel maintains display(T2+T3): Display specific

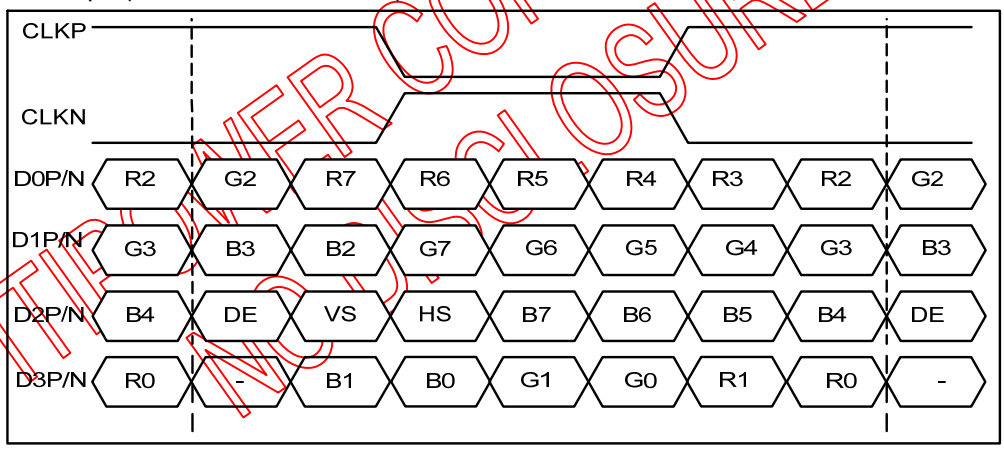
## 11. DATA INPUT FORMAT

### 11.1. Data Input Format for LVDS

- 6-bit LVDS input(LVBIT="L",LVMT=Don't Care)

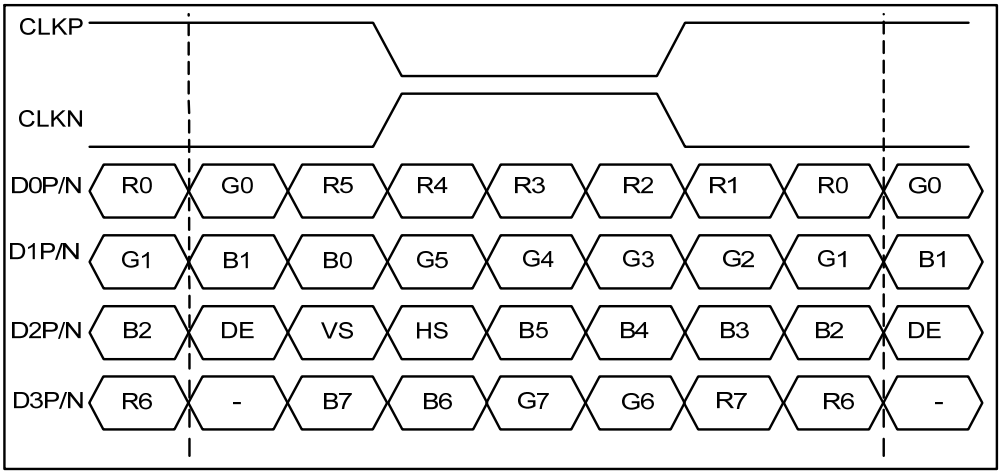



- 8-bit LVDS input(LVBIT="H",LVFMT="H")-JEIDA



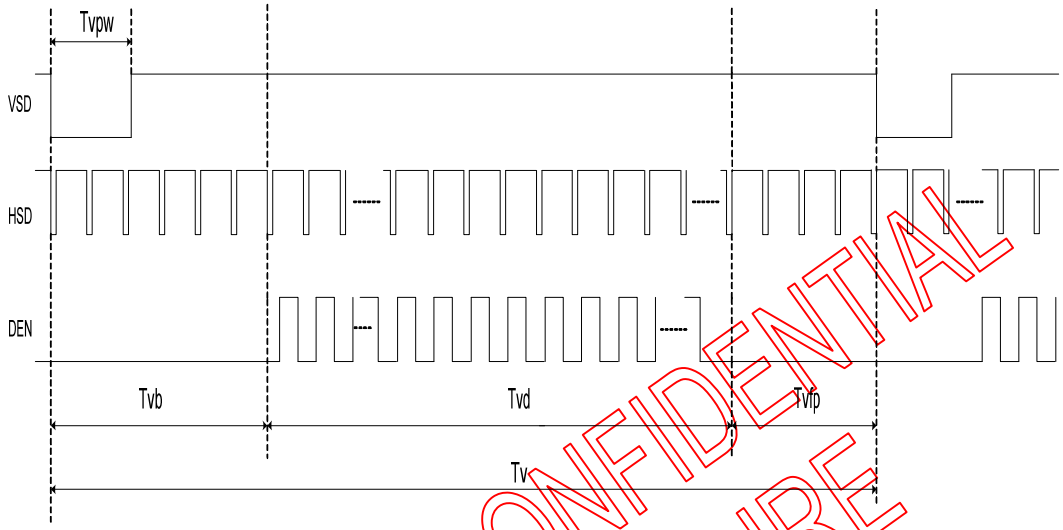



- 8-bit LVDS input(LVBIT="H",LVFMT="L")-VESA

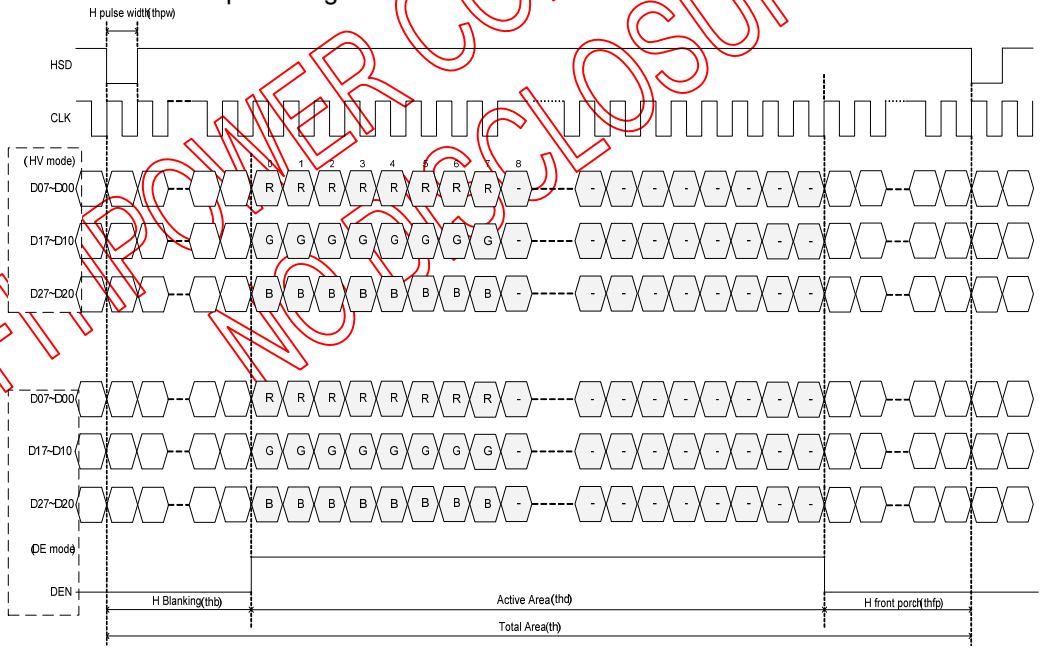


### 11.1.1. Equivalent Data Input Format for LVDS

- Equivalent vertical input timing format




- Equivalent horizontal input timing format



### 11.2. Input Timing Table

**For 1024RGB x 768 panel**

DE mode

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DCLK frequency @Frame rate=60hz | fclk | 52 | 65 | 71 | Mhz |
| Horizontal display area | thd | | 1024 | | DCLK |
| HSYNC period time | th | 1114 | 1344 | 1400 | DCLK |
| HSYNC blanking | thb+thfp | 90 | 320 | 376 | DCLK |
| Vertical display area | Tvd | | 768 | | H |
| VSYNC period time | Tv | 778 | 806 | 845 | H |
| VSYNC blanking | Tvb+Tvfp | 10 | 38 | 77 | H |

HV mode

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| Horizontal display area | | thd | 1024 | | | DCLK |
| DCLK frequency@ Frame rate=60hz | | fclk | Min. | Typ. | Max. | |
| | | | 57 | 65 | 70.5 | Mhz |
| 1 Horizontal Line | | th | 1200 | 1344 | 1400 | DCLK |
| HSYNC pulse width | Min. | thpw | 1 | | | |
| | Typ. | | — | | | |
| | Max. | | 140 | | | |
| HSYNC blanking | | thb | 160 | 160 | 160 | |
| HSYNC front porch | | thfp | 16 | 160 | 216 | |

HV mode

Vertical input timing

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vertical display area | tvd | | 768 | | H |
| VSYNC period time | tv | 792 | 806 | 840 | H |
| VSYNC pulse width | tvpw | 1 | — | 20 | H |
| VSYNC back porch | tvb | 23 | 23 | 23 | H |
| VSYNC front porch | tvfp | 1 | 15 | 49 | H |

**For 1024RGB x 600 panel**

DE mode

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DCLK frequency @Frame rate=60hz | fclk | 40.8 | 51.2 | 70.3 | Mhz |
| Horizontal display area | thd | | 1024 | | DCLK |
| HSYNC period time | th | 1114 | 1344 | 1464 | DCLK |
| HSYNC blanking | thb+thfp | 90 | 320 | 376 | DCLK |
| Vertical display area | Tvd | | 600 | | H |
| VSYNC period time | Tv | 610 | 635 | 800 | H |
| VSYNC blanking | Tvb+Tvfp | 10 | 35 | 200 | H |

HV mode

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| Horizontal display area | | thd | | 1024 | | DCLK |
| DCLK frequency@ Frame rate=60hz | | fclk | Min. | Typ. | Max. | |
| | | | 44.9 | 51.2 | 70.3 | Mhz |
| 1 Horizontal Line | | th | 1200 | 1344 | 1464 | DCLK |
| HSYNC pulse width | Min. | thpw | 1 | | | |
| | Typ. | | — | | | |
| | Max. | | 140 | | | |
| HSYNC blanking | | thb | 160 | 160 | 160 | |
| HSYNC front porch | | thfp | 16 | 160 | 216 | |

HV mode

Vertical input timing

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vertical display area | tvd | | 600 | | H |
| VSYNC period time | tv | 624 | 635 | 800 | H |
| VSYNC pulse width | tvpw | 1 | — | 20 | H |
| VSYNC back porch | tvb | 23 | 23 | 23 | H |
| VSYNC front porch | tvfp | 1 | 12 | 177 | H |

**For 800RGB x 600 panel**

DE mode

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DCLK frequency @Frame rate=60hz | fclk | 32.6 | 39.6 | 62.4 | Mhz |
| Horizontal display area | thd | | 800 | | DCLK |
| HSYNC period time | th | 890 | 1000 | 1300 | DCLK |
| HSYNC blanking | thb+thfp | 90 | 200 | 500 | DCLK |
| Vertical display area | Tvd | | 600 | | H |
| VSYNC period time | Tv | 610 | 660 | 800 | H |
| VSYNC blanking | Tvb+Tvfp | 10 | 60 | 200 | H |

HV mode

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| Horizontal display area | | thd | | 800 | | DCLK |
| DCLK frequency@ Frame rate=60hz | | fclk | Min. | Typ. | Max. | |
| | | | 34.5 | 39.6 | 50.4 | Mhz |
| 1 Horizontal Line | | th | 900 | 1000 | 1200 | DCLK |
| HSYNC pulse width | Min. | thpw | 1 | | | |
| | Typ. | | – | | | |
| | Max. | | 40 | | | |
| HSYNC blanking | | thb | 88 | 88 | 88 | |
| HSYNC front porch | | thfp | 12 | 112 | 312 | |

HV mode

Vertical input timing

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vertical display area | tvd | | 600 | | H |
| VSYNC period time | tv | 640 | 660 | 700 | H |
| VSYNC pulse width | tvpw | 1 | – | 20 | H |
| VSYNC back porch | tvb | 39 | 39 | 39 | H |
| VSYNC front porch | tvfp | 1 | 21 | 61 | H |

**For 800RGB x 480 panel**

DE mode

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DCLK frequency @Frame rate=60hz | fclk | 26.2 | 29.2 | 54.6 | Mhz |
| Horizontal display area | thd | | 800 | | DCLK |
| HSYNC period time | th | 890 | 928 | 1300 | DCLK |
| HSYNC blanking | thb+thfp | 90 | 128 | 500 | DCLK |
| Vertical display area | Tvd | | 480 | | H |
| VSYNC period time | Tv | 490 | 525 | 700 | H |
| VSYNC blanking | Tvb+Tvfp | 10 | 45 | 220 | H |

HV mode

Horizontal input timing

| Parameter | | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| Horizontal display area | | thd | | 800 | | DCLK |
| DCLK frequency@ Frame rate=60hz | | fclk | Min. | Typ. | Max. | |
| | | | 27.7 | 29.2 | 39.6 | Mhz |
| 1 Horizontal Line | | th | 900 | 928 | 1100 | DCLK |
| HSYNC pulse width | Min. | thpw | 1 | | | |
| | Typ. | | — | | | |
| | Max. | | 40 | | | |
| HSYNC blanking | | thb | 88 | 88 | 88 | |
| HSYNC front porch | | thfp | 12 | 40 | 212 | |

HV mode

Vertical input timing

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Vertical display area | tvd | | 480 | | H |
| VSYNC period time | tv | 513 | 525 | 600 | H |
| VSYNC pulse width | tvpw | 1 | — | 3 | H |
| VSYNC back porch | tvb | 32 | 32 | 32 | H |
| VSYNC front porch | tvfp | 1 | 13 | 88 | H |

## 12. ABSOLUTE MAXIMUM RATING

VOLTAGE (TA = 25°C, GND = AGND = GND_IF = 0V)

| | Min. | Max. | Unit |
|---|---|---|---|
| Digital Supply Voltage, VDD | -0.3 | +2.0 | V |
| Analog Supply Voltage, AVDD, V1~V14 | -0.5 | +15.0 | V |

TEMPERATURE

| | Min. | Max. | Unit |
|---|---|---|---|
| Operating temperature | -20 | +85 | °C |
| Storage temperature | -55 | +125 | °C |

## 13. RECOMMENDED OPERATING RANGE

Recommended Operating Range (TA = -20 to 85°C, GND = AGND = GND_IF = 0V )

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Digital supply voltage | VDD | 1.71 | 1.8 | 1.89 | V |
| MIPI/LVDS supply voltage | VDD_IF | 1.71 | 1.8 | 1.89 | V |
| Analog supply voltage | AVDD | 8 | - | 13.5 | V |

## 14. DC ELECTRICAL CHARACTERISTICS

### 14.1. Basic DC Characteristic

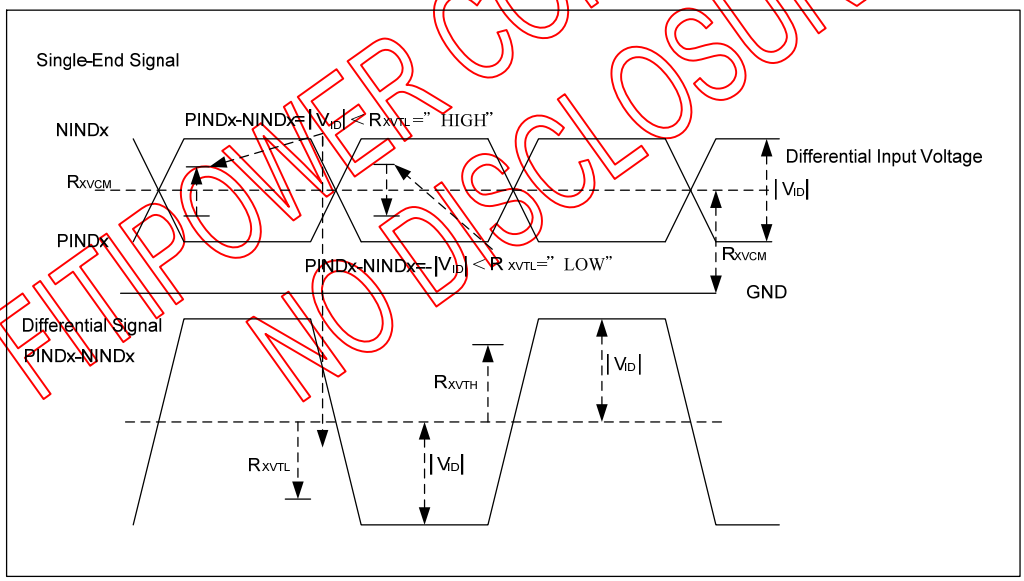
(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Low level input voltage | Vil | For the digital circuit | 0 | - | 0.3×VDD | V |
| High level input voltage | Vih | For the digital circuit | 0.7×VDD | - | VDD | V |
| Input leakage current | Ii | For the digital circuit | - | - | ±1 | μA |
| High level output voltage | Voh | Ioh= -400 μA | VDD - 0.4 | - | - | V |
| Low level output voltage | Vol | Iol= +400 μA | - | - | GND+0.4 | V |
| Pull low/high resistor | Ri | For the digital input pin @ VDD_IF=1.8V | 200K | 250K | 300K | ohm |
| Digital Operation current | Idd | Fclk=51.2MHz, VDD=VDD_IF=1.8V | - | TBD | - | mA |
| Digital Stand-by current | Ist1 | Clock and all functions are stopped | - | 10 | 50 | μA |
| Analog Operating Current | Idda | No load, Fclk=51.2MHz, @AVDD=13.5V,V1=13.4V, V14=0.1V | - | 10 | 12 | mA |
| Analog Stand-by current | Ist2 | No load, clock and all functions are stopped | - | 10 | 50 | μA |
| Input level of V1 ~ V7 | Vref1 | Gamma correction voltage input | 0.4*AVDD | - | AVDD-0.1 | V |
| Input level of V8 ~ V14 | Vref2 | Gamma correction voltage input | 0.1 | - | 0.6*AVDD | V |
| Output Voltage deviation | Vod1 | Vo = AGND+0.1V ~ AGND+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V | - | ±20 | ±35 | mV |
| Output Voltage deviation | Vod2 | Vo = AGND+0.5V ~ AVDD-0.5V | - | ±15 | ±20 | mV |
| Output Voltage Offset between Chips | Voc | Vo = AGND+0.5V ~ AVDD-0.5V | - | - | ±20 | mV |
| Dynamic Range of Output | Vdr | SO1 ~ 1536 | 0.1 | - | AVDD-0.1 | V |
| Sinking Current of Outputs | IOLy | SO1 ~ 1536; Vo=0.1V v.s 1.0V , AVDD=13.5V | 80 | - | - | uA |
| Driving Current of Outputs | IOHy | SO1 ~ 1536; Vo=13.4V v.s 12.5V , AVDD=13.5V | 80 | - | - | uA |
| Resistance of Gamma Table | Rg | Rn: Internal gamma resistor | 0.7*Rn | 1.0*Rn | 1.3*Rn | ohm |

### 14.2. LVDS Interface DC Characteristic

LVDS DC Characteristic(TBD)
(VDD=VDD_IF=1.8V,AVDD=8 to 13.5V,GND=AGND=GND_IF=0V,TA=-20℃ to 85℃)

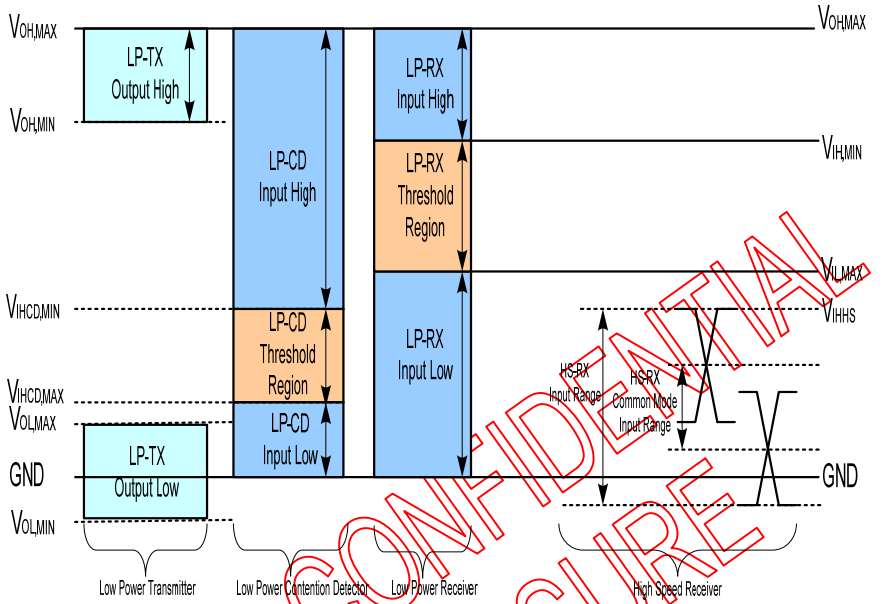
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential input high threshold voltage | RxVTH | - | 0.2 | - | V | RxVCM=1.2V |
| Differential input low threshold voltage | RxVTL | - | -0.2 | - | V | |
| Input voltage range(single-end) | RxVIN | 0 | - | 1.8 | V | |
| Differential input common mode voltage | RxVCM | $\|V_{ID}\|/2$ | 1.2 | 1.8 -$\|V_{ID}\|/2$ | V | |
| Differential input voltage | $\|V_{ID}\|$ | 0.2 | 0.4 | 0.6 | V | |
| Differential input leakage current | ILCLVDS | -10 | - | +10 | uA | |
| LVDS digital operating current | IDDLVDS | - | 20 | - | mA | Fclk=51.2Mhz, VDD=1.8V |
| LVDS digital standby current | ISTLVDS | - | 10 | - | uA | Clock & all functions are stop |
| Differential input impedance | ZID | 70 | 100 | 130 | ohm | |

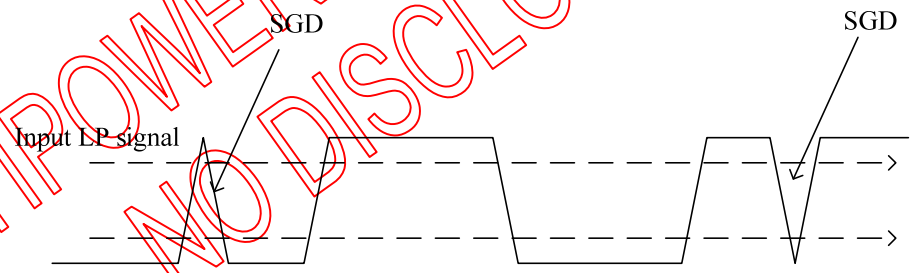


### 14.3. MIPI Interface DC Characteristic

(VDD=VDD_IF=1.8V,AVDD=8 to 13.5V,GND=AGND=GND_IF=0V,TA=-20℃ to 85℃)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| MIPI Characteristics for High Speed Receiver | | | | | |
| Single-ended input low voltage (DSI-CLKP/N,DSI-DnP/N) | $V_{ILHS}$ | -40 | - | - | mV |
| Single-ended input high voltage (DSI-CLKP/N,DSI-DnP/N) | $V_{IHHS}$ | - | - | 460 | mV |
| Input Common-mode voltage (DSI-CLKP/N,DSI-DnP/N) | $V_{CDRXDC}$ | 70 | - | 330 | mV |
| Differential input impedance | $Z_{ID}$ | | 100 | | ohm |
| HS transmit differential voltage(VOD=VDP-VDN) | $\|V_{OD}\|$ | 140 | 200 | 250 | mV |
| Low-level differential input voltage threshold | $V_{THLCLK}$ $V_{THLDATA}$ | -70 | - | - | mV |
| High-level differential input voltage threshold | $V_{THHCLK}$ $V_{THHDATA}$ | - | - | - | mV |
| Single-ended threshold voltage for termination | $V_{TERN\_EN}$ | - | - | 450 | mV |
| Termination capacitor | $C_{TERM}$ | | - | 14 | pf |
| Input voltage common mode variation(<=450Mhz) | $V_{CMRCLK}$ $V_{CMRDATAL}$ | -50 | - | 50 | mV |
| Input voltage common mode variation(>=450Mhz) | $V_{CMRCLKM}$ $V_{CMRDATAM}$ | | - | 100 | mV |
| MIPI Characteristics for Low Power Mode | | | | | |
| Pad signal voltage range | $V_I$ | -50 | - | 1350 | mV |
| Ground shift | $V_{GNDSH}$ | -50 | - | 50 | mV |
| Logic 0 input threshold | $V_{IL}$ | 0 | - | 550 | mV |
| Logic 1 input threshold | $V_{IH}$ | 880 | - | 1350 | mV |
| Logic 0 input voltage LPRX(CLK,ULP mode) | $V_{ILLPRXULP}$ | 0 | - | 300 | mV |
| Input hysteresis | $V_{HYST}$ | 25 | - | - | mV |
| Output low level | $V_{OL}$ | -50 | - | 50 | mV |
| Output high level | $V_{OH}$ | 1.1 | 1.2 | 1.3 | V |
| Output impedance of Low Power Transmitter | $Z_{OLP}$ | 90 | 100 | 110 | ohm |
| Logic 0 contention threshold | $V_{ILCD,MAX}$ | - | - | 200 | mV |
| Logic 0 contention threshold | $V_{IHCD,MIN}$ | 450 | - | 1350 | mV |
| Logic high level input current | $I_{IH}$ | - | - | 10 | uA |
| Logic low level input current | $I_{IL}$ | -10 | - | - | uA |
| Input pulse rejection (DSI-CLKP/N,DSI-DnP/N) | SGD | - | - | 300 | Vps |






### 14.4. Power Block DC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V,TA=-20 to +85℃)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Base drive current for PWM | IDRV | - | - | 60 | mA | DRVA =0.7V |
| DRV output voltage for PWM | VDRV | 0 | - | VDD | V | |
| Feedback voltage for PWM | VFB | 1.1 | 1.2 | 1.3 | V | |
| Duty cycle maximum | Dmax | - | - | 85 | % | |
| VCOM buffer input voltage | VCOMI | 1 | - | AVDD | V | |
| VCOM buffer output voltage | VCOMO | VCOMI-0.2 | VCOMI | VCOMI+0.2 | V | |
| VCOM buffer output current | IVCOM | - | - | 10 | mA | VCOMO=5V vs 4.9V |

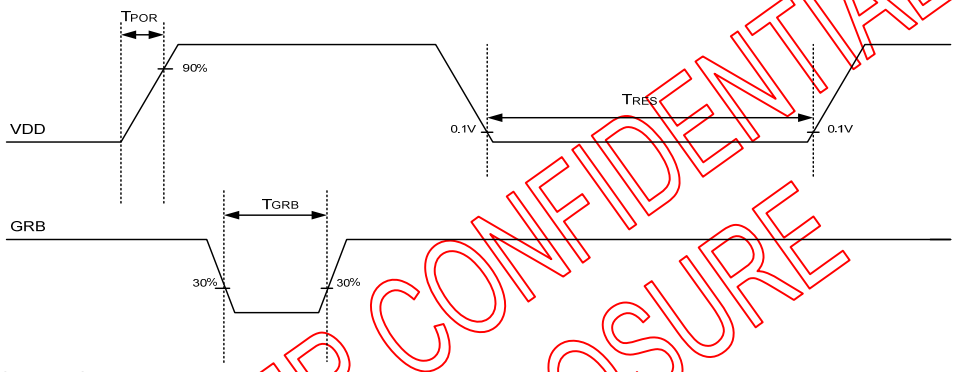
## 15. AC ELECTRICAL CHARACTERISTIC

### 15.1. Basic AC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V,TA=-20 to +85℃)

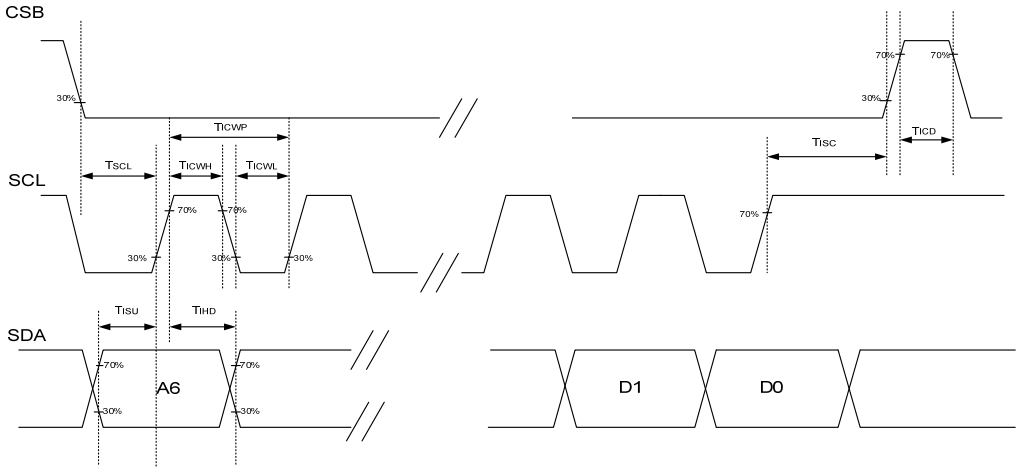
VDD/GRB AC characteristic

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| VDD power slew rate | $T_{POR}$ | - | - | 20 | ms | From 0 to 90% VDD |
| GRB active pulse width | $T_{GRB}$ | 1 | - | - | ms | VDD=VDD_IF=1.8V |
| VDD resettle time | $T_{RES}$ | 1 | - | - | s | |



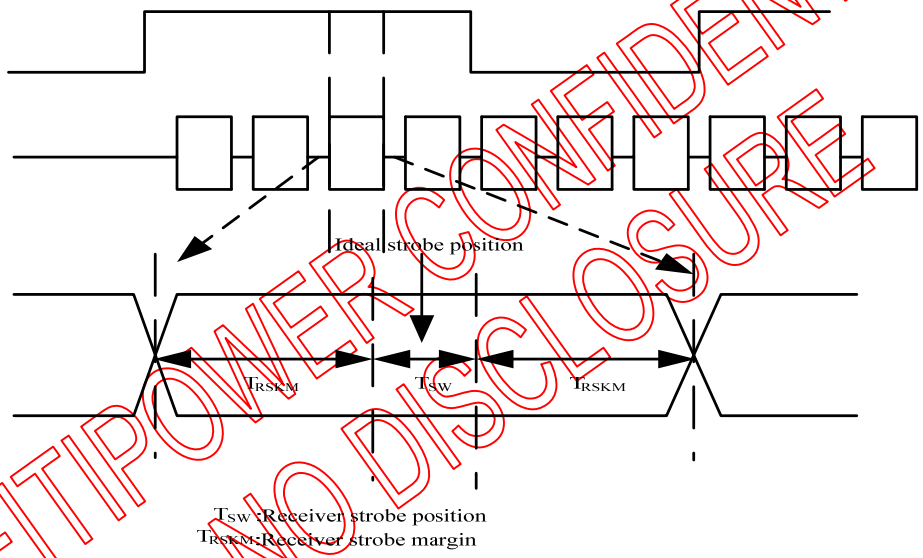

3-wire interface AC characteristic:

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CSB falling to SCL rising time | $T_{SCL}$ | 200 | - | - | ns |
| SCL pulse high period | $T_{ICWH}$ | 100 | - | - | ns |
| SCL pulse low period | $T_{ICWL}$ | 100 | - | - | ns |
| SCL pulse width | $T_{ICWP}$ | 250 | - | - | ns |
| SDA data input setup time | $T_{ISU}$ | 100 | - | - | ns |
| SDA data input hold time | $T_{IHD}$ | 100 | - | - | ns |
| SCL to CSB rising time | $T_{ISC}$ | 250 | - | - | ns |
| CSB rising to failing time | $T_{ICD}$ | 1 | - | - | us |



### 15.2. LVDS AC Characteristic

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Clock Frequency | $R_{xFCLK}$ | | 20 | - | 71 | MHz |
| Input data skew margin | $T_{RSKM}$ | $\|V_{ID}\|$=400mV<br>$R_{xVCM}$=1.2V<br>$R_{xFCLK}$=71MHz | 500 | | | ps |
| Clock High Time | $T_{LVCH}$ | | | 4/(7* $R_{xFCLK}$) | | ns<br>ns |
| Clock Low Time | $T_{LVCL}$ | | | 3/(7* $R_{xFCLK}$) | | ns |
| PLL wake-up-time | $T_{enPLL}$ | | | | 150 | us |

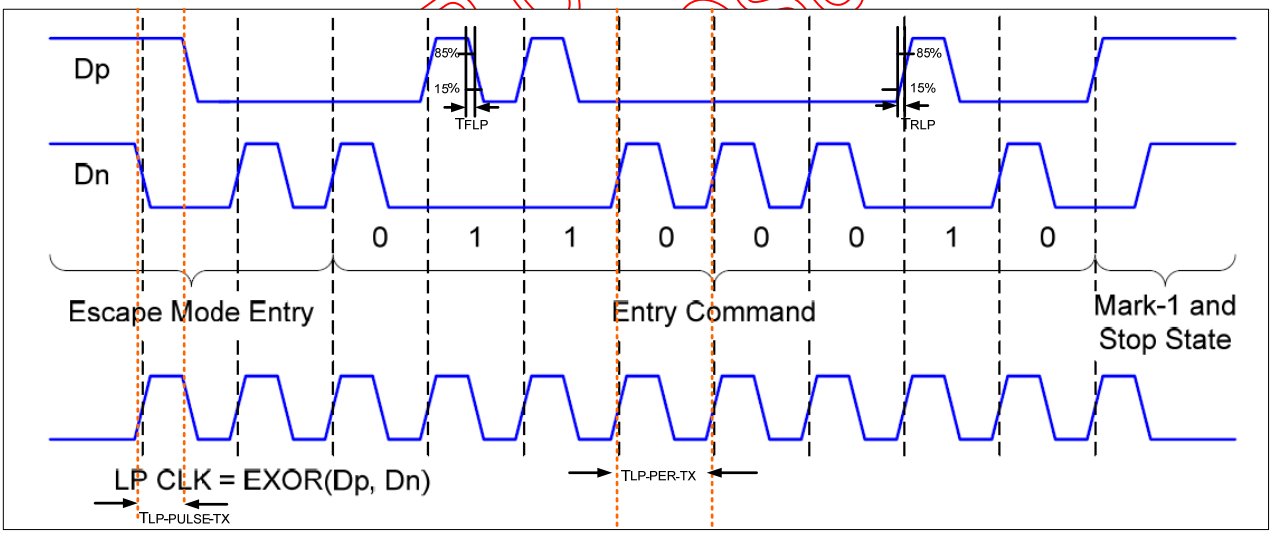


### 15.3. MIPI AC Characteristic

#### 15.3.1. LP Transmitter AC Specification

| Parameter | | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| 15%~85% rising time and falling time | | $T_{RLP}$ /$T_{FLP}$ | - | - | 25 | ns | - |
| 30%~85% rising time and falling time | | $T_{REOT}$ | - | - | 35 | ns | - |
| Pulse width of LP exclusive-OR clock | First LP EXOR clock pulse after STOP state or Last pulse before stop state | $T_{LP-PULSE-TX}$ | 40 | - | - | ns | - |
| | All other pulses | | 20 | - | - | ns | - |
| Period of the LP EXOR clock | | $T_{LP-PER-TX}$ | 90 | - | - | mV/ns | - |
| Slew Rate @$C_{LOAD}$ =0pF | | $\delta V / \delta t_{SR}$ | 30 | - | 500 | mV/ns | - |
| Slew Rate @$C_{LOAD}$ =5pF | | | 30 | - | 200 | mV/ns | - |
| Slew Rate @$C_{LOAD}$ =20pF | | | 30 | - | 150 | mV/ns | - |
| Slew Rate @$C_{LOAD}$ =70pF | | | 30 | - | 100 | mV/ns | - |
| Load Capacitance | | $T_{RLP}$ | - | - | 70 | pF | - |

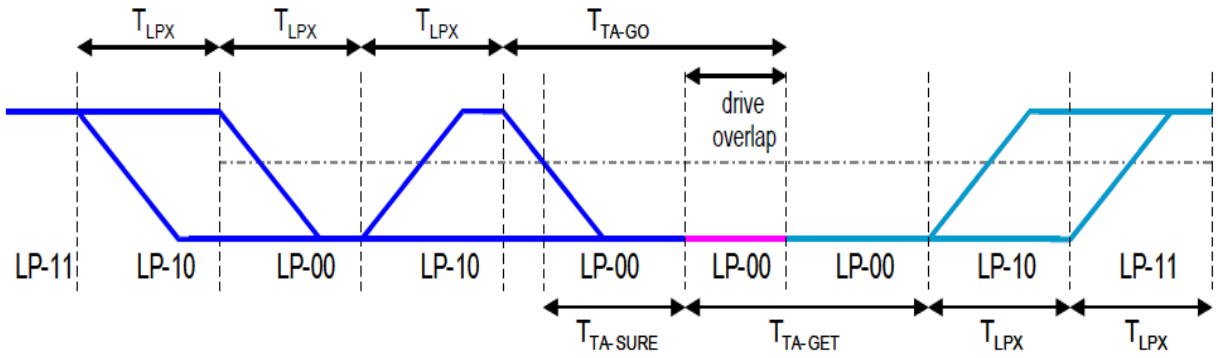




### 15.3.2. Turnaround Procedure

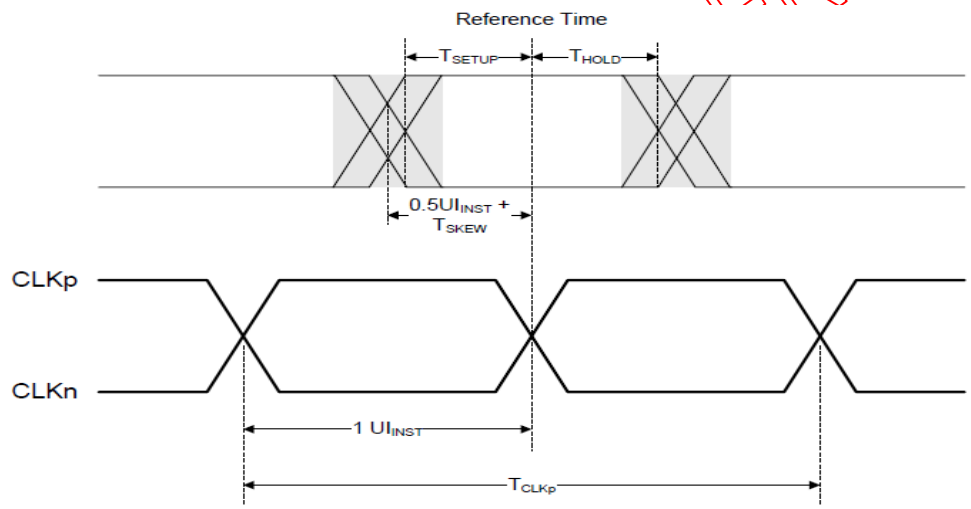
Turnaround Procedure Operation Timing Parameters

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Length of any Low-Power state period: Master side | $T_{LPX}$ | 50 | - | 75 | ns |
| Length of any Low-Power state period: Slave side | $T_{LPX}$ | 50 | 55.56 | 58.34 | ns |
| Ratio of $T_{LPX}$(Master)/ $T_{LPX}$ (Slave) between Master and Slave side | Ratio $T_{LPX}$ | 2/3 | - | 3/2 | |
| Time-out before new TX side start driving | $T_{TA-Sure}$ | $T_{LPX}$ | - | $2T_{LPX}$ | ns |
| Time to drive LP-00 by new TX | $T_{TA-GET}$ | - | $5T_{LPX}$ | - | ns |
| Time to drive LP-00 after Turnaround Request | $T_{TA-GO}$ | - | $4T_{LPX}$ | - | ns |



**15.3.3.** High speed transmission

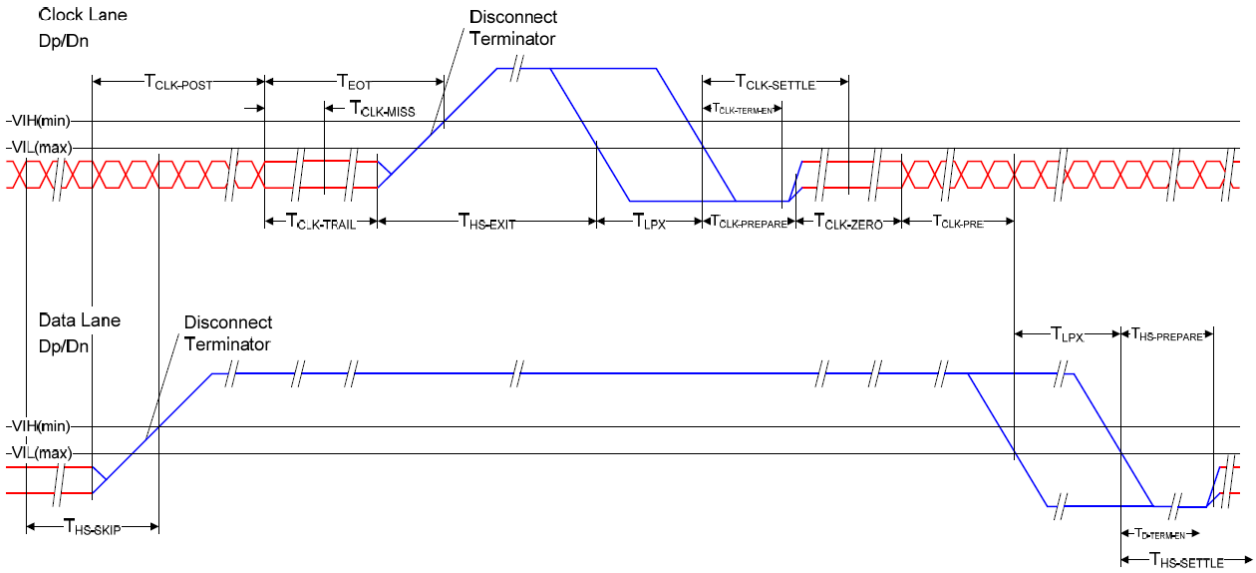
| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | 2 | - | 12.5 | ns |
| Data to Clock Skew(measured at transmitter) | $T_{SKEW(TX)}$ | -0.15 | - | 0.15 | $UI_{INST}$ |
| Data to Clock Setup time(measured at receiver) | $T_{SETUP(RX)}$ | 0.15 | - | - | $UI_{INST}$ |
| Data to Clock Hold time(measured at receiver) | $T_{HOLD(RX)}$ | 0.15 | - | - | $UI_{INST}$ |
| 20%~80% rise time and fall time | $T_R$, $T_F$ | 150 | - | - | ps |
| | | - | - | 0.3 | $UI_{INST}$ |



**15.3.4.** High Speed Clock Transmission

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | $T_{CLK-POST}$ | 60+52UI | - | - | ns |
| Detection time that the clock has stopped toggling | $T_{CLK-MISS}$ | - | - | 60 | ns |
| Time to drive LP-00 to prepare for HS clock transmission | $T_{CLK-PREPARE}$ | 38 | - | 95 | ns |
| Minimum lead HS-0 drive period before starting clock | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | 300 | - | - | ns |
| Time to enable Clock Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$ | $T_{HS-TERM-EN}$ | - | - | 38 | ns |
| Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode | $T_{CLK-PRE}$ | 8 | - | - | UI |
| Time to drive HS differential state after last payload clock bit of a HS transmission burst | $T_{CLK-TRAIL}$ | 60 | - | - | ns |

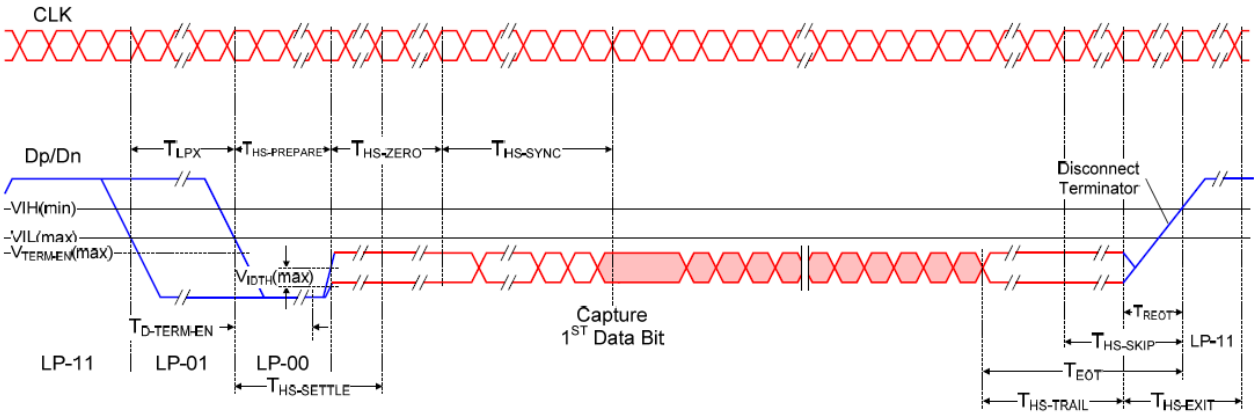




**15.3.5.** High Speed Data Transmission in Bursts

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Time to drive LP-00 to prepare for HS transmission | $T_{HS-PREPARE}$ | 40+4UI | - | 85+6UI | ns |
| Time from start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ period to start of LP-11 state | $T_{EOT}$ | - | - | 105+12UI | ns |
| Time to enable Data Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$ | $T_{HS-TERM-EN}$ | - | - | 35+4UI | ns |
| Time to drive flipped differential state after last payload data bit of a HS transmission burst | $T_{HS-TRAIL}$ | 60+4UI | - | - | ns |
| Time-out at RX to ignore transition period of EoT | $T_{HS-SKIP}$ | 40 | - | 55+4UI | ns |
| Time to drive LP-11 after HS burst | $T_{HS-EXIT}$ | 100 | - | - | ns |
| Length of any Low-Power state period | $T_{LPX}$ | 50 | - | - | ns |
| Sync sequence period | $T_{HS-SYNC}$ | - | 8UI | - | ns |
| Minimum lead HS-0 drive period before the Sync sequence | $T_{HS-ZERO}$ | 105+6UI | - | - | ns |

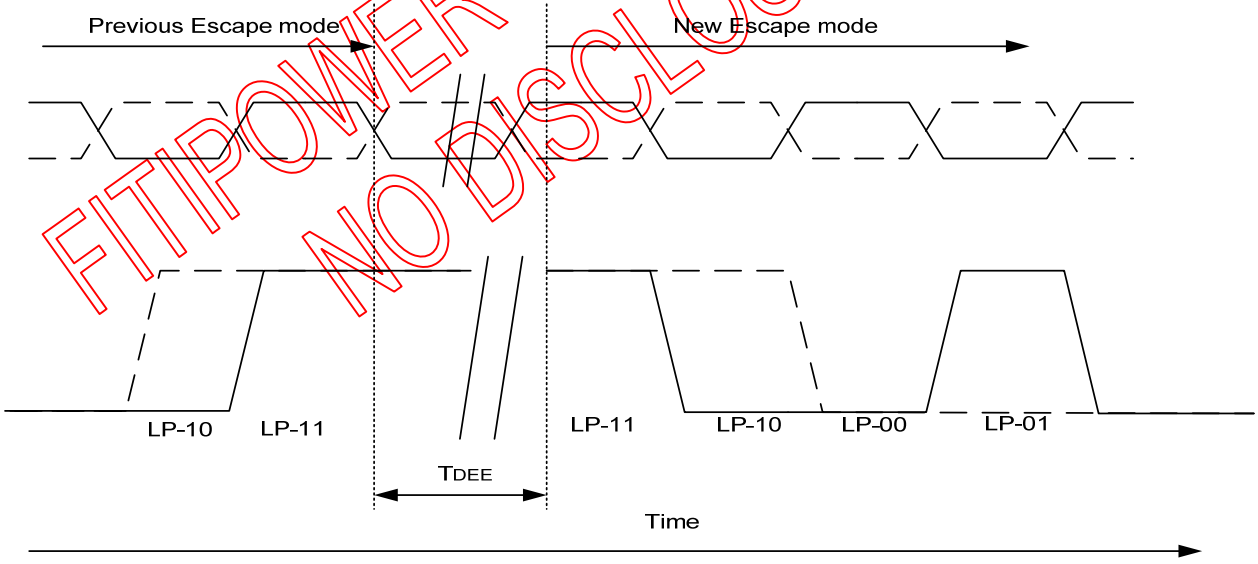




**15.3.6.** LP11 timing request between data transformation

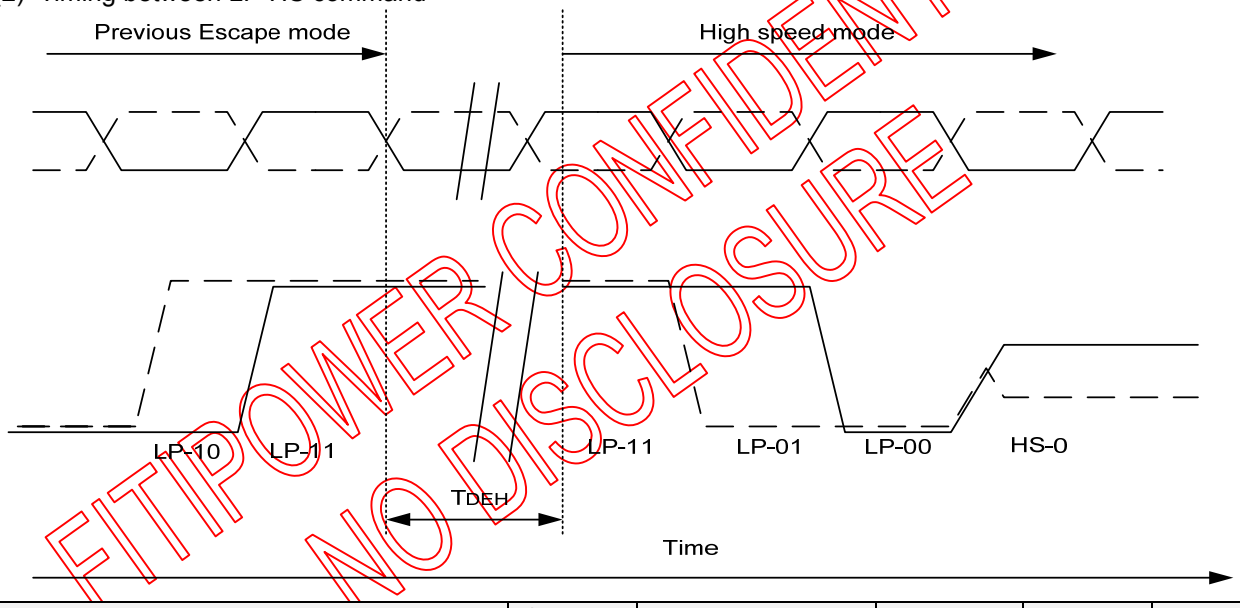
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP–LP, LP–HS, HS–LP, HS–HS, BTA–BTA, LP–BTA, BTA–LP, HS–BTA, and BTA–HS.This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP-LP command




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the new Escape Mode Entry | TDEE | 150 | - | - | ns |

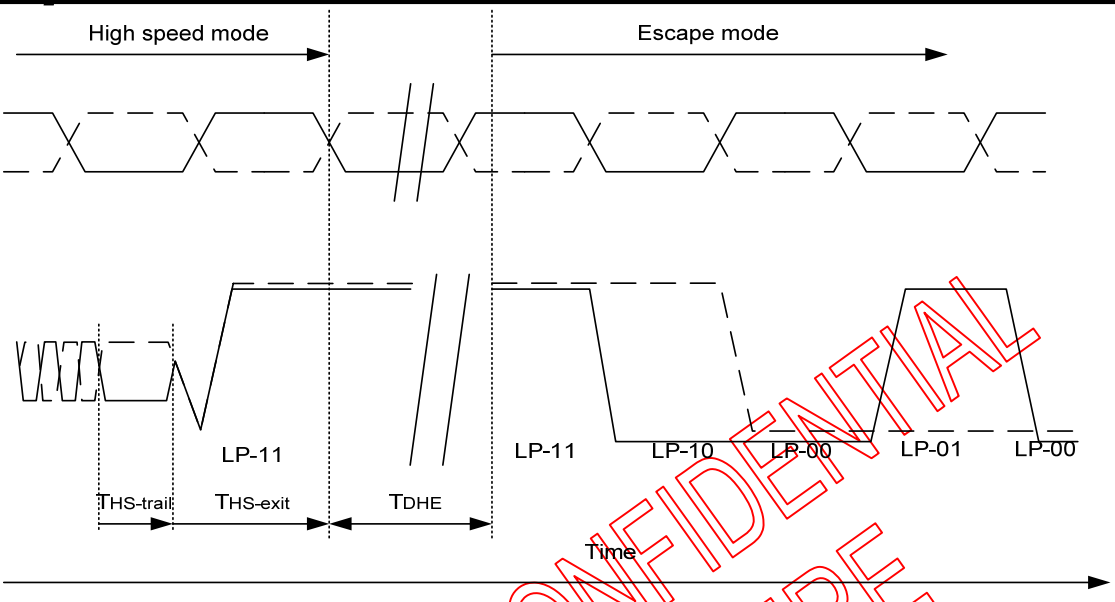
(2) Timing between LP-HS command






| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the Entering High Speed Mode | TDEH | Max(150,32UI) | - | - | ns |

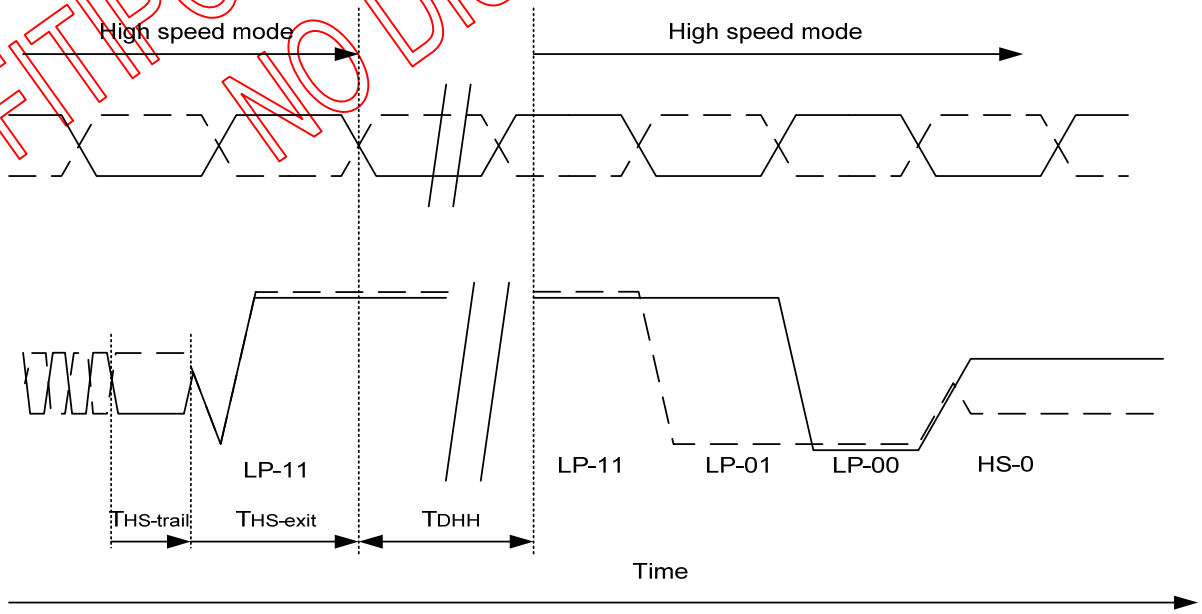
(3) Timing between HS-LP command




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the Escape Mode Entry | TDHE | Max(150,32UI) | - | - | ns |

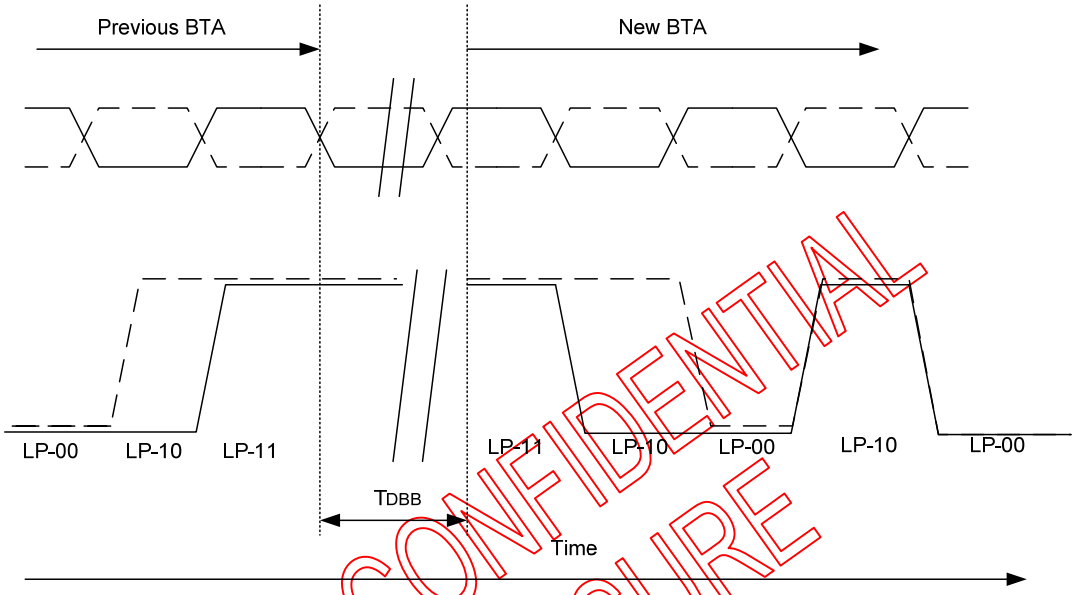


(4) Timing between HS-HS command



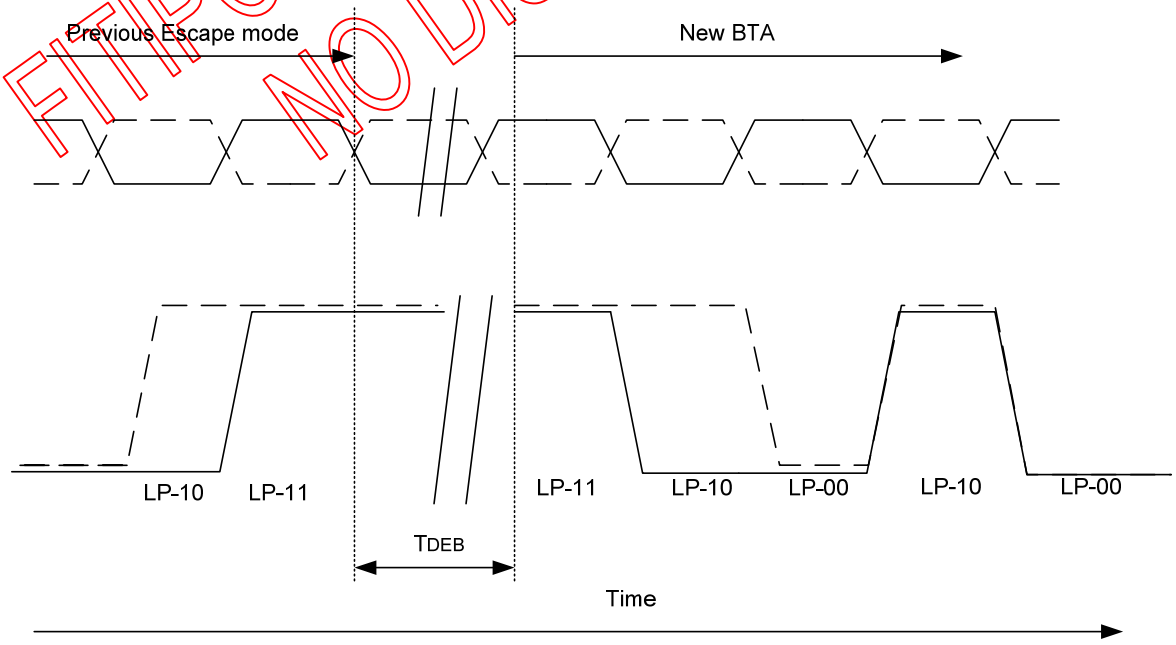

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the Entering High Speed Mode | TDHH | Max(150,32UI) | - | - | ns |

(5) Timing between BTA-BTA command



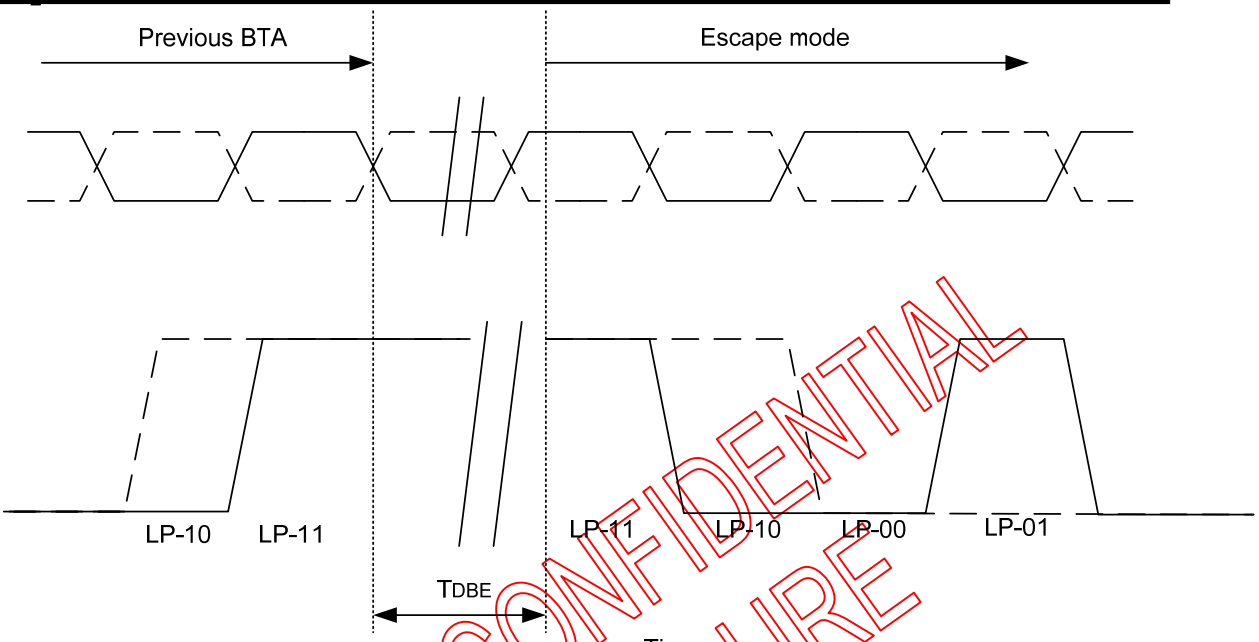

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the new BTA | $T_{DBB}$ | 150 | - | - | ns |

(6) Timing between LP-BTA command



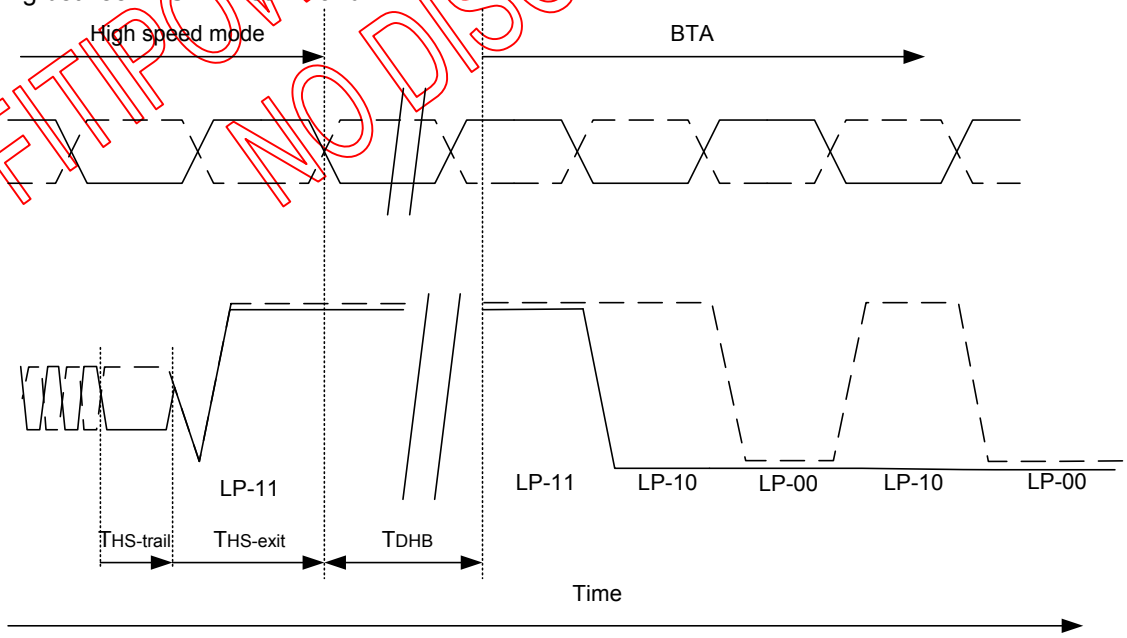

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the new BTA | $T_{DEB}$ | 150 | - | - | ns |

(7) Timing between BTA-LP command



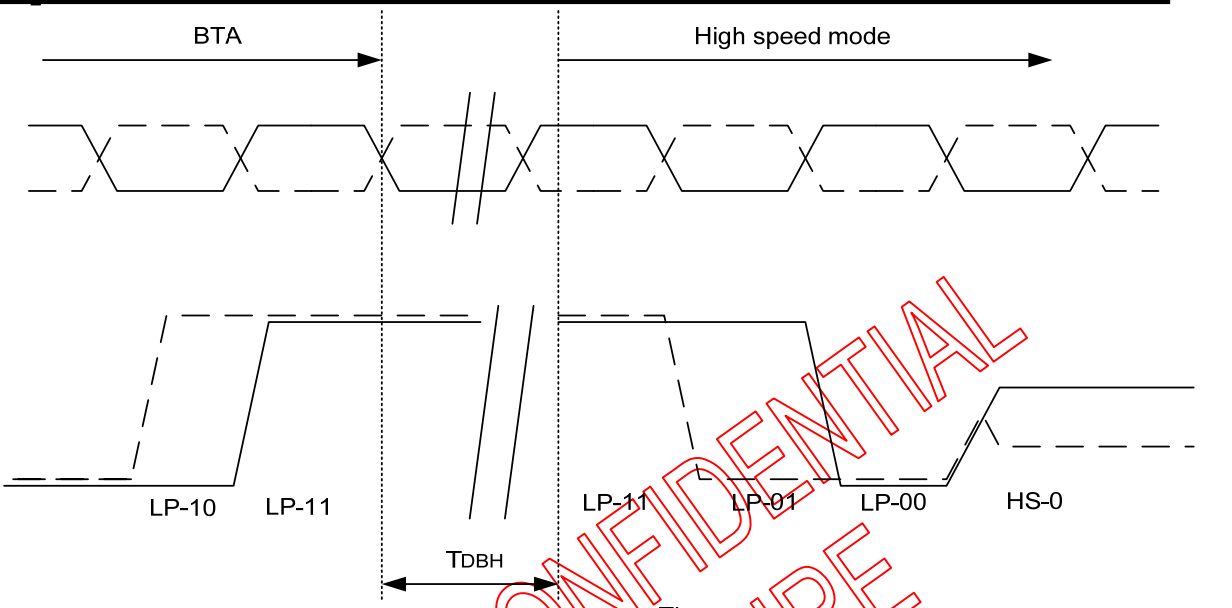

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the Escape Mode Entry | $T_{DBE}$ | 150 | - | - | ns |

(8) Timing between HS-BTA command




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the BTA | $T_{DHB}$ | Max(150,32UI) | - | - | ns |

(9) Timing between BTA-HP command




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LP-11 delay to start of the Entering High Speed Mode | TDBH | Max(150,32UI) | - | - | ns |



### 15.4. Output Timing Table

- Dual gate mode

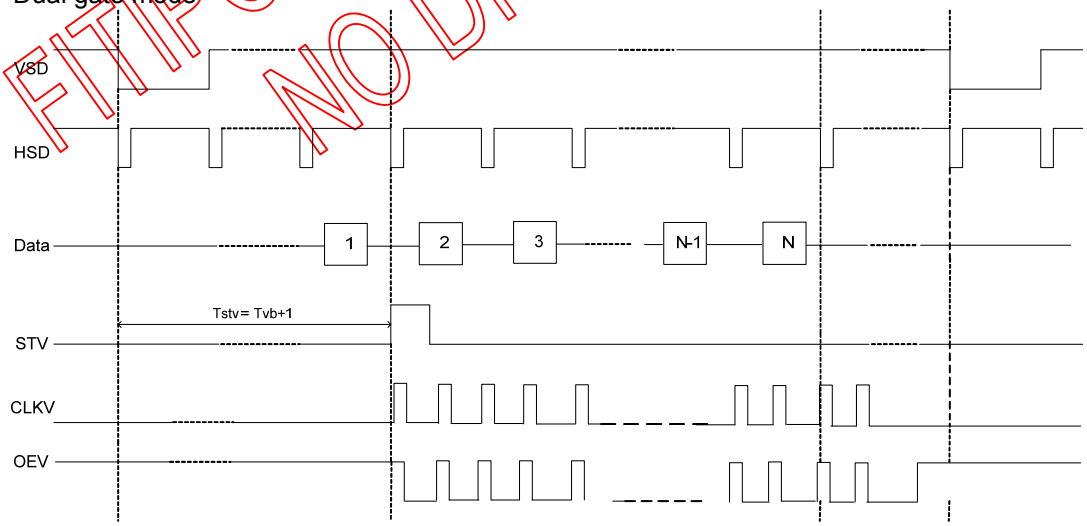



Fig. 11. Vertical output timing

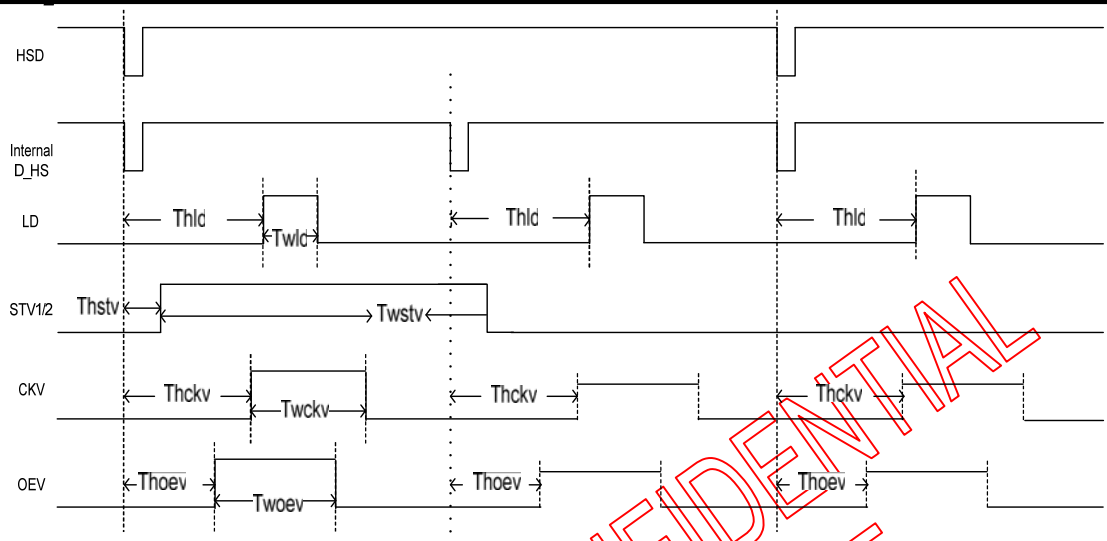
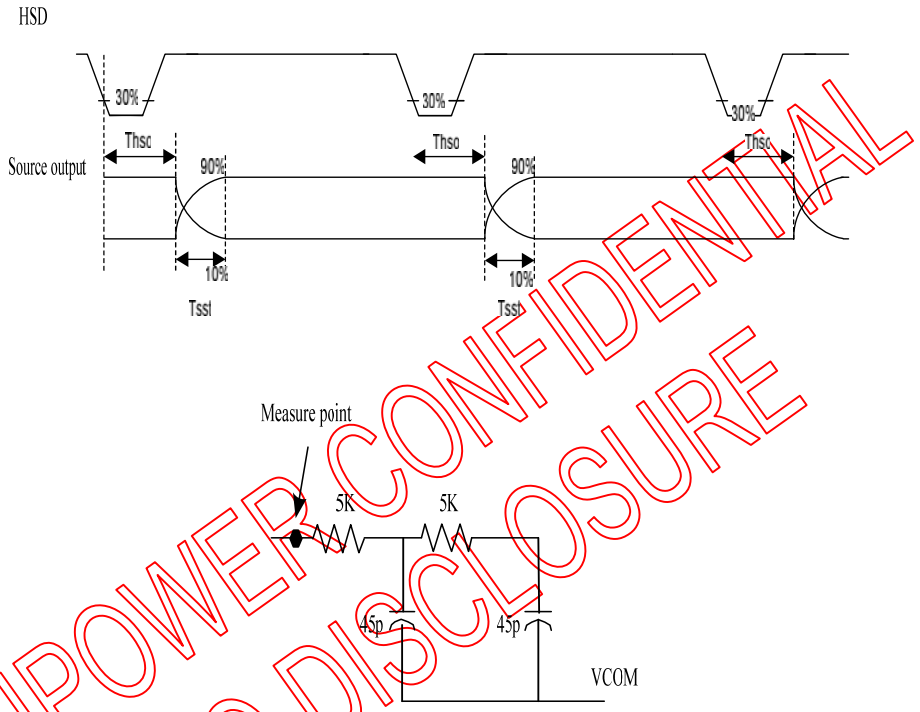


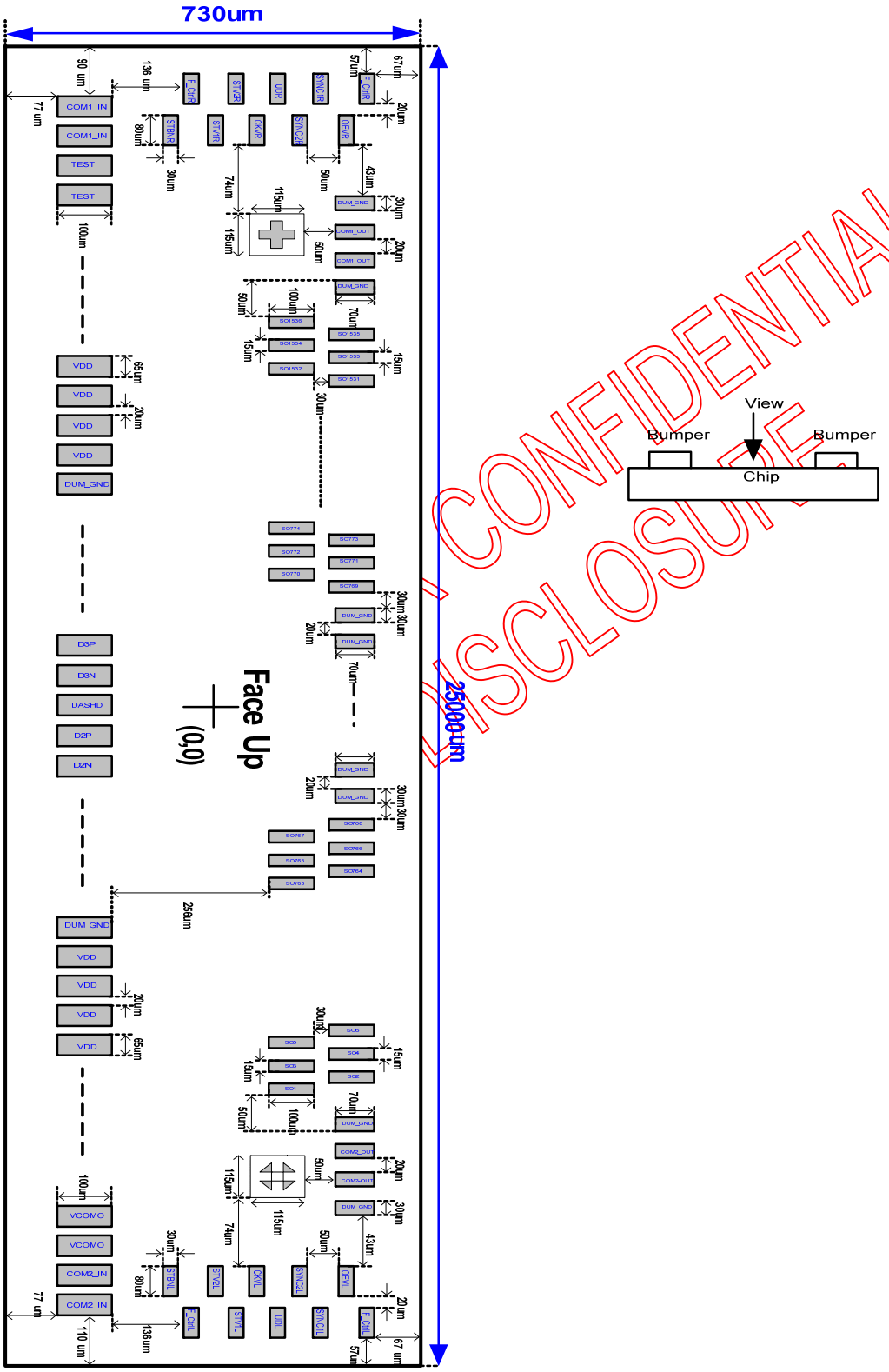

Fig. 11. Gate output timing

Analog output AC characteristic

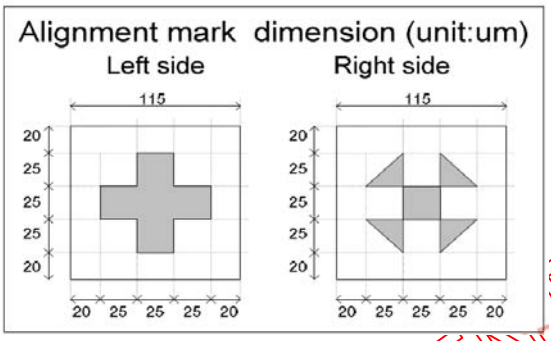
| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Source Driver output stable time | Tsst | - | 3 | - | μs |



## 16. CHIP OUTLINE DIMENSIONS



### 16.1. Alignment Mark



## 17. PAD COORDINATE

| Pad | Text Name | CX | CY |
|---|---|---|---|
| 1 | COM1_IN | -12377.5 | -238 |
| 2 | COM1_IN | -12292.5 | -238 |
| 3 | TP1 | -12207.5 | -238 |
| 4 | TP2 | -12122.5 | -238 |
| 5 | TP3 | -12037.5 | -238 |
| 6 | TP4 | -11952.5 | -238 |
| 7 | SHIELDING | -11867.5 | -238 |
| 8 | AGND | -11782.5 | -238 |
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| 10 | AGND | -11612.5 | -238 |
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| 12 | SHIELDING | -11442.5 | -238 |
| 13 | AVDD | -11357.5 | -238 |
| 14 | AVDD | -11272.5 | -238 |
| 15 | AVDD | -11187.5 | -238 |
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| 17 | SHIELDING | -11017.5 | -238 |
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| 23 | VDD | -10507.5 | -238 |
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| 27 | SHIELDING | -10167.5 | -238 |
| 28 | TP5 | -10082.5 | -238 |
| 29 | TP6 | -9997.5 | -238 |
| 30 | TP7 | -9912.5 | -238 |
| 31 | TP8 | -9827.5 | -238 |
| 32 | TP9 | -9742.5 | -238 |
| 33 | TP10 | -9657.5 | -238 |
| 34 | TP11 | -9572.5 | -238 |
| 35 | TP12 | -9487.5 | -238 |
| 36 | TP13 | -9402.5 | -238 |
| 37 | TP14 | -9317.5 | -238 |
| 38 | SHIELDING | -9232.5 | -238 |
| 39 | DIMI | -9147.5 | -238 |
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| 41 | NBW | -8977.5 | -238 |
| 42 | NBW | -8892.5 | -238 |
| 43 | PINCTL | -8807.5 | -238 |
| 44 | PINCTL | -8722.5 | -238 |
| 45 | SHIELDING | -8637.5 | -238 |
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| 48 | SHIELDING | -8382.5 | -238 |
| 49 | DITHER | -8297.5 | -238 |
| 50 | DITHER | -8212.5 | -238 |
| 51 | HFRC | -8127.5 | -238 |
| 52 | HFRC | -8042.5 | -238 |
| 53 | TP15 | -7957.5 | -238 |
| 54 | TP16 | -7872.5 | -238 |
| 55 | FRAME | -7787.5 | -238 |
| 56 | FRAME | -7702.5 | -238 |
| 57 | SEL[0] | -7617.5 | -238 |
| 58 | SEL[0] | -7532.5 | -238 |
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| 62 | CSB | -7192.5 | -238 |
| 63 | SHIELDING | -7107.5 | -238 |
| 64 | SDA | -7022.5 | -238 |
| 65 | SDA | -6937.5 | -238 |
| 66 | SHIELDING | -6852.5 | -238 |
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| 89 | SHIELDING | -4897.5 | -238 |
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| 91 | V1 | -4727.5 | -238 |
| 92 | V2 | -4642.5 | -238 |
| 93 | V2 | -4557.5 | -238 |
| 94 | V3 | -4472.5 | -238 |
| 95 | V3 | -4387.5 | -238 |
| 96 | V4 | -4302.5 | -238 |
| 97 | V4 | -4217.5 | -238 |
| 98 | V5 | -4132.5 | -238 |
| 99 | V5 | -4047.5 | -238 |
| 100 | V6 | -3962.5 | -238 |
| 101 | V6 | -3877.5 | -238 |
| 102 | V7 | -3792.5 | -238 |
| 103 | V7 | -3707.5 | -238 |
| 104 | GAMH | -3622.5 | -238 |
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| 106 | SHIELDING | -3452.5 | -238 |
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| 108 | LVFMT | -3282.5 | -238 |
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| 110 | LVBIT | -3112.5 | -238 |
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| 124 | CLKN | -1922.5 | -238 |
| 125 | DASHD | -1837.5 | -238 |
| 126 | D1P | -1752.5 | -238 |
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| 137 | DASHD | -817.5 | -238 |
| 138 | VDDLV | -732.5 | -238 |
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| 142 | VDDLV | -392.5 | -238 |
| 143 | VDDLV | -307.5 | -238 |
| 144 | TP18 | -222.5 | -238 |
| 145 | TP19 | -137.5 | -238 |
| 146 | DASHD | -52.5 | -238 |
| 147 | TP20 | 32.5 | -238 |
| 148 | TP21 | 117.5 | -238 |
| 149 | DASHD | 202.5 | -238 |
| 150 | TP22 | 287.5 | -238 |
| 151 | TP23 | 372.5 | -238 |
| 152 | DASHD | 457.5 | -238 |
| 153 | TP24 | 542.5 | -238 |
| 154 | TP25 | 627.5 | -238 |
| 155 | DASHD | 712.5 | -238 |
| 156 | TP26 | 797.5 | -238 |
| 157 | TP27 | 882.5 | -238 |
| 158 | TP28 | 967.5 | -238 |
| 159 | TP29 | 1052.5 | -238 |
| 160 | TP30 | 1137.5 | -238 |
| 161 | DASHD | 1222.5 | -238 |
| 162 | SHIELDING | 1307.5 | -238 |
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| 165 | V8 | 1562.5 | -238 |
| 166 | V8 | 1647.5 | -238 |
| 167 | V9 | 1732.5 | -238 |
| 168 | V9 | 1817.5 | -238 |
| 169 | V10 | 1902.5 | -238 |
| 170 | V10 | 1987.5 | -238 |
| 171 | V11 | 2072.5 | -238 |
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| 173 | V12 | 2242.5 | -238 |
| 174 | V12 | 2327.5 | -238 |
| 175 | V13 | 2412.5 | -238 |
| 176 | V13 | 2497.5 | -238 |
| 177 | V14 | 2582.5 | -238 |
| 178 | V14 | 2667.5 | -238 |
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| 182 | AGND | 3007.5 | -238 |

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| 184 | SHIELDING | 3177.5 | -238 |
| 185 | AVDD | 3262.5 | -238 |
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| 187 | AVDD | 3432.5 | -238 |
| 188 | AVDD | 3517.5 | -238 |
| 189 | SHIELDING | 3602.5 | -238 |
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| 199 | SHIELDING | 4452.5 | -238 |
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| 202 | MASL | 4707.5 | -238 |
| 203 | MASL | 4792.5 | -238 |
| 204 | MASLOC | 4877.5 | -238 |
| 205 | MASLOC | 4962.5 | -238 |
| 206 | CABC_EN[0] | 5047.5 | -238 |
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| 209 | CABC_EN[1] | 5302.5 | -238 |
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| 216 | BIST | 5897.5 | -238 |
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| 218 | RES[0] | 6067.5 | -238 |
| 219 | RES[0] | 6152.5 | -238 |
| 220 | RES[1] | 6237.5 | -238 |
| 221 | RES[1] | 6322.5 | -238 |
| 222 | TP_TEST | 6407.5 | -238 |
| 223 | TP_TEST | 6492.5 | -238 |
| 224 | STBYB | 6577.5 | -238 |
| 225 | STBYB | 6662.5 | -238 |

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| 244 | TP42 | 8277.5 | -238 |
| 245 | TP43 | 8362.5 | -238 |
| 246 | TP44 | 8447.5 | -238 |
| 247 | SHIELDING | 8532.5 | -238 |
| 248 | VDD | 8617.5 | -238 |
| 249 | VDD | 8702.5 | -238 |
| 250 | VDD | 8787.5 | -238 |
| 251 | VDD | 8872.5 | -238 |
| 252 | SHIELDING | 8957.5 | -238 |
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| 261 | AVDD | 9722.5 | -238 |
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| 266 | AGND | 10147.5 | -238 |
| 267 | SHIELDING | 10232.5 | -238 |
| 268 | TP45 | 10317.5 | -238 |
| 269 | VCOMI | 10402.5 | -238 |
| 270 | VCOMI | 10487.5 | -238 |
| 271 | PWR_EN | 10572.5 | -238 |
| 272 | PWR_EN | 10657.5 | -238 |
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| 274 | FBL | 10827.5 | -238 |
| 275 | FBH | 10912.5 | -238 |
| 276 | FBH | 10997.5 | -238 |
| 277 | FBA | 11082.5 | -238 |
| 278 | FBA | 11167.5 | -238 |
| 279 | AVDDG | 11252.5 | -238 |
| 280 | AVDDG | 11337.5 | -238 |
| 281 | DRVA | 11422.5 | -238 |
| 282 | DRVA | 11507.5 | -238 |
| 283 | DRVH | 11592.5 | -238 |
| 284 | DRVH | 11677.5 | -238 |
| 285 | DRVL | 11762.5 | -238 |

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| 305 | COM2_OUT | 12105 | 263 |
| 306 | SHIELDING | 12055 | 263 |
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| 309 | SO3 | 11982.5 | 118 |
| 310 | SO4 | 11967.5 | 248 |
| 311 | SO5 | 11952.5 | 118 |
| 312 | SO6 | 11937.5 | 248 |
| 313 | SO7 | 11922.5 | 118 |
| 314 | SO8 | 11907.5 | 248 |
| 315 | SO9 | 11892.5 | 118 |
| 316 | SO10 | 11877.5 | 248 |
| 317 | SO11 | 11862.5 | 118 |
| 318 | SO12 | 11847.5 | 248 |
| 319 | SO13 | 11832.5 | 118 |
| 320 | SO14 | 11817.5 | 248 |
| 321 | SO15 | 11802.5 | 118 |
| 322 | SO16 | 11787.5 | 248 |
| 323 | SO17 | 11772.5 | 118 |
| 324 | SO18 | 11757.5 | 248 |
| 325 | SO19 | 11742.5 | 118 |
| 326 | SO20 | 11727.5 | 248 |
| 327 | SO21 | 11712.5 | 118 |
| 328 | SO22 | 11697.5 | 248 |
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| 331 | SO25 | 11652.5 | 118 |
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| 333 | SO27 | 11622.5 | 118 |
| 334 | SO28 | 11607.5 | 248 |
| 335 | SO29 | 11592.5 | 118 |
| 336 | SO30 | 11577.5 | 248 |
| 337 | SO31 | 11562.5 | 118 |
| 338 | SO32 | 11547.5 | 248 |
| 339 | SO33 | 11532.5 | 118 |
| 340 | SO34 | 11517.5 | 248 |
| 341 | SO35 | 11502.5 | 118 |
| 342 | SO36 | 11487.5 | 248 |
| 343 | SO37 | 11472.5 | 118 |
| 344 | SO38 | 11457.5 | 248 |
| 345 | SO39 | 11442.5 | 118 |

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| 228 | SHLR | 6917.5 | -238 |
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| 230 | UPDN | 7087.5 | -238 |
| 231 | UPDN | 7172.5 | -238 |
| 232 | SHIELDING | 7257.5 | -238 |
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| 235 | TP33 | 7512.5 | -238 |
| 236 | TP34 | 7597.5 | -238 |
| 237 | TP35 | 7682.5 | -238 |
| 238 | TP36 | 7767.5 | -238 |
| 239 | TP37 | 7852.5 | -238 |
| 240 | TP38 | 7937.5 | -238 |
| 241 | TP39 | 8022.5 | -238 |
| 242 | TP40 | 8107.5 | -238 |

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| 287 | DRVL_B | 11932.5 | -238 |
| 288 | DRVL_B | 12017.5 | -238 |
| 289 | VCOMO | 12102.5 | -238 |
| 290 | VCOMO | 12187.5 | -238 |
| 291 | COM2_IN | 12272.5 | -238 |
| 292 | COM2_IN | 12357.5 | -238 |
| 293 | STBNL | 12303 | -77 |
| 294 | F_CtrlL(CLK4) | 12403 | -37 |
| 295 | STV2L(STV) | 12303 | 3 |
| 296 | STV1L(STV) | 12403 | 43 |
| 297 | CKVL(CLK1) | 12303 | 83 |
| 298 | UDL(CLK2) | 12403 | 123 |
| 299 | SYNC2L | 12303 | 163 |
| 300 | SYNC1L | 12403 | 203 |
| 301 | OEVL(CLK3) | 12303 | 243 |
| 302 | F_CtrlL(CLK4) | 12403 | 283 |

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| 407 | SO101 | 10512.5 | 118 |
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| 1458 | SO1143 | -6117.5 | 248 |
| 1459 | SO1144 | -6132.5 | 118 |
| 1460 | SO1145 | -6147.5 | 248 |
| 1461 | SO1146 | -6162.5 | 118 |
| 1462 | SO1147 | -6177.5 | 248 |
| 1463 | SO1148 | -6192.5 | 118 |
| 1464 | SO1149 | -6207.5 | 248 |
| 1465 | SO1150 | -6222.5 | 118 |
| 1466 | SO1151 | -6237.5 | 248 |
| 1467 | SO1152 | -6252.5 | 118 |
| 1468 | SO1153 | -6267.5 | 248 |
| 1469 | SO1154 | -6282.5 | 118 |
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| 1475 | SO1160 | -6372.5 | 118 |
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| 1477 | SO1162 | -6402.5 | 118 |
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| 1481 | SO1166 | -6462.5 | 118 |
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| 1483 | SO1168 | -6492.5 | 118 |
| 1484 | SO1169 | -6507.5 | 248 |
| 1485 | SO1170 | -6522.5 | 118 |

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| 1504 | SO1189 | -6807.5 | 248 |
| 1505 | SO1190 | -6822.5 | 118 |
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| 1512 | SO1197 | -6927.5 | 248 |
| 1513 | SO1198 | -6942.5 | 118 |
| 1514 | SO1199 | -6957.5 | 248 |
| 1515 | SO1200 | -6972.5 | 118 |
| 1516 | SO1201 | -6987.5 | 248 |
| 1517 | SO1202 | -7002.5 | 118 |
| 1518 | SO1203 | -7017.5 | 248 |
| 1519 | SO1204 | -7032.5 | 118 |
| 1520 | SO1205 | -7047.5 | 248 |
| 1521 | SO1206 | -7062.5 | 118 |
| 1522 | SO1207 | -7077.5 | 248 |
| 1523 | SO1208 | -7092.5 | 118 |
| 1524 | SO1209 | -7107.5 | 248 |
| 1525 | SO1210 | -7122.5 | 118 |
| 1526 | SO1211 | -7137.5 | 248 |
| 1527 | SO1212 | -7152.5 | 118 |
| 1528 | SO1213 | -7167.5 | 248 |
| 1529 | SO1214 | -7182.5 | 118 |
| 1530 | SO1215 | -7197.5 | 248 |
| 1531 | SO1216 | -7212.5 | 118 |
| 1532 | SO1217 | -7227.5 | 248 |
| 1533 | SO1218 | -7242.5 | 118 |
| 1534 | SO1219 | -7257.5 | 248 |
| 1535 | SO1220 | -7272.5 | 118 |
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| 1537 | SO1222 | -7302.5 | 118 |
| 1538 | SO1223 | -7317.5 | 248 |
| 1539 | SO1224 | -7332.5 | 118 |
| 1540 | SO1225 | -7347.5 | 248 |
| 1541 | SO1226 | -7362.5 | 118 |
| 1542 | SO1227 | -7377.5 | 248 |
| 1543 | SO1228 | -7392.5 | 118 |
| 1544 | SO1229 | -7407.5 | 248 |
| 1545 | SO1230 | -7422.5 | 118 |

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| 1564 | SO1249 | -7707.5 | 248 |
| 1565 | SO1250 | -7722.5 | 118 |
| 1566 | SO1251 | -7737.5 | 248 |
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| 1576 | SO1261 | -7887.5 | 248 |
| 1577 | SO1262 | -7902.5 | 118 |
| 1578 | SO1263 | -7917.5 | 248 |
| 1579 | SO1264 | -7932.5 | 118 |
| 1580 | SO1265 | -7947.5 | 248 |
| 1581 | SO1266 | -7962.5 | 118 |
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| 1583 | SO1268 | -7992.5 | 118 |
| 1584 | SO1269 | -8007.5 | 248 |
| 1585 | SO1270 | -8022.5 | 118 |
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| 1587 | SO1272 | -8052.5 | 118 |
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| 1589 | SO1274 | -8082.5 | 118 |
| 1590 | SO1275 | -8097.5 | 248 |
| 1591 | SO1276 | -8112.5 | 118 |
| 1592 | SO1277 | -8127.5 | 248 |
| 1593 | SO1278 | -8142.5 | 118 |
| 1594 | SO1279 | -8157.5 | 248 |
| 1595 | SO1280 | -8172.5 | 118 |
| 1596 | SO1281 | -8187.5 | 248 |
| 1597 | SO1282 | -8202.5 | 118 |
| 1598 | SO1283 | -8217.5 | 248 |
| 1599 | SO1284 | -8232.5 | 118 |
| 1600 | SO1285 | -8247.5 | 248 |
| 1601 | SO1286 | -8262.5 | 118 |
| 1602 | SO1287 | -8277.5 | 248 |
| 1603 | SO1288 | -8292.5 | 118 |
| 1604 | SO1289 | -8307.5 | 248 |
| 1605 | SO1290 | -8322.5 | 118 |

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| 1487 | SO1172 | -6552.5 | 118 |
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| 1489 | SO1174 | -6582.5 | 118 |
| 1490 | SO1175 | -6597.5 | 248 |
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| 1492 | SO1177 | -6627.5 | 248 |
| 1493 | SO1178 | -6642.5 | 118 |
| 1494 | SO1179 | -6657.5 | 248 |
| 1495 | SO1180 | -6672.5 | 118 |
| 1496 | SO1181 | -6687.5 | 248 |
| 1497 | SO1182 | -6702.5 | 118 |
| 1498 | SO1183 | -6717.5 | 248 |
| 1499 | SO1184 | -6732.5 | 118 |
| 1500 | SO1185 | -6747.5 | 248 |
| 1501 | SO1186 | -6762.5 | 118 |
| 1502 | SO1187 | -6777.5 | 248 |

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| 1547 | SO1232 | -7452.5 | 118 |
| 1548 | SO1233 | -7467.5 | 248 |
| 1549 | SO1234 | -7482.5 | 118 |
| 1550 | SO1235 | -7497.5 | 248 |
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| 1553 | SO1238 | -7542.5 | 118 |
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| 1556 | SO1241 | -7587.5 | 248 |
| 1557 | SO1242 | -7602.5 | 118 |
| 1558 | SO1243 | -7617.5 | 248 |
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| 1560 | SO1245 | -7647.5 | 248 |
| 1561 | SO1246 | -7662.5 | 118 |
| 1562 | SO1247 | -7677.5 | 248 |

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| 1607 | SO1292 | -8352.5 | 118 |
| 1608 | SO1293 | -8367.5 | 248 |
| 1609 | SO1294 | -8382.5 | 118 |
| 1610 | SO1295 | -8397.5 | 248 |
| 1611 | SO1296 | -8412.5 | 118 |
| 1612 | SO1297 | -8427.5 | 248 |
| 1613 | SO1298 | -8442.5 | 118 |
| 1614 | SO1299 | -8457.5 | 248 |
| 1615 | SO1300 | -8472.5 | 118 |
| 1616 | SO1301 | -8487.5 | 248 |
| 1617 | SO1302 | -8502.5 | 118 |
| 1618 | SO1303 | -8517.5 | 248 |
| 1619 | SO1304 | -8532.5 | 118 |
| 1620 | SO1305 | -8547.5 | 248 |
| 1621 | SO1306 | -8562.5 | 118 |
| 1622 | SO1307 | -8577.5 | 248 |

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|---|---|---|---|
| 1623 | SO1308 | -8592.5 | 118 |
| 1624 | SO1309 | -8607.5 | 248 |
| 1625 | SO1310 | -8622.5 | 118 |
| 1626 | SO1311 | -8637.5 | 248 |
| 1627 | SO1312 | -8652.5 | 118 |
| 1628 | SO1313 | -8667.5 | 248 |
| 1629 | SO1314 | -8682.5 | 118 |
| 1630 | SO1315 | -8697.5 | 248 |
| 1631 | SO1316 | -8712.5 | 118 |
| 1632 | SO1317 | -8727.5 | 248 |
| 1633 | SO1318 | -8742.5 | 118 |
| 1634 | SO1319 | -8757.5 | 248 |
| 1635 | SO1320 | -8772.5 | 118 |
| 1636 | SO1321 | -8787.5 | 248 |
| 1637 | SO1322 | -8802.5 | 118 |
| 1638 | SO1323 | -8817.5 | 248 |
| 1639 | SO1324 | -8832.5 | 118 |
| 1640 | SO1325 | -8847.5 | 248 |
| 1641 | SO1326 | -8862.5 | 118 |
| 1642 | SO1327 | -8877.5 | 248 |
| 1643 | SO1328 | -8892.5 | 118 |
| 1644 | SO1329 | -8907.5 | 248 |
| 1645 | SO1330 | -8922.5 | 118 |
| 1646 | SO1331 | -8937.5 | 248 |
| 1647 | SO1332 | -8952.5 | 118 |
| 1648 | SO1333 | -8967.5 | 248 |
| 1649 | SO1334 | -8982.5 | 118 |
| 1650 | SO1335 | -8997.5 | 248 |
| 1651 | SO1336 | -9012.5 | 118 |
| 1652 | SO1337 | -9027.5 | 248 |
| 1653 | SO1338 | -9042.5 | 118 |
| 1654 | SO1339 | -9057.5 | 248 |
| 1655 | SO1340 | -9072.5 | 118 |
| 1656 | SO1341 | -9087.5 | 248 |
| 1657 | SO1342 | -9102.5 | 118 |
| 1658 | SO1343 | -9117.5 | 248 |
| 1659 | SO1344 | -9132.5 | 118 |
| 1660 | SO1345 | -9147.5 | 248 |
| 1661 | SO1346 | -9162.5 | 118 |
| 1662 | SO1347 | -9177.5 | 248 |
| 1663 | SO1348 | -9192.5 | 118 |
| 1664 | SO1349 | -9207.5 | 248 |
| 1665 | SO1350 | -9222.5 | 118 |

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| 1684 | SO1369 | -9507.5 | 248 |
| 1685 | SO1370 | -9522.5 | 118 |
| 1686 | SO1371 | -9537.5 | 248 |
| 1687 | SO1372 | -9552.5 | 118 |
| 1688 | SO1373 | -9567.5 | 248 |
| 1689 | SO1374 | -9582.5 | 118 |
| 1690 | SO1375 | -9597.5 | 248 |
| 1691 | SO1376 | -9612.5 | 118 |
| 1692 | SO1377 | -9627.5 | 248 |
| 1693 | SO1378 | -9642.5 | 118 |
| 1694 | SO1379 | -9657.5 | 248 |
| 1695 | SO1380 | -9672.5 | 118 |
| 1696 | SO1381 | -9687.5 | 248 |
| 1697 | SO1382 | -9702.5 | 118 |
| 1698 | SO1383 | -9717.5 | 248 |
| 1699 | SO1384 | -9732.5 | 118 |
| 1700 | SO1385 | -9747.5 | 248 |
| 1701 | SO1386 | -9762.5 | 118 |
| 1702 | SO1387 | -9777.5 | 248 |
| 1703 | SO1388 | -9792.5 | 118 |
| 1704 | SO1389 | -9807.5 | 248 |
| 1705 | SO1390 | -9822.5 | 118 |
| 1706 | SO1391 | -9837.5 | 248 |
| 1707 | SO1392 | -9852.5 | 118 |
| 1708 | SO1393 | -9867.5 | 248 |
| 1709 | SO1394 | -9882.5 | 118 |
| 1710 | SO1395 | -9897.5 | 248 |
| 1711 | SO1396 | -9912.5 | 118 |
| 1712 | SO1397 | -9927.5 | 248 |
| 1713 | SO1398 | -9942.5 | 118 |
| 1714 | SO1399 | -9957.5 | 248 |
| 1715 | SO1400 | -9972.5 | 118 |
| 1716 | SO1401 | -9987.5 | 248 |
| 1717 | SO1402 | -10002.5 | 118 |
| 1718 | SO1403 | -10017.5 | 248 |
| 1719 | SO1404 | -10032.5 | 118 |
| 1720 | SO1405 | -10047.5 | 248 |
| 1721 | SO1406 | -10062.5 | 118 |
| 1722 | SO1407 | -10077.5 | 248 |
| 1723 | SO1408 | -10092.5 | 118 |
| 1724 | SO1409 | -10107.5 | 248 |
| 1725 | SO1410 | -10122.5 | 118 |

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| 1743 | SO1428 | -10392.5 | 118 |
| 1744 | SO1429 | -10407.5 | 248 |
| 1745 | SO1430 | -10422.5 | 118 |
| 1746 | SO1431 | -10437.5 | 248 |
| 1747 | SO1432 | -10452.5 | 118 |
| 1748 | SO1433 | -10467.5 | 248 |
| 1749 | SO1434 | -10482.5 | 118 |
| 1750 | SO1435 | -10497.5 | 248 |
| 1751 | SO1436 | -10512.5 | 118 |
| 1752 | SO1437 | -10527.5 | 248 |
| 1753 | SO1438 | -10542.5 | 118 |
| 1754 | SO1439 | -10557.5 | 248 |
| 1755 | SO1440 | -10572.5 | 118 |
| 1756 | SO1441 | -10587.5 | 248 |
| 1757 | SO1442 | -10602.5 | 118 |
| 1758 | SO1443 | -10617.5 | 248 |
| 1759 | SO1444 | -10632.5 | 118 |
| 1760 | SO1445 | -10647.5 | 248 |
| 1761 | SO1446 | -10662.5 | 118 |
| 1762 | SO1447 | -10677.5 | 248 |
| 1763 | SO1448 | -10692.5 | 118 |
| 1764 | SO1449 | -10707.5 | 248 |
| 1765 | SO1450 | -10722.5 | 118 |
| 1766 | SO1451 | -10737.5 | 248 |
| 1767 | SO1452 | -10752.5 | 118 |
| 1768 | SO1453 | -10767.5 | 248 |
| 1769 | SO1454 | -10782.5 | 118 |
| 1770 | SO1455 | -10797.5 | 248 |
| 1771 | SO1456 | -10812.5 | 118 |
| 1772 | SO1457 | -10827.5 | 248 |
| 1773 | SO1458 | -10842.5 | 118 |
| 1774 | SO1459 | -10857.5 | 248 |
| 1775 | SO1460 | -10872.5 | 118 |
| 1776 | SO1461 | -10887.5 | 248 |
| 1777 | SO1462 | -10902.5 | 118 |
| 1778 | SO1463 | -10917.5 | 248 |
| 1779 | SO1464 | -10932.5 | 118 |
| 1780 | SO1465 | -10947.5 | 248 |
| 1781 | SO1466 | -10962.5 | 118 |
| 1782 | SO1467 | -10977.5 | 248 |
| 1783 | SO1468 | -10992.5 | 118 |
| 1784 | SO1469 | -11007.5 | 248 |
| 1785 | SO1470 | -11022.5 | 118 |

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| 1666 | SO1351 | -9237.5 | 248 |
| 1667 | SO1352 | -9252.5 | 118 |
| 1668 | SO1353 | -9267.5 | 248 |
| 1669 | SO1354 | -9282.5 | 118 |
| 1670 | SO1355 | -9297.5 | 248 |
| 1671 | SO1356 | -9312.5 | 118 |
| 1672 | SO1357 | -9327.5 | 248 |
| 1673 | SO1358 | -9342.5 | 118 |
| 1674 | SO1359 | -9357.5 | 248 |
| 1675 | SO1360 | -9372.5 | 118 |
| 1676 | SO1361 | -9387.5 | 248 |
| 1677 | SO1362 | -9402.5 | 118 |
| 1678 | SO1363 | -9417.5 | 248 |
| 1679 | SO1364 | -9432.5 | 118 |
| 1680 | SO1365 | -9447.5 | 248 |
| 1681 | SO1366 | -9462.5 | 118 |
| 1682 | SO1367 | -9477.5 | 248 |

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| 1726 | SO1411 | -10137.5 | 248 |
| 1727 | SO1412 | -10152.5 | 118 |
| 1728 | SO1413 | -10167.5 | 248 |
| 1729 | SO1414 | -10182.5 | 118 |
| 1730 | SO1415 | -10197.5 | 248 |
| 1731 | SO1416 | -10212.5 | 118 |
| 1732 | SO1417 | -10227.5 | 248 |
| 1733 | SO1418 | -10242.5 | 118 |
| 1734 | SO1419 | -10257.5 | 248 |
| 1735 | SO1420 | -10272.5 | 118 |
| 1736 | SO1421 | -10287.5 | 248 |
| 1737 | SO1422 | -10302.5 | 118 |
| 1738 | SO1423 | -10317.5 | 248 |
| 1739 | SO1424 | -10332.5 | 118 |
| 1740 | SO1425 | -10347.5 | 248 |
| 1741 | SO1426 | -10362.5 | 118 |
| 1742 | SO1427 | -10377.5 | 248 |

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| 1786 | SO1471 | -11037.5 | 248 |
| 1787 | SO1472 | -11052.5 | 118 |
| 1788 | SO1473 | -11067.5 | 248 |
| 1789 | SO1474 | -11082.5 | 118 |
| 1790 | SO1475 | -11097.5 | 248 |
| 1791 | SO1476 | -11112.5 | 118 |
| 1792 | SO1477 | -11127.5 | 248 |
| 1793 | SO1478 | -11142.5 | 118 |
| 1794 | SO1479 | -11157.5 | 248 |
| 1795 | SO1480 | -11172.5 | 118 |
| 1796 | SO1481 | -11187.5 | 248 |
| 1797 | SO1482 | -11202.5 | 118 |
| 1798 | SO1483 | -11217.5 | 248 |
| 1799 | SO1484 | -11232.5 | 118 |
| 1800 | SO1485 | -11247.5 | 248 |
| 1801 | SO1486 | -11262.5 | 118 |
| 1802 | SO1487 | -11277.5 | 248 |

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| 1803 | SO1488 | -11292.5 | 118 |
| 1804 | SO1489 | -11307.5 | 248 |
| 1805 | SO1490 | -11322.5 | 118 |
| 1806 | SO1491 | -11337.5 | 248 |
| 1807 | SO1492 | -11352.5 | 118 |
| 1808 | SO1493 | -11367.5 | 248 |
| 1809 | SO1494 | -11382.5 | 118 |
| 1810 | SO1495 | -11397.5 | 248 |
| 1811 | SO1496 | -11412.5 | 118 |
| 1812 | SO1497 | -11427.5 | 248 |
| 1813 | SO1498 | -11442.5 | 118 |
| 1814 | SO1499 | -11457.5 | 248 |
| 1815 | SO1500 | -11472.5 | 118 |
| 1816 | SO1501 | -11487.5 | 248 |
| 1817 | SO1502 | -11502.5 | 118 |
| 1818 | SO1503 | -11517.5 | 248 |
| 1819 | SO1504 | -11532.5 | 118 |
| 1820 | SO1505 | -11547.5 | 248 |
| 1821 | SO1506 | -11562.5 | 118 |
| 1822 | SO1507 | -11577.5 | 248 |
| 1823 | SO1508 | -11592.5 | 118 |
| 1824 | SO1509 | -11607.5 | 248 |
| 1825 | SO1510 | -11622.5 | 118 |
| 1826 | SO1511 | -11637.5 | 248 |
| 1827 | SO1512 | -11652.5 | 118 |
| 1828 | SO1513 | -11667.5 | 248 |
| 1829 | SO1514 | -11682.5 | 118 |
| 1830 | SO1515 | -11697.5 | 248 |
| 1831 | SO1516 | -11712.5 | 118 |
| 1832 | SO1517 | -11727.5 | 248 |
| 1833 | SO1518 | -11742.5 | 118 |
| 1834 | SO1519 | -11757.5 | 248 |
| 1835 | SO1520 | -11772.5 | 118 |
| 1836 | SO1521 | -11787.5 | 248 |
| 1837 | SO1522 | -11802.5 | 118 |
| 1838 | SO1523 | -11817.5 | 248 |
| 1839 | SO1524 | -11832.5 | 118 |
| 1840 | SO1525 | -11847.5 | 248 |
| 1841 | SO1526 | -11862.5 | 118 |
| 1842 | SO1527 | -11877.5 | 248 |
| 1843 | SO1528 | -11892.5 | 118 |
| 1844 | SO1529 | -11907.5 | 248 |
| 1845 | SO1530 | -11922.5 | 118 |

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|---|---|---|---|
| 1863 | STV1R(STV) | -12303 | 3 |
| 1864 | F_CtrlR(CLK4) | -12403 | -37 |
| 1865 | STBNR | -12303 | -77 |

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|---|---|---|---|
| 1846 | SO1531 | -11937.5 | 248 |
| 1847 | SO1532 | -11952.5 | 118 |
| 1848 | SO1533 | -11967.5 | 248 |
| 1849 | SO1534 | -11982.5 | 118 |
| 1850 | SO1535 | -11997.5 | 248 |
| 1851 | SO1536 | -12012.5 | 118 |
| 1852 | SHIELDING | -12055 | 263 |
| 1853 | COM1_OUT | -12105 | 263 |
| 1854 | COM1_OUT | -12155 | 263 |
| 1855 | SHIELDING | -12205 | 263 |
| 1856 | F_CtrlR(CLK4) | -12403 | 283 |
| 1857 | OEVR(CLK3) | -12303 | 243 |
| 1858 | SYNC1R | -12403 | 203 |
| 1859 | SYNC2R | -12303 | 163 |
| 1860 | UDR(CLK2) | -12403 | 123 |
| 1861 | CKVR(CLK1) | -12303 | 83 |
| 1862 | STV2R(STV) | -12403 | 43 |

## 18. REVISION HISTORY

| Reversion | Content | Date |
|---|---|---|
| 1.0 | New issue | 2013/11/26 |

## Appendix A : BIST pattern

R→G→B→Black→White→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern →Chess board (L255/L0)→Flicker pattern→Black background with white out frame