MAX17574

4.5V–60V, 3A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

General Description

The MAX17574, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 3A current. Output voltage is programmable from 0.9V to 90%V_{IN}. The feedback voltage regulation accuracy over -40°C to +125°C is ±0.9%.

The MAX17574 features a peak-current-mode control architecture. The device can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) control schemes. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. An open-drain $\overline{RESET}$ pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

The MAX17574 is available in a 24-pin (4mm x 5mm) TQFN package. Simulation models are available.

Applications

- Industrial Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - Internal Compensation for Any Output Voltage
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Output Adjustable from 0.9V to 90%V_{IN}
  - Delivers up to 3A Current Over Temperature
  - 100kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization
- Reduces Power Dissipation
  - Peak Efficiency > 90%
  - PFM and DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - 2.8µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup Mode Overload Protection
  - Adjustable Soft-Start and Prebiased Power-Up
  - Built-In Output-Voltage Monitoring with $\overline{RESET}$
  - Programmable EN/UVLO Threshold
  - Monotonic Startup Into Prebiased Load
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

19-8635; Rev 0; 9/16

maxim integrated™

Absolute Maximum Ratings

V_{IN} to PGND .....-0.3V to +65V
EN/UVLO to SGND .....-0.3V to +65V
LX to PGND.....-0.3V to V_{IN} + 0.3V
$EXTV_{CC}$ to SGND .....-0.3V to +26V
BST to PGND .....-0.3V to +70V
BST to LX .....-0.3V to +6.5V
BST to V_{CC} .....-0.3V to +65V
FB, $\overline{RESET}$, SS, MODE/SYNC, V_{CC}, RT, CF to SGND.....-0.3V to +6.5V
FB to SGND .....-0.3V to +1.5V
PGND to SGND.....-0.3V to +0.3V
LX Total RMS Current ..... ±5.6A
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (multilayer Board) (T_A = +70°C, derate 28.6mW/°C above +70°C.).....2285.7mW
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Junction temperature greater than +125°C degrades operating lifetimes.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1.8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2KΩ (f_{SW} = 500kHz), C_{VCC} = 2.2µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 1V, LX = SS = CF = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	$V_{IN\_}$		4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		2.8	4.5	µA
Input Quiescent Current	I_{Q_PFM}	MODE/SYNC = RT = open, $EXTV_{CC}$ = 5V		61		µA
		MODE/SYNC = open, $EXTV_{CC}$ = 5V		71		µA
	I_{Q_DCM}	DCM Mode, V_{LX} = 0.1V		1.2	1.8	mA
	I_{Q_PWM}	Normal switching mode, F_{SW} = 500kHz, V_{FB} = 0.8V		14		mA
ENABLE/UVLO (EN)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.26	V
EN/UVLO Threshold	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.131	V
EN/UVLO Threshold	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling		0.8		V
EN Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	-50	0	+50	nA
V_{CC} LDO						
V_{CC} Output Voltage Range	V_{CC}	1mA ≤ I_{VCC} ≤ 25mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 60V; I_{VCC} = 1mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 7V	40	65	130	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V , I_{VCC} = 20mA	4.2			V
V_{CC} UVLO	V_{CC-UVR}	Rising	4.05	4.2	4.3	V
	V_{CC-UVF}	Falling	3.65	3.8	3.9	V

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2KΩ (f_{SW} = 500kHz), C_{VCC} = 2.2µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 1V, LX = SS = CF = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXT LDO						
$EXTV_{CC}$ Operating Voltage Range			4.84		24	V
$EXTV_{CC}$ Switchover Threshold	$EXTV_{CC}$	Rising	4.56	4.7	4.84	V
	$EXTV_{CC}$	Falling	4.3	4.45	4.6	V
$EXTV_{CC}$ Dropout	$EXTV_{CC-DO}$	$EXTV_{CC}$ = 4.75V, IV_{CC} = 20mA			0.3	V
$EXTV_{CC}$ Current Limit	IV_{CC-MAX}	V_{CC} = 4.5V, $EXTV_{CC}$ = 7V	40	85	160	mA
POWER MOSFETS						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A ,sourcing		100	200	mΩ
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A , sinking		64	125	mΩ
LX Leakage Current	ILX_{LKG}	T_A = 25°C, V_{LX} = (V_{PGND} + 1V) to (V_{IN} - 1V)	-2		+2	µA
SOFT START						
Soft-Start Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}	MODE/SYNC = SGND or V_{CC}	0.892	0.9	0.908	V
FB Regulation Voltage	V_{FB_REG}	MODE/SYNC = OPEN	0.892	0.916	0.934	V
FB Input Leakage Current	I_{FB}	0 < V_{FB} < 1V, T_A = 25°C	-50		+50	nA
MODE/SYNC						
MODE Threshold	V_{M-DCM}	MODE = V_{CC} (DCM Mode)	V_{CC} – 0.65			V
MODE Threshold	V_{M-PFM}	MODE = OPEN (PFM Mode)		V_{CC}/2		V
MODE Threshold	V_{M-PWM}	MODE = SGND (PWM Mode)			0.75	V
SYNC Frequency Capture Range			1.1 x F_{SW}		1.4 x F_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IL}				0.8	V
	V_{IH}		2.1			V

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = 40.2KΩ (f_{SW} = 500kHz), C_{VCC} = 2.2µF, V_{SGND} = V_{PGND} = $V_{MODE/SYNC}$ = V_{EXTVCC} = 0V, V_{FB} = 1V, LX = SS = CF = $\overline{RESET}$ = OPEN, V_{BST} to V_{LX} = 5V, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

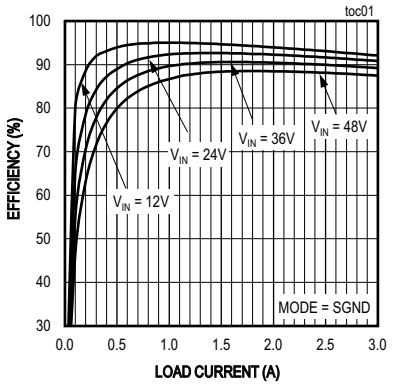
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Peak Current Limit Threshold	$I_{PEAK-LIMIT}$		4.4	5.25	5.85	A
Runaway Current Limit Threshold	$I_{RUNAWAY-LIMIT}$		4.9	5.8	6.7	A
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	MODE/SYNC = OPEN or MODE/SYNC = V_{CC}	-0.25	0	+0.25	A
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	MODE/SYNC = SGND		-1.8		A
PFM Current-Limit Threshold	I_{PFM}	MODE/SYNC = OPEN	0.575	0.725	0.9	A
RT/SYNC						
Switching Frequency	F_{SW}	R_{RT} = 40.2KΩ	475	500	525	kHz
		R_{RT} = OPEN	460	500	540	kHz
		R_{RT} = 8.06KΩ	1950	2200	2450	kHz
		R_{RT} = 210KΩ	90	100	110	kHz
V_{FB} Undervoltage Trip Level to Cause HICCUP	$V_{OUT-HICF}$		0.56	0.58	0.65	V
HICCUP Timeout				32768		Cycles
Minimum On-Time	t_{ON_MIN}			60	80	ns
Minimum off-Time	t_{OFF_MIN}		140		160	ns
LX Dead Time				5		ns
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			400	mV
$\overline{RESET}$ Output Leakage Current		T_A = T_J = 25°C, $V_{\overline{RESET}}$ = 5.5V	-0.1		+0.1	µA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.8	95	97.8	%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.5	92	94.6	%
$\overline{RESET}$ De-Assertion Delay After FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDNR}	Temp rising		165		°C
Thermal Shutdown Hysteresis	T_{SHDNHY}			10		°C

Note 2: All limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

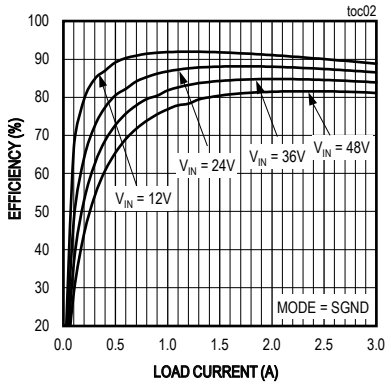
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

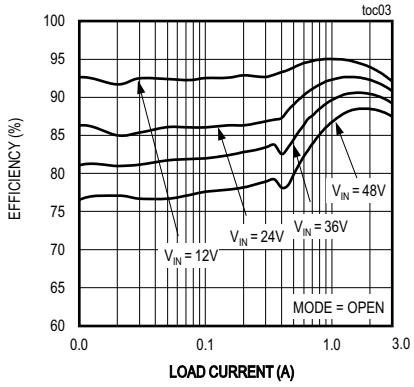
MAX17574, 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT, EFFICIENCY VS. LOAD CURRENT



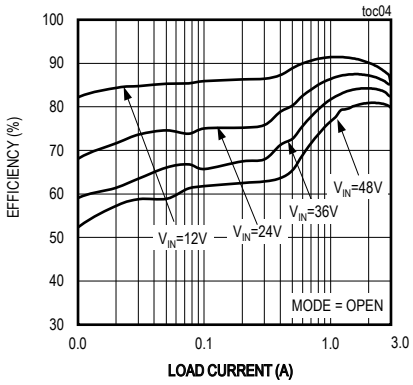
MAX17574, 3.3V OUTPUT, PWM MODE,FIGURE 4 CIRCUIT, EFFICIENCY VS. LOAD CURRENT



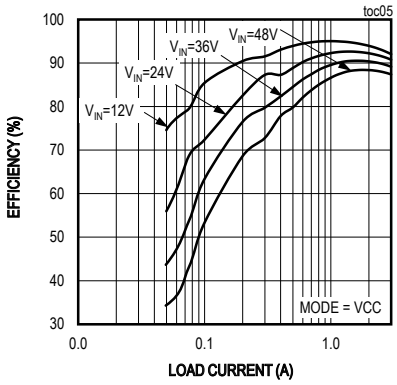
MAX17574,5V OUTPUT, PFM MODE, FIGURE 3 CIRCUIT, EFFICIENCY VS. LOAD CURRENT



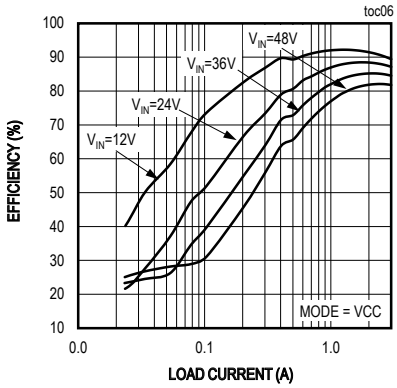
MAX17574, 3.3V OUTPUT, PFM MODE,FIGURE 4 CIRCUIT, EFFICIENCY vs. LOAD CURRENT



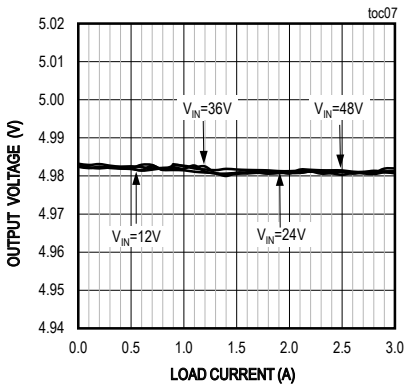
MAX17574, 5V OUTPUT, DCM MODE,FIGURE 3 CIRCUIT, EFFICIENCY VS. LOAD CURRENT



MAX17574, 3.3V OUTPUT, DCM MODE,FIGURE 4 CIRCUIT, EFFICIENCY VS. LOAD CURRENT



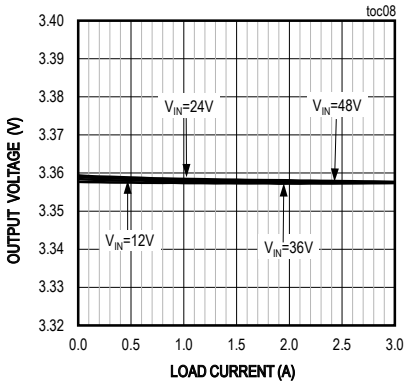
MAX17574, 5V OUTPUT, PWM MODE,FIGURE 3 CIRCUIT, LOAD AND LINE REGULATION



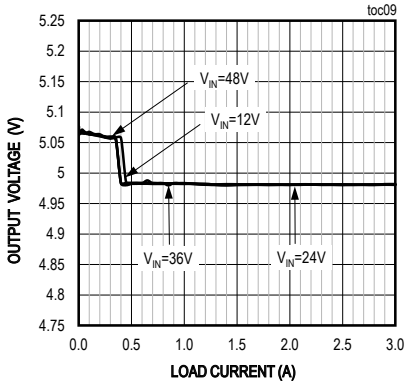
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17574, 3.3V OUTPUT, PWM MODE,FIGURE 4 CIRCUIT, LOAD AND LINE REGULATION



MAX17574, 5V OUTPUT, PFM MODE,FIGURE 3 CIRCUIT, LOAD AND LINE REGULATION



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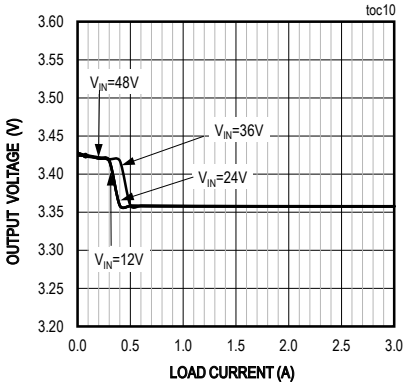
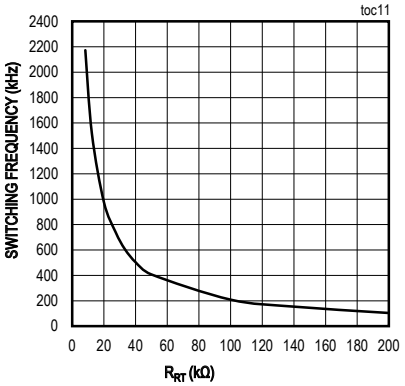
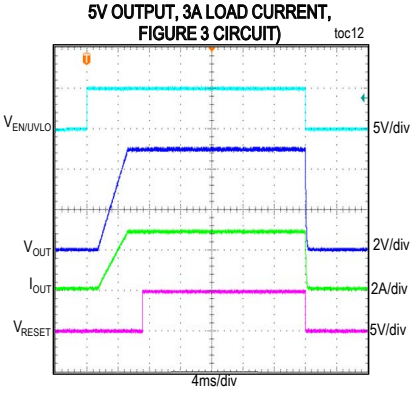


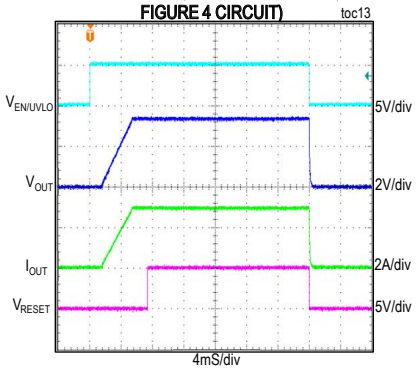
SWITCHING FREQUENCY vs. RT RESISTANCE



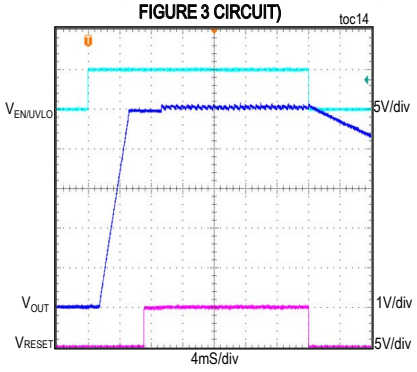
MAX17574, SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, 3A LOAD CURRENT, FIGURE 3 CIRCUIT)



MAX17574, SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, 3A LOAD CURRENT, FIGURE 4 CIRCUIT)



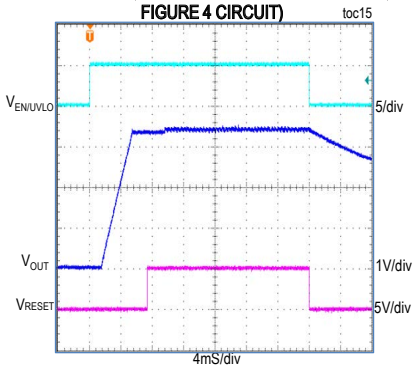
MAX17574, SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT,PFM MODE 5mA LOAD CURRENT, FIGURE 3 CIRCUIT)



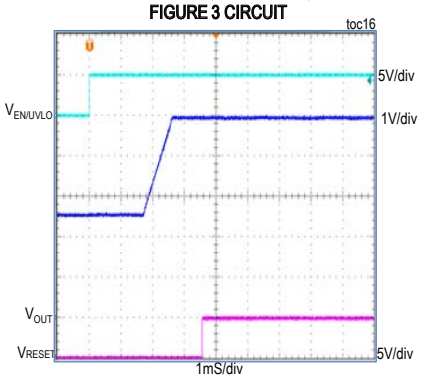
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

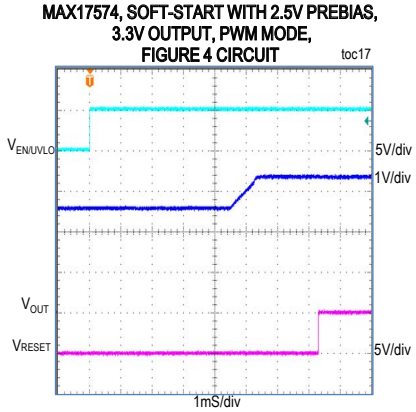
MAX17574, SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT,PFM MODE 5mA LOAD CURRENT, FIGURE 4 CIRCUIT)



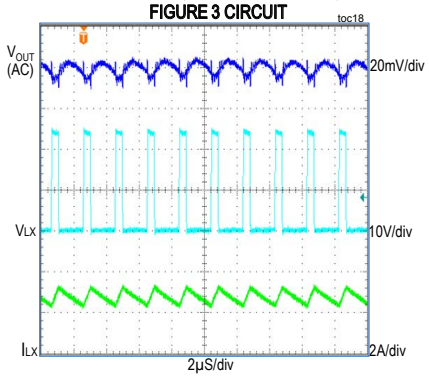
MAX17574, SOFT-START WITH 2.5V PREBIAS, 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



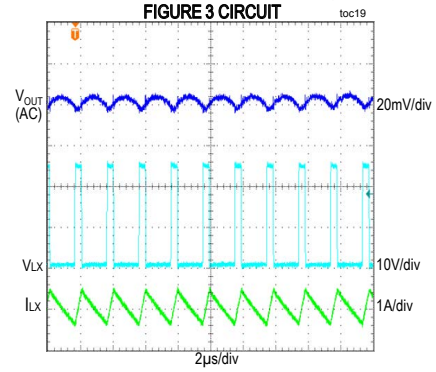
MAX17574, SOFT-START WITH 2.5V PREBIAS, 3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



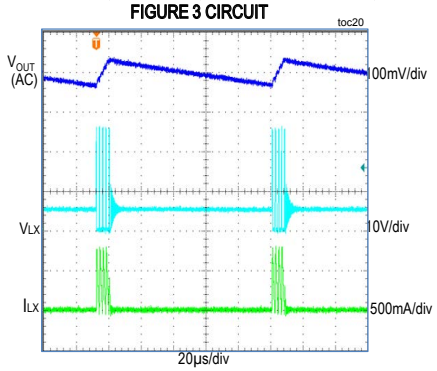
MAX17574, STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 3A LOAD CURRENT, FIGURE 3 CIRCUIT



MAX17574, STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, NO LOAD CURRENT, FIGURE 3 CIRCUIT



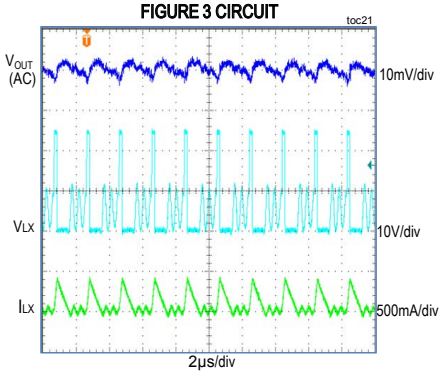
MAX17574, STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, PFM MODE, 25mA LOAD CURRENT, FIGURE 3 CIRCUIT



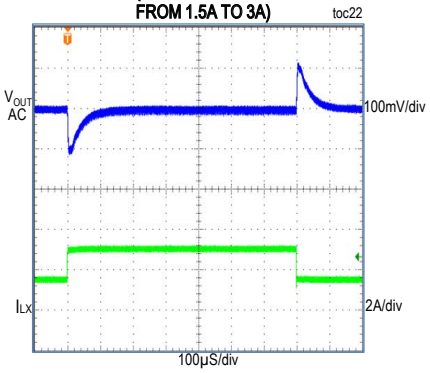
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

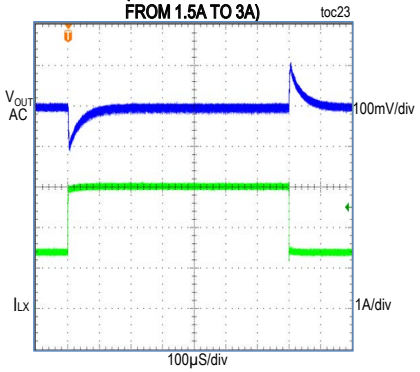
MAX17574, STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, DCM MODE, 75mA LOAD CURRENT, FIGURE 3 CIRCUIT



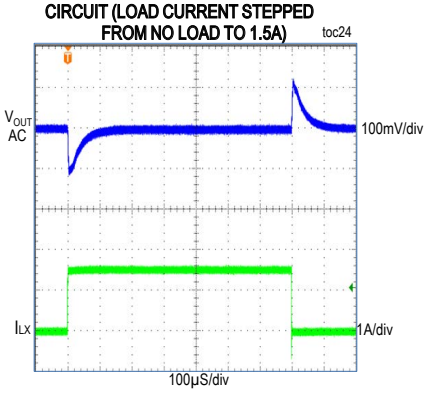
MAX17574, 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM 1.5A TO 3A)



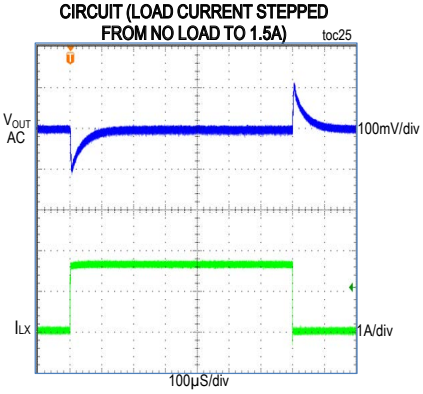
MAX17574, 3.3V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM 1.5A TO 3A)



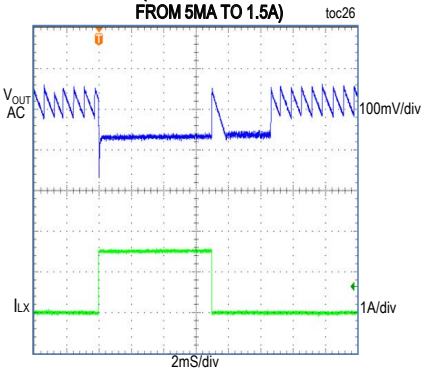
MAX17574, 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM NO LOAD TO 1.5A)



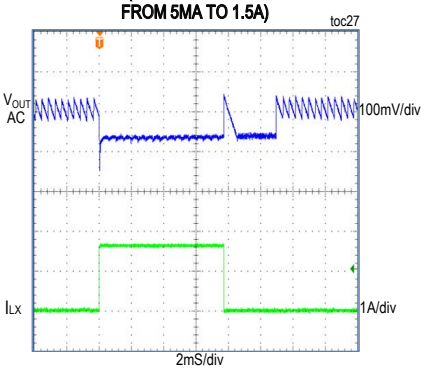
MAX17574, 3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM NO LOAD TO 1.5A)



MAX17574, 5V OUTPUT, PFM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM 5MA TO 1.5A)



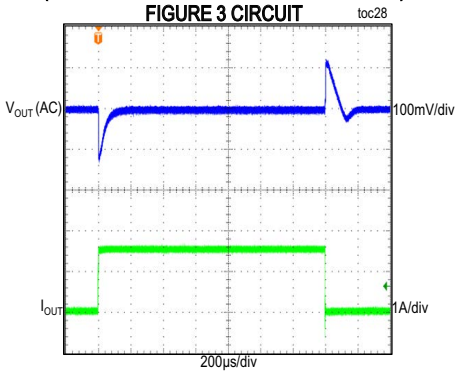
MAX17574, 3.3V OUTPUT, PFM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM 5MA TO 1.5A)



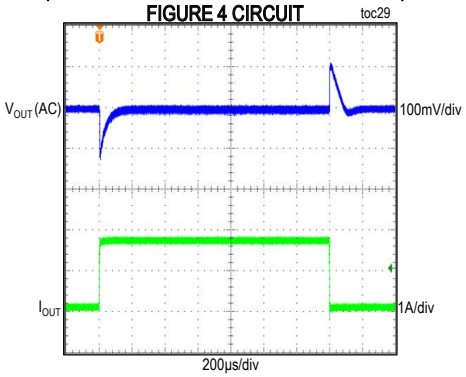
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{GND} = V_{PGND} = 0V, CV_{IN} = 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

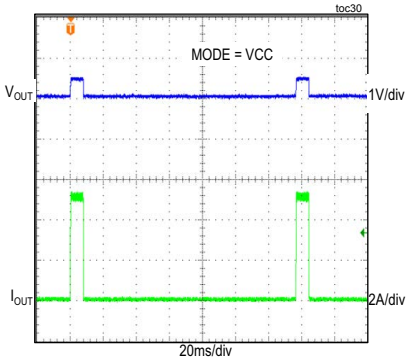
MAX17574, 5V OUTPUT, DCM MODE
(LOAD CURRENT STEPPED FROM 50mA TO 1.5A)
FIGURE 3 CIRCUIT



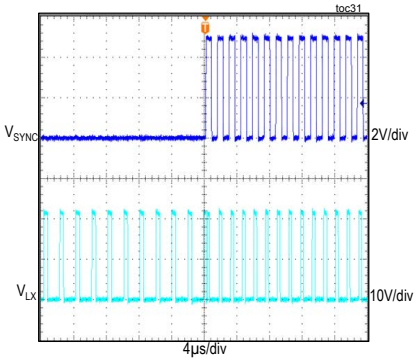
MAX17574, 3.3V OUTPUT, DCM MODE
(LOAD CURRENT STEPPED FROM 50mA TO 1.5A)
FIGURE 4 CIRCUIT



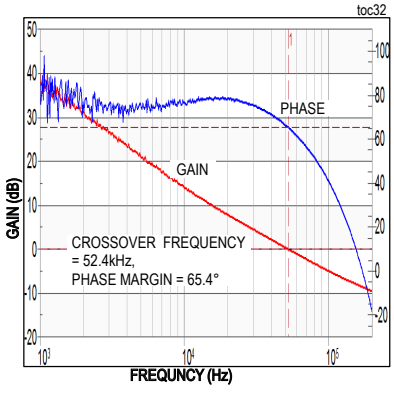
MAX17574, OVERLOAD PROTECTION
5V OUTPUT, FIGURE 3 CIRCUIT



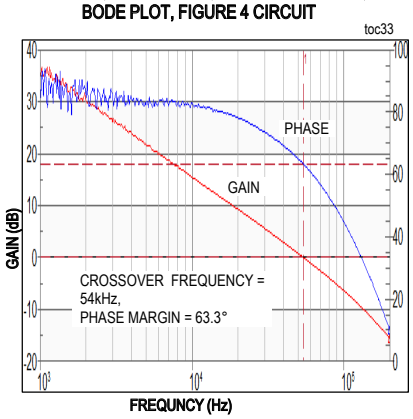
MAX17574, APPLICATION OF EXTERNAL CLOCK AT 700kHz,
5V OUTPUT, FIGURE 3 CIRCUIT



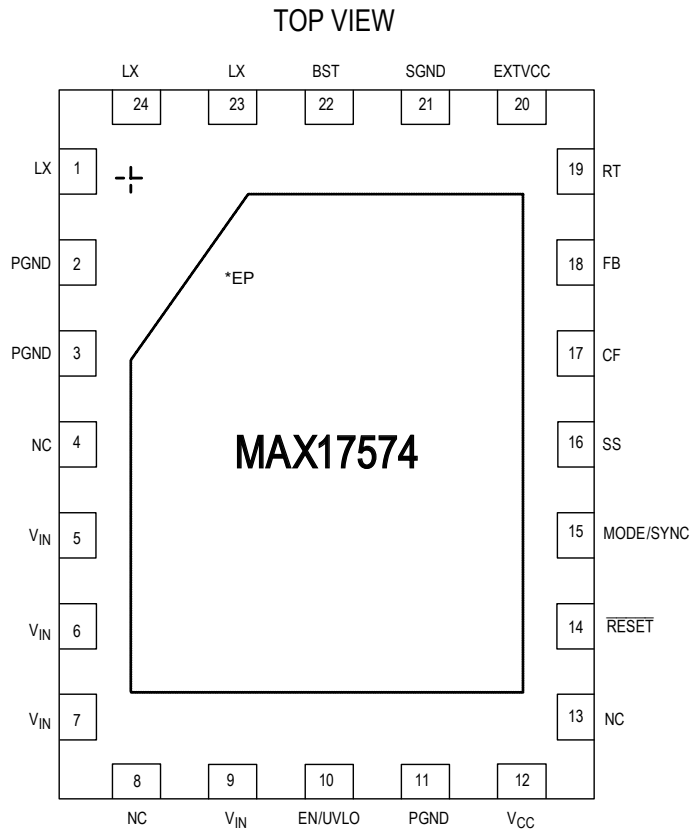
MAX17574, 5V OUTPUT, 3A LOAD CURRENT,
BODE PLOT, FIGURE 3 CIRCUIT



MAX17574, 3.3V OUTPUT, 3A LOAD CURRENT,
BODE PLOT, FIGURE 4 CIRCUIT



Pin Configuration



24-pin TQFN 4mm X 5mm

*EXPOSED PAD (CONNECT TO GROUND)

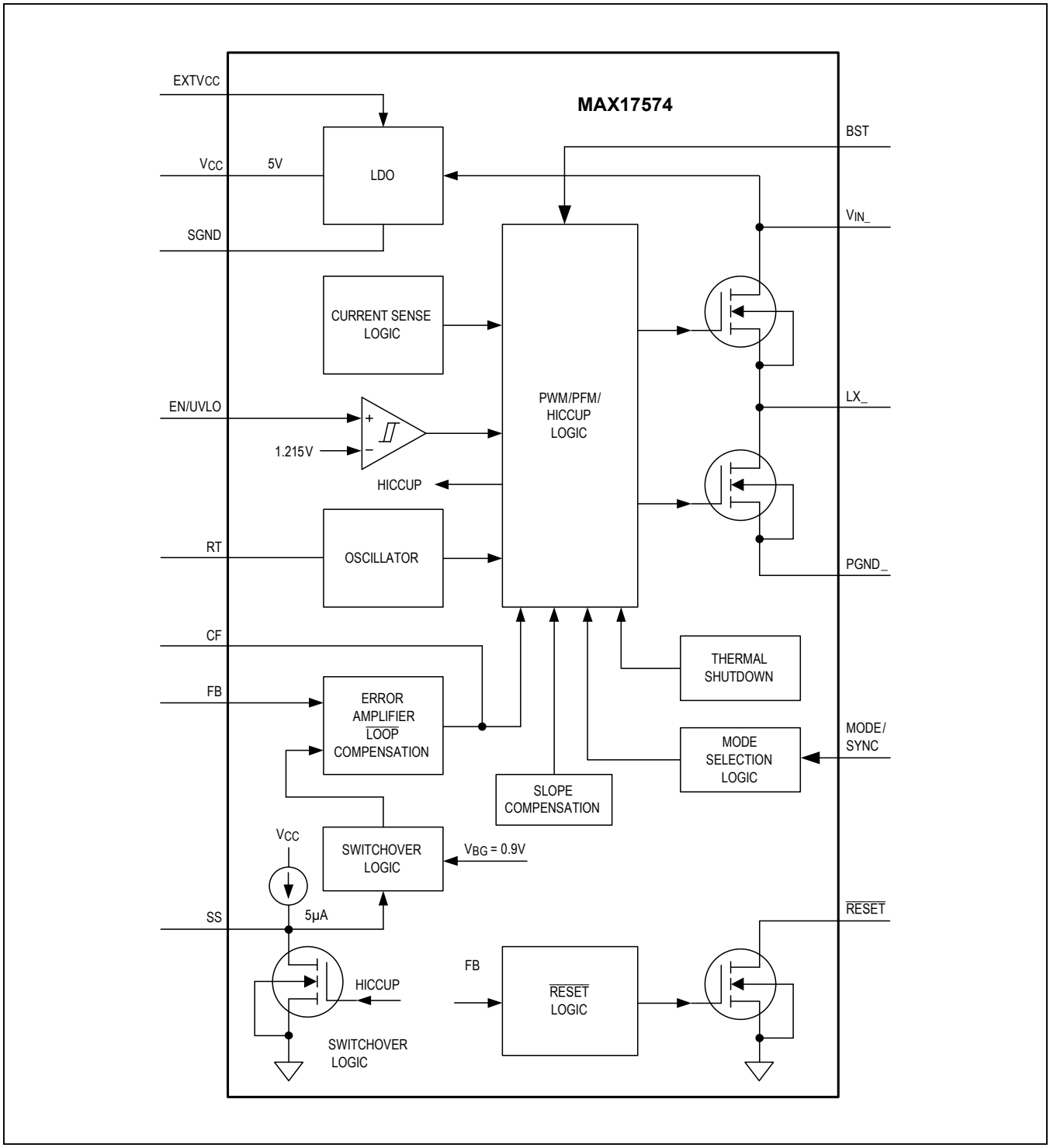
Pin Description

NAME	PIN	FUNCTION
1, 23, 24	LX	Switching Nodes. Connect LX pins to the switching side of the inductor.
2, 3, 11	PGND	Power Ground Pins of the Converter. Connect externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitor. Refer to the *MAX17574 Evaluation Kit* data sheet for a layout example
4, 8, 13	N.C.	No Connect. Keep these pins open.
5–7, 9	V_{IN}	Power-Supply Input. The input supply range is from 4.5V to 60V.

Pin Description (continued)

NAME	PIN	FUNCTION
10	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the part turns on. Connect to V_{IN} pins for always-on operation.
12	V_{CC}	5V LDO Output of the Part. Bypass V_{CC} with a 2.2µF ceramic capacitance to SGND.
14	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 1024 cycles after FB rises above 95% of its set value.
15	MODE/ SYNC	MODE pin configures the device to operate either in PWM, PFM, or DCM modes of operation. Leave MODE unconnected for PFM operation (pulse-skipping at light loads). Connect MODE to SGND for constant-frequency PWM operation at all loads. Connect MODE to V_{SS} for DCM operation. The device can be synchronized to an external clock using this pin. See the *Mode Selection (MODE)* section and the *External Frequency Synchronization* section for more details.
16	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
17	CF	At switching frequencies lower than 500kHz, connect a capacitor from CF to FB. Leave CF open if switching frequency is equal or more than 500kHz.
18	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details
19	RT	Connect a resistor from RT to SGND to set the regulator's switching frequency between 100kHz and 2.2MHz. Leave RT open for the default 500kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
20	$EXTV_{CC}$	External Power Supply Input for the Internal LDO. Applying a voltage between 4.84V and 24V at $EXTV_{CC}$ pin will bypass the internal LDO and improve efficiency. Add a 4.7Ω resistor from buck output to this pin to limit V_{CC} bypass cap discharge current during output short-circuit condition. Also, add a local bypassing on this pin to SGND.
21	SGND	Analog Ground.
22	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
—	EP	Exposed Pad. Connect to the GND pin of the IC. Connect to a large copper plane below the IC to improve heat dissipation capability.

Functional (or Block) Diagram



Detailed Description

The MAX17574, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 3A current. Output voltage is programmable from 0.9V to 90%V_{IN}. The feedback voltage regulation accuracy over -40°C to +125°C is ±0.9%.

The MAX17574 features a peak-current-mode control architecture. The device can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM) or discontinuous-conduction mode (DCM) control schemes. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/under voltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. An open-drain $\overline{RESET}$ pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

Mode Selection (MODE)

The logic state of the MODE pin is latched when V_{CC} and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is open at power-up, the device operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the device operates in constant-frequency PWM mode at all loads. Finally, if the MODE pin is connected to V_{CC} at power-up, the device operates in constant-frequency DCM mode at light loads. State changes on the MODE pin are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 725mA every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The trade-off is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads. The output voltage ripple in PFM mode can be reduced by increasing the amount of output capacitance.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes.

Linear Regulator (V_{CC} and $EXTV_{CC}$)

The MAX17574 has two internal LDO (Low Dropout) regulators which powers V_{CC}. One LDO is powered from $V_{IN\_}$ (INLDO) and the other LDO is powered from $EXTV_{CC}$ ($EXTV_{CC}$ LDO). Only one of the two LDOs is in operation at a time, depending on the voltage levels present at EXTVCC. If $EXTV_{CC}$ voltage is greater than 4.7V (typ), V_{CC} is powered from $EXTV_{CC}$. If $EXTV_{CC}$ is lower than 4.7V (typ), V_{CC} is powered from $V_{IN\_}$. Powering V_{CC} from $EXTV_{CC}$ increases efficiency at higher input voltages. $EXTV_{CC}$ voltage should not exceed 24V.

Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver and re-charges the external bootstrap capacitor. Both INLDO and $EXTV_{CC}$ LDO can source up to 65mA. The MAX17574 employs an undervoltage lockout circuit that forces both the regulators off when V_{CC} falls below 3.8V (typ). The regulators can be immediately enabled again when V_{CC} > 4.2V. The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck converter output is connected to $EXTV_{CC}$ pin, if the output is shorted to ground then the transfer from EXTVCCLDO to INLDO happens seamlessly without any impact on the normal functionality.

Switching Frequency Selection

The switching frequency of the device can be programmed from 100kHz to 2.2MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} = \frac{21 \times 10^3}{F_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open causes the device to operate at the default switching frequency of 500kHz. See Table 1 for RT resistor values for a few common switching frequencies.

External Frequency Synchronization

The internal oscillator of the MAX17574 can be synchronized to an external clock signal on the MODE/SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency programmed by the RT resistor. When an external clock is applied to MODE/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on RT setting) after detecting 16 external clock edges. The converter will operate in PWM mode during synchronization operation.

When the external clock is applied on-fly then the mode of operation will change to PWM from the initial state of PFM/DCM/PWM. When the external clock is removed on-fly then the internal oscillator frequency changes to the RT set frequency and the converter will still continue to operate in PWM mode. The minimum external clock pulse-width high should be greater than 50ns. See the MODE/SYNC section in the *Electrical Characteristics* table for details.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
500	OPEN
100	210
200	102
400	49.9
1000	19.1
2200	8.06

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + 0.15))}{1 - (f_{SW(MAX)} \times t_{OFF(MAX)})} + (I_{OUT(MAX)} \times 0.175)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

Where V_{OUT} is the steady-state output voltage, $I_{OUT\ (MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor, $f_{SW(MAX)}$ is the maximum switching frequency, $t_{OFF(MAX)}$ is the worst-case minimum switch off-time (160ns) and $t_{ON\text{-}MIN}$ is the worst-case minimum switch on-time (80ns).

Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 5.25A (typ). A runaway current limit on the high-side switch current at 5.8A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if, due to a fault condition, feedback voltage drops to 0.58V (typ) any time after soft-start is complete, and hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload condition, if feedback voltage does not exceed 0.58V, the device switches at half the programmed switching frequency. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the MAX17574 starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1-D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D = V_{OUT}/V_{IN} is the duty ratio of the controller, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT}}{f_{SW}}$$

Where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of 5.25A.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$tRESPONSE \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right)$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output-voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. Select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 55kHz.

Soft-Start capacitor selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to GND.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND. Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}.

Loop Compensation

The device is internally loop compensated. However, if the switching frequency is less than 500kHz, connect a 0402 capacitor C6 between the CF pin and the FB pin. Use **Table 2** to select the value of C6.

Table 2. C6 Capacitor Value at Various Switching Frequencies

SWITCHING FREQUENCY RANGE (kHz)	C6 (pF)
200 to 300	2.2
300 to 400	1.2
400 to 500	0.75

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R6 from the output to the FB pin as follows:

$$R6 = \frac{216 \times 10^3}{f_C \times C_{OUT}}$$

where R6 is in kΩ, crossover frequency f_C is in kHz, and the output capacitor C_{OUT} is in µF. Choose f_C to be 1/9th of the switching frequency, f_{SW}, if the switching frequency is less than or equal to 500kHz. If the switching frequency is more than 500kHz, select f_C to be 55kHz. Calculate resistor R7 from the FB pin to SGND as follows:

$$R7 = \frac{R6 \times 0.9}{(V_{OUT} - 0.9)}$$

R7 is in kΩ.

Power dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

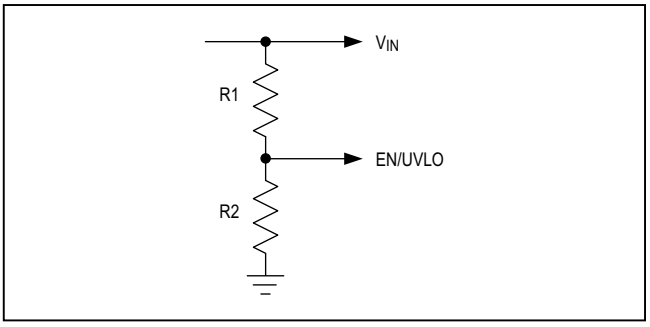


Figure 1. Setting the Input Undervoltage Lockout

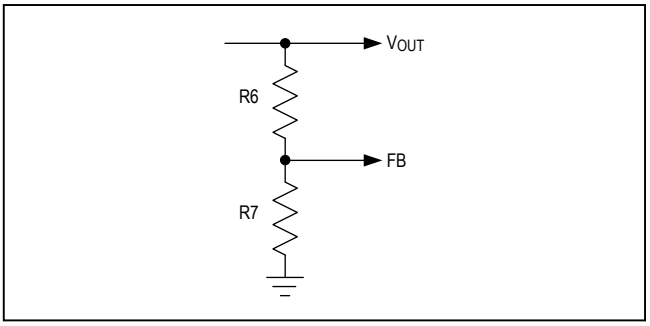


Figure 2. Adjusting Output Voltage

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - \left(I_{OUT}^{2} \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

Where P_{OUT} is the output power, η is the efficiency of the converter and R_{DCR} is the DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 35°C / W$$

$$\theta_{JC} = 1.8°C / W$$

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Junction temperatures greater than +125°C degrades operating lifetimes.

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

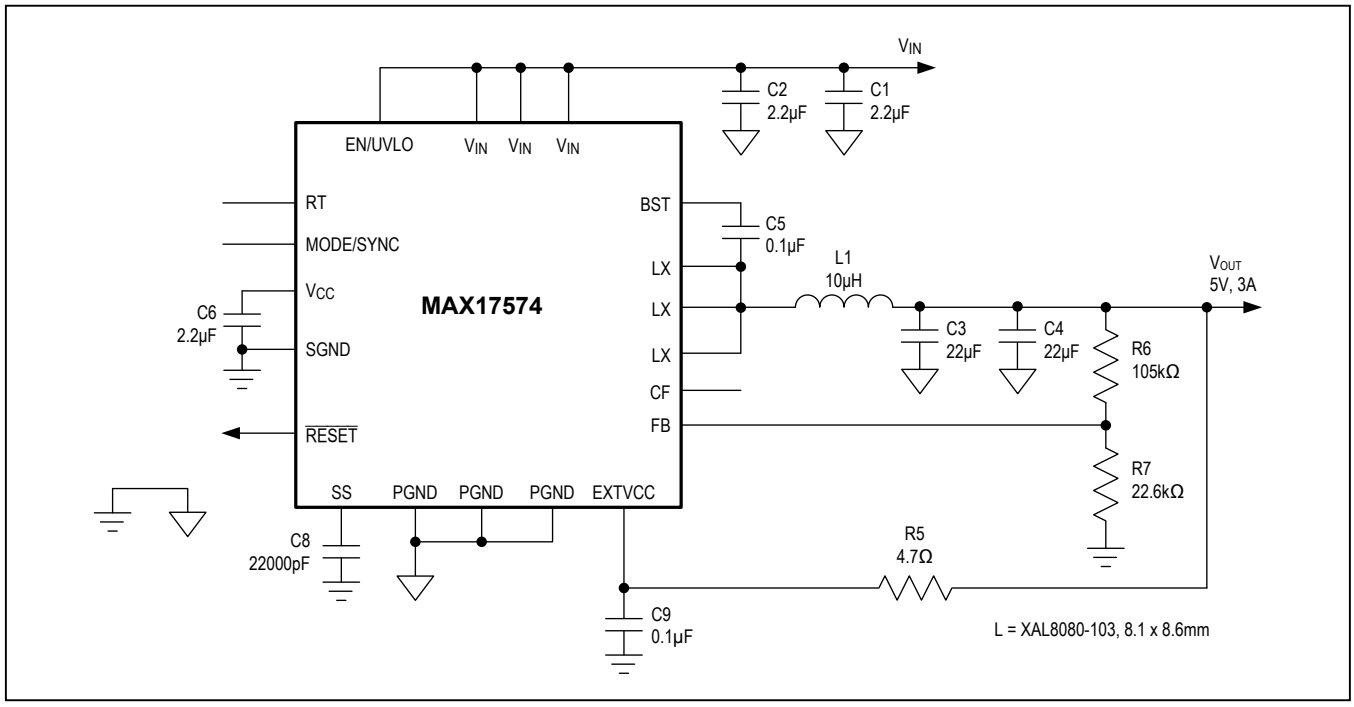
A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

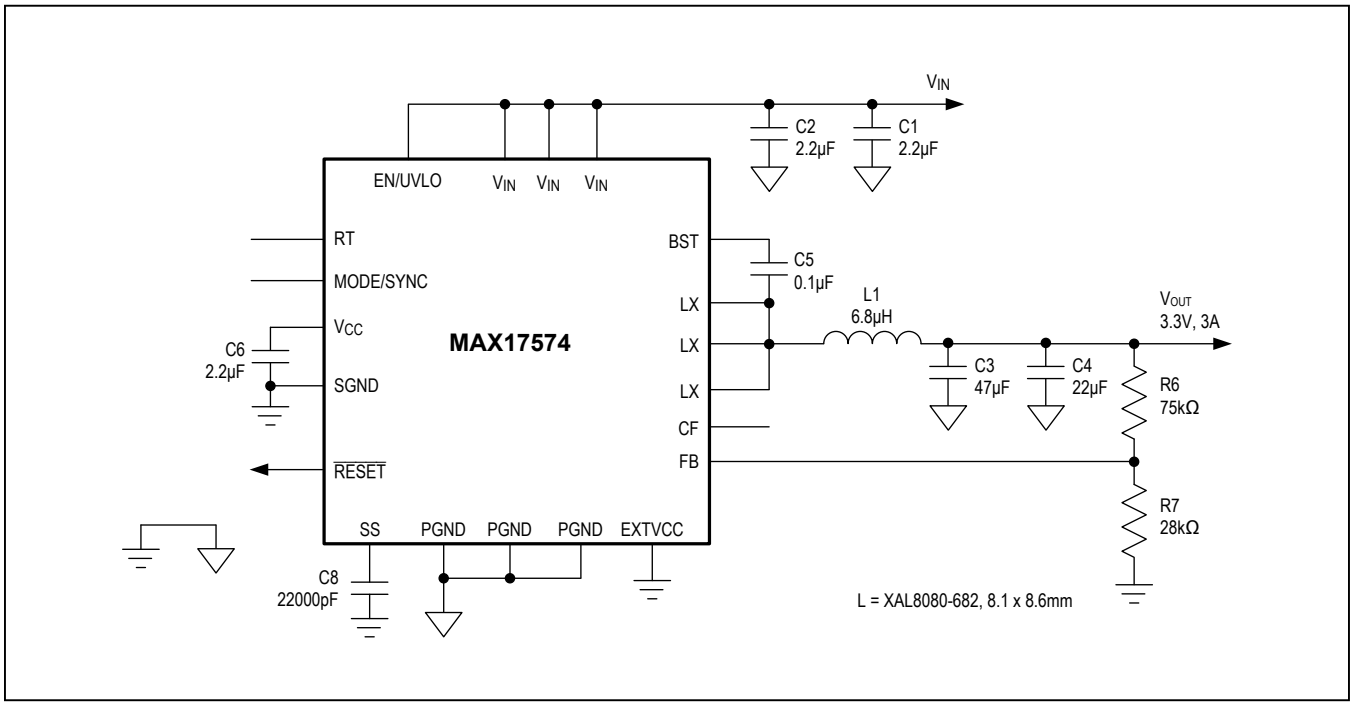
PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17574 evaluation kit layout available at **www.maximintegrated.com**.

Typical Application Circuit—5V Output Application Circuit



Typical Application Circuit—3.3V Output Application Circuit



Ordering Information

PART	PIN-PACKAGE	PACKAGE-SIZE
MAX17574ATG+	24-TQFN	4mm x 5mm

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP*	T2445+1C	21-0201	90-0083

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/16	Initial release	—