

DATA SHEET

SKY13431-374LF: 0.5 – 6.0 GHz SPDT Switch, 50 Ω Terminated

Applications

- Dual-band WLANs (802.11 a/b/g/n)
- WLAN 802.11a/c for video distribution
- LTE/4G systems
- WiMAX 802.16

Features

- 50 Ω matched RF ports in all states
- Low insertion loss: 0.5 dB @ 2.5 GHz
- High isolation: 25 dB @ 2.5 GHz
- IP1dB: +36 dBm
- Small, DFN (6-pin, 1.5 x 1.5 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



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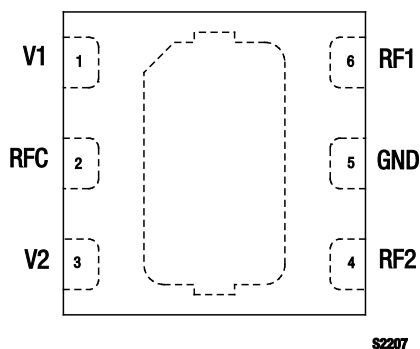


Figure 2. SKY13431-374LF Pinout – 6-Pin DFN (Top View)

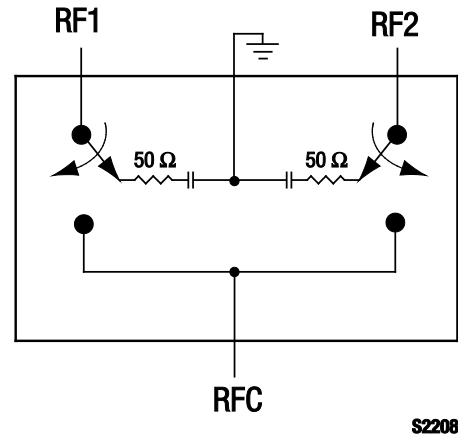


Figure 1. SKY13431-374LF Block Diagram

Description

The SKY13431-374LF is a GaAs pHEMT Single-Pole, Double-Throw (SPDT) high power switch with 50 Ω terminated outputs. The high linearity performance and low insertion loss achieved by the SKY13431-374LF make it an ideal choice for WiMAX and higher power WLAN applications such as access points.

This part is designed for use in WLAN systems using discrete Power Amplifier (PA) and Low-Noise Amplifier (LNA) implementations. The 50 Ω impedance of the switch in the “off” state ensures good isolation regardless of the match to which the switch is connected.

The SKY13431-374LF is manufactured in a compact, 1.5 x 1.5 mm, 6-pin Dual Flat No-Lead (DFN) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKY13431-374LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	V1	DC control voltage. A logic high voltage enables an insertion loss path between the RFC and RF1 pins.	4	RF2	RF output: 50 Ω terminated when in isolation state. Must be DC blocked.
2	RFC	RF common input. Must be DC blocked.	5	GND	Ground
3	V2	DC control voltage. A logic high voltage enables an insertion loss path between the RFC and RF2 pins.	6	RF1	RF output: 50 Ω terminated when in isolation state. Must be DC blocked.

Table 2. SKY13431-374LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Control voltage	V _{CTL}		6	V
Input power	P _{IN}		+37	dBm
Storage temperature	T _{STG}	-40	+125	°C
Operating temperature	T _{OP}	-40	+85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

Functional Description

Switching is controlled by two control voltage inputs, V1 and V2 (pins 1 and 3, respectively). Depending on the logic voltage level applied to the control pins, the RFC pin is connected to one of the two switched RF outputs, RF1 or RF2, using a low insertion loss path, while the path between the RFC pin and the other RF pin is in a high isolation state.

DC blocking capacitors are required on all RF ports of the switch. The value of the capacitors determines the low frequency operation. The isolated RF output is internally terminated to 50 Ω. The return loss of the isolated port is limited in frequency by on-chip capacitors.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13431-374LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY13431-374LF are illustrated in Figures 3 through 6.

The state of the SKY13431-374LF is determined by the logic provided in Table 4.

Table 3. SKY13431-374LF Electrical Specifications (Note 1)

($V_{CTL} = 0\text{ V}$ and $+3.0\text{ V}$, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\text{ }\Omega$, $C_{BLK} = 47\text{ pF}$, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss	IL	RFC to RF1 or RF2:				
		0.50 to 2.70 GHz		0.50	0.80	dB
		2.70 to 3.80 GHz		0.60	0.95	dB
		3.80 to 5.85 GHz		0.80	1.30	dB
Isolation	Iso	RFC to RF1 or RF2:				
		0.50 to 2.70 GHz	23	25	29	dB
		2.70 to 3.80 GHz	20	23		dB
		3.80 to 5.85 GHz	17	20		dB
Input return loss ("on" state)	IS11I	RFC or RF1 or RF2, 0.5 to 6.0 GHz		17.5		dB
Output return loss ("off" state)	IS22I	Isolated output RF1 or RF2:				
		2.30 to 2.70 GHz		11		dB
		2.70 to 3.80 GHz		11		dB
		3.80 to 5.85 GHz		11		dB
1 dB Input Compression Point	IP1dB	$V_{CTL} = 3.0\text{ V}$:				
		2.30 to 2.70 GHz		+36		dBm
		3.30 to 3.80 GHz		+36		dBm
		4.90 to 5.85 GHz		+36		dBm
3 rd Order Input Intercept Point	IIP3	$P_{IN} = +25\text{ dBm/ tone}$, $\Delta F = 1\text{ MHz}$, $V_{CTL} = 3.0\text{ V}$:				
		2.4 GHz		58		dB
		3.8 GHz		58		dB
		5.8 GHz		57		dB
2 nd harmonic	2fo	$P_{IN} = +25\text{ dBm}$, $V_{CTL} = 3.0\text{ V}$:				
		0.9 GHz		78		dBc
		1.8 GHz		78		dBc
		2.4 GHz		81		dBc
		3.8 GHz		82		dBc
		5.8 GHz		75		dBc
3 rd harmonic	3fo	$P_{IN} = +25\text{ dBm}$, $V_{CTL} = 3.0\text{ V}$:				
		0.9 GHz		76		dBc
		1.8 GHz		76		dBc
		2.4 GHz		72		dBc
		3.8 GHz		68		dBc
		5.8 GHz		75		dBc
Switching speed		50% V_{CTL} to 90/10% RF		100	250	ns
DC Specifications						
Control voltage	V_{CTL}		2.5	3.0	5.0	V
Control current	I_{CC}			5		μA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

($V_{CTL} = 0\text{ V}$ and $+3.0\text{ V}$, $T_{OP} = +25\text{ }^{\circ}\text{C}$, $P_{IN} = 0\text{ dBm}$, Characteristic Impedance [Z_0] = $50\ \Omega$, $C_{BLK} = 47\text{ pF}$, Unless Otherwise Noted)

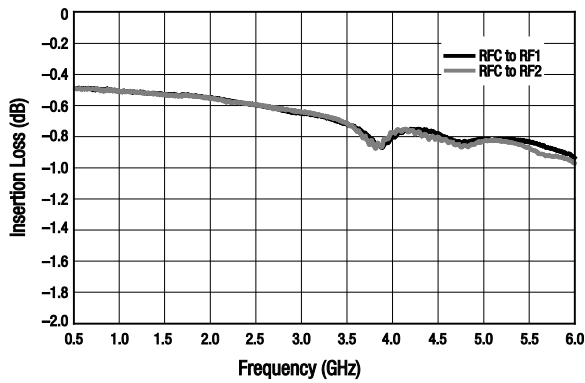


Figure 3. Typical Insertion Loss vs Frequency

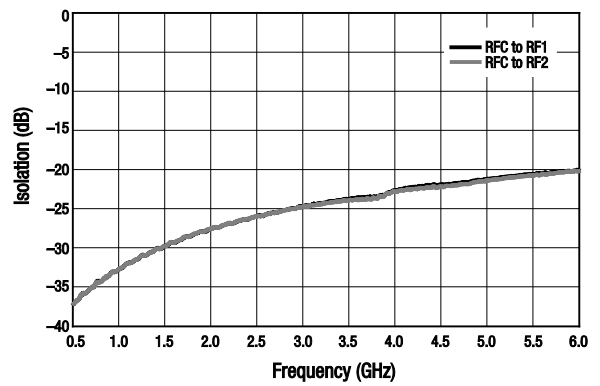


Figure 4. Typical Isolation vs Frequency

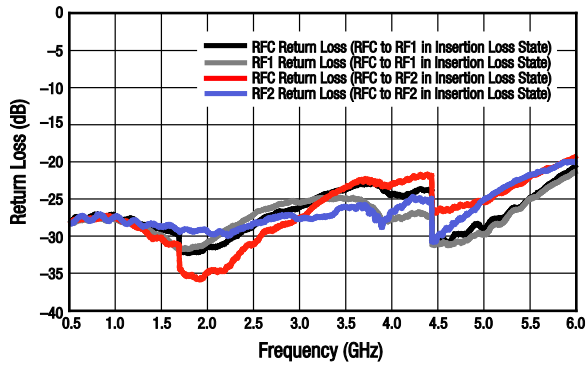


Figure 5. Return Loss vs Frequency (Insertion Loss State)

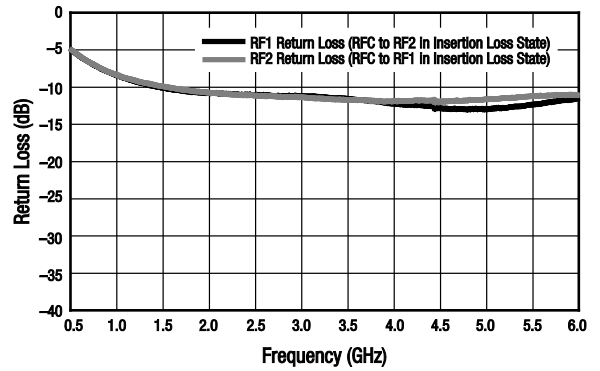


Figure 6. Return Loss vs Frequency (Isolation State)

Table 4. SKY13431-374LF Truth Table

V1 (Pin 1)	V2 (Pin 3)	Insertion Loss State
1	0	RFC to RF1
0	1	RFC to RF2

Note: "1" = +2.5 V to +5.0 V. "0" = 0 V to +0.2 V. Any state other than described in this Table places the switch into an undefined state. An undefined state will not damage the device.

Evaluation Board Description

The SKY13431-374LF Evaluation Board is used to test the performance of the SKY13431-374LF SPDT Switch. An Evaluation Board schematic diagram is provided in Figure 7. An assembly Board schematic diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

Package Dimensions

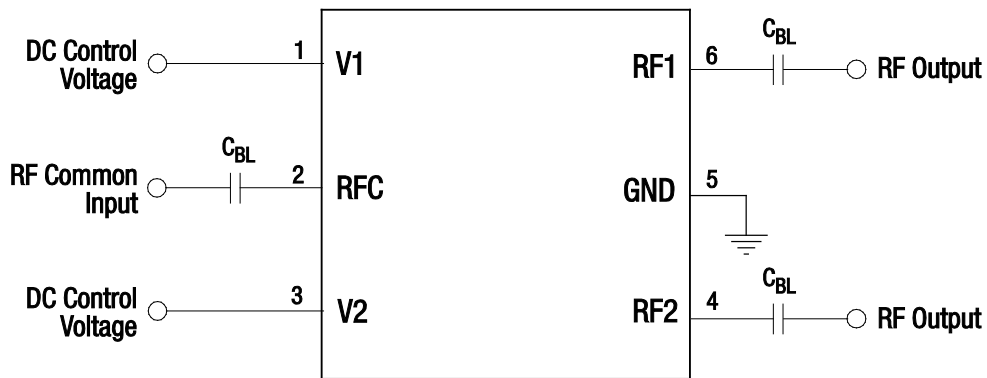
The PCB layout footprint for the SKY13431-374LF is provided in Figure 9. Typical case markings are shown in Figure 10. Package dimensions for the 6-pin DFN are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13431-374LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



C_{BL} = 47 pF for >1 GHz operation. Increase value for lower frequency operation.

Exposed ground paddle should be grounded for best performance.

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Figure 7. SKY13431-374LF Evaluation Board Schematic

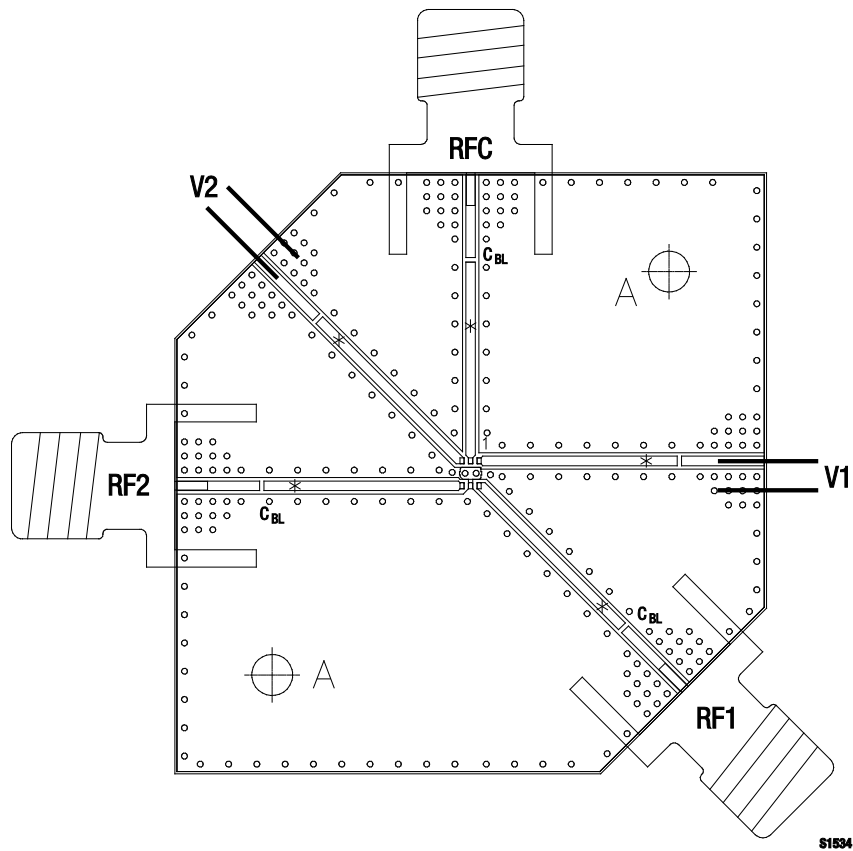


Figure 8. SKY13431-374LF Evaluation Board Assembly Diagram

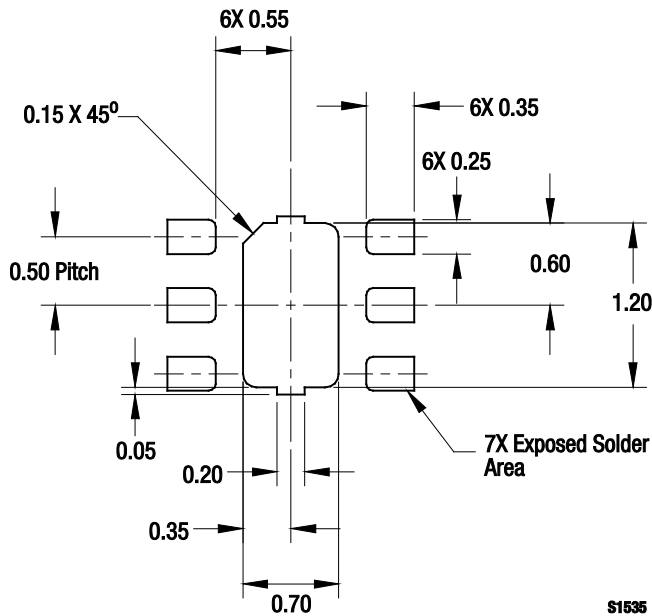


Figure 9. SKY13431-374LF PCB Layout Footprint (Top View)

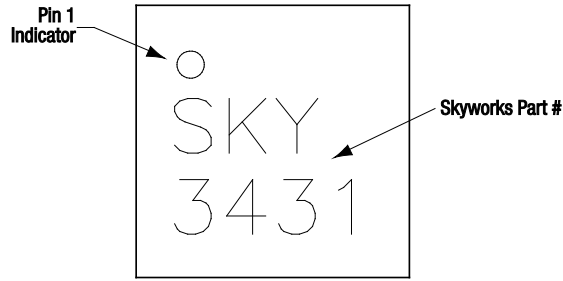
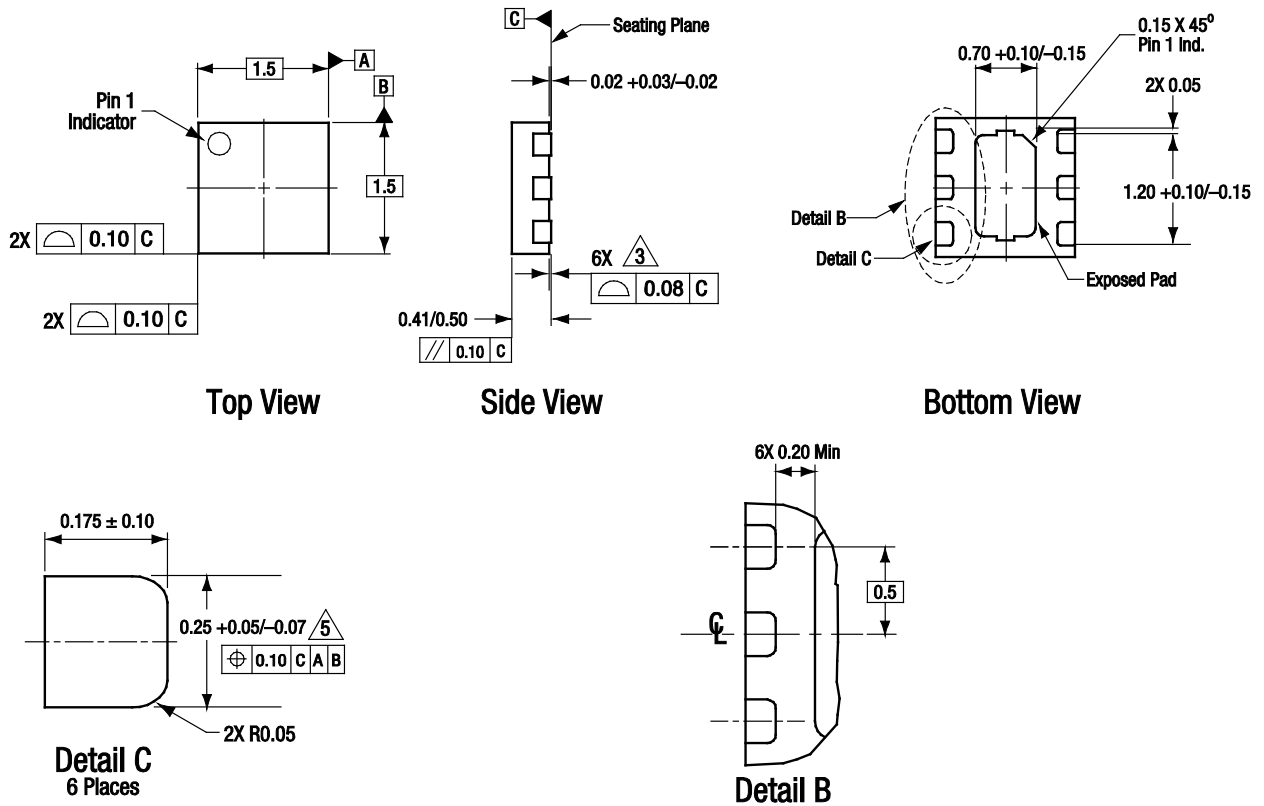


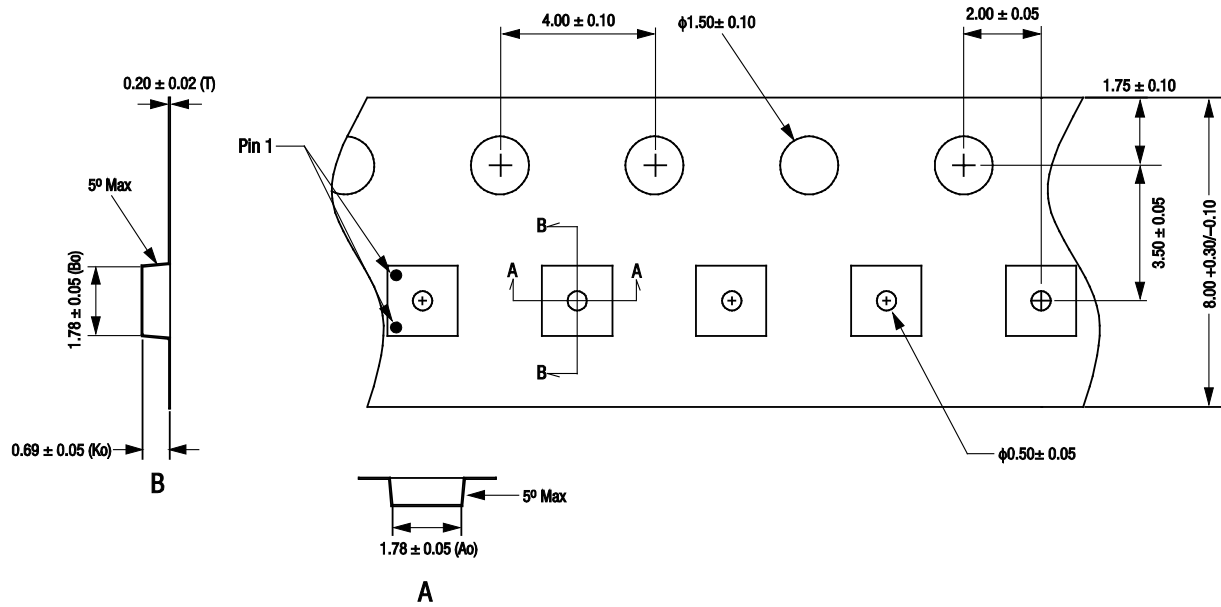
Figure 10. Typical Part Markings (Top View)



All measurements are in millimeters.
 Dimensioning and tolerancing according to ASME Y14.5M-1994.
 Coplanarity applies to the exposed heat sink slug as well as the terminals.
 Plating requirement per source control drawing (SCD) 2504.
 Dimension applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
 Metalized contact areas are NiPdAu.

S1536

Figure 11. SKY13431-374LF 6-Pin DFN Package Dimensions



Notes:

1. Carrier tape: black conductive polycarbonate.
2. Cover tape material: transparent conductive PSA.
3. Cover tape size: 5.4 mm width.
4. All measurements are in millimeters.
5. ESD surface resistivity is $\leq 1 \times 10^8$ Ohms/square per EIA, JEDEC tape and reel specification.
6. Pin 1 orientation is in lower left corner for SOT-666 packages.
Pin 1 orientation is in upper left corner for 1.5 x 1.5 mm MLPD, QFN, and DFN packages.

S1382

Figure 12. SKY13431-374LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13431-374LF SPDT Switch	SKY13431-374LF	SKY13431-374LF-EVB

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