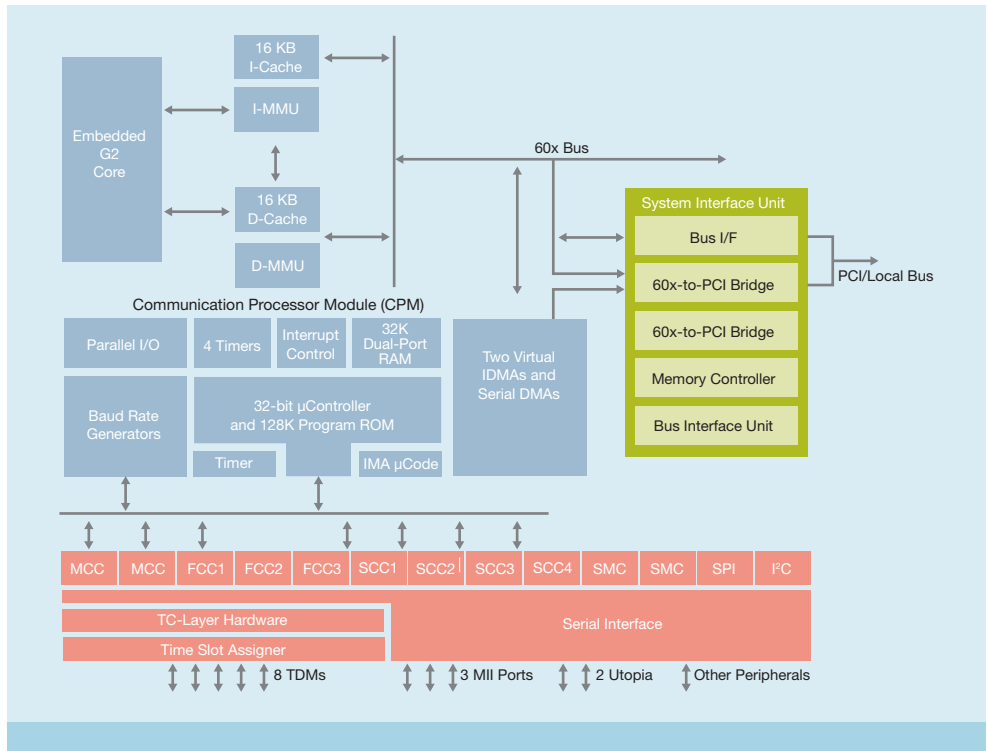


# MPC8260 PowerQUICC™ II Processor Family

The PowerQUICC™ II family of integrated communications processors delivers excellent integration of processing power for networking and communications peripherals, providing customers with an innovative, total system solution for building high-end communications systems. Freescale's PowerQUICC II processor family, built on the Power Architecture™ technology, offers high performance in all areas of device operation, including exceptional flexibility, extensive capabilities and a high level of integration.

Freescale's MPC8260 PowerQUICC II processor integrates two processing blocks: a high-performance embedded G2 core and a Communications Processor Module (CPM). The CPM is designed to support up to three fast serial communications controllers (FCCs), two multi-channel controllers (MCCs), four serial communications controllers (SCCs), two serial management controllers (SMCs), one serial peripheral interface (SPI) and one I<sup>2</sup>C interface. The combination of the G2 core and the CPM, along with the versatility and performance of the PowerQUICC II processor family, provides customers with enormous potential in developing networking and communications products while significantly reducing time to market development stages.

MPC8260 Block Diagram



## Product Highlights

- 300 MHz high-speed embedded G2 core
- Powerful memory controller and system functions
- Enhanced 32-bit RISC CPM
- Up to three multi-port 10/100 Mbps Ethernet MACs
- Up to two UTOPIA ports supporting 155 Mbps ATM
- Up to 256 HDLC channels (each channel 64 kbps, full duplex)
- Up to four 10 Mbps Ethernet MACs
- Transmission convergence sub-layer and inverse multiplexing for ATM capabilities
- Integrated PCI interface
- Strong third-party tools support from Freescale's Design Alliance members

## Typical Applications

- Remote access concentrators
- Regional office routers
- Cellular infrastructure equipment
- Telecom switching equipment
- Ethernet switches
- T1/E1-to-T3/E3 bridges
- LAN-to-WAN bridges/routers
- xDSL systems

**MPC**

Product Code  
 KXPC Sample Pack (2-10)  
 XPC Engineering Production  
 MPC Fully Qualified

**8260**

8260 Series Device Number  
 (8250, 8255, 8260, 8264, 8265, 8266)

**A**

A=0.25 micron (HIP4)  
 Otherwise, no designation  
 here = 0.29 micron (HIP3)

**C**

Temp. Range  
 None 0°C to +105°C  
 C -40°C to +105°C

**ZU**

Package  
 ZU-TBGA  
 VV-TBGA Pb-Free  
 ZQ-PBGA  
 VR-PBGA Pb-Free

**IFB**

CPU/CPM/Bus Speed  
 A=50 I=200  
 B=66 J=208  
 C=75 K=233  
 D=83 L=250  
 E=100 M=266  
 F=133 N=291  
 G=150 P=300  
 H=166 Q=333

**B**

Die Mask Revision

## PowerQUICC II family

	8250	8255	8260	8264	8265	8266
Serial Communications Controllers (SCCs)	4	4	4	4	4	4
Fast Serial Communications Controllers (FCCs)	3	2	3	3	3	3
I-Cache (KB)	16	16	16	16	16	16
D-Cache (KB)	16	16	16	16	16	16
Ethernet (10/100)	Up to 3	Up to 2	Up to 3	Up to 3	Up to 3	Up to 3
UTOPIA II Ports (ATM)	-	2	2	2	2	2
Multi-Channel HDLC	Up to 128	Up to 128	Up to 256	Up to 256	Up to 256	Up to 256
PCI Interface	Yes	-	-	-	Yes	Yes
IMA Functionality	-	-	-	Yes	-	Yes
Dual-Port RAM	32K	32K	32K*	32K	32K	32K

\*8260A, 8255A

## Technical Specifications

- Embedded G2 core available up to 300 MHz
  - 570 MIPS at 300 MHz (Dhrystone 2.1)
  - High-performance, superscalar microprocessor
  - Disable-CPU mode
  - Support for the Freescale external L2 cache chip (MPC2605)
  - Improved low-power core
  - 16 KB data and 16 KB instruction cache
  - Memory management unit (MMU)
  - Floating point unit
  - Common on-chip processor (COP)
- System interface unit (SIU)
  - Memory controller, including two dedicated SDRAM machines
- PCI up to 66 MHz (8250, 8265, 8266 versions)
- Hardware bus monitor and software watchdog timer
- IEEE® 1149.1 JTAG test access port
- High-performance CPM
  - G2 core and CPM may run at different frequencies
  - Parallel I/O registers
  - On-board 32 KB of dual-port RAM
  - Two MCCs, each supporting 128 full-duplex, 64 kbps, HDLC lines
  - Virtual DMA functionality
- Three FCCs supporting:
  - Up to 155 Mbps ATM SAR, maximum of two (AAL0, AAL1, AAL2, AAL5)
  - 10/100 Mbps Ethernet, up to three (IEEE 802.3X with flow control)
- 45 Mbps HDLC/transparent (up to three)
- Two UTOPIA Level II master/slave ports with multi-PHY support
- Three MII interfaces
- Eight TDM interfaces (T1/E1), two TDM ports that can be interfaced with T3/E3
- Transmission convergence layer capabilities
- Inverse multiplexing for ATM (IMA) functionality
- Two-bus architecture: one 64-bit 60x bus and one 32-bit PCI or local bus
  - Integrated PCI interface
- 1.8V or 2.0V internal and 2.5V I/O
- 480 TBGA package (37.5 x 37.5 mm)
- 516 PBGA package (27 x 27 mm) (8250 only)

## Learn More:

For current information about Freescale products and documentation, please visit [www.freescale.com](http://www.freescale.com).



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