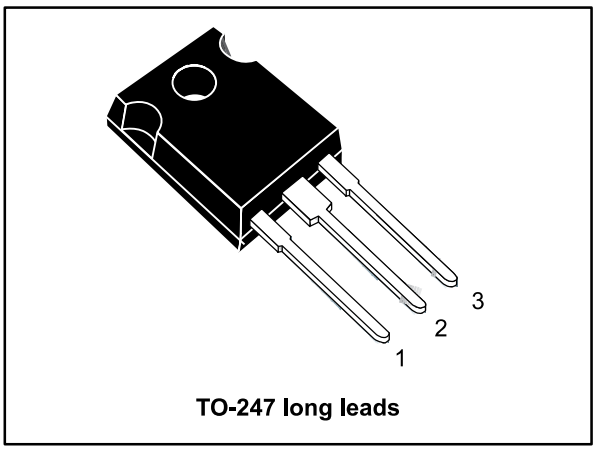
STWA40N95K5

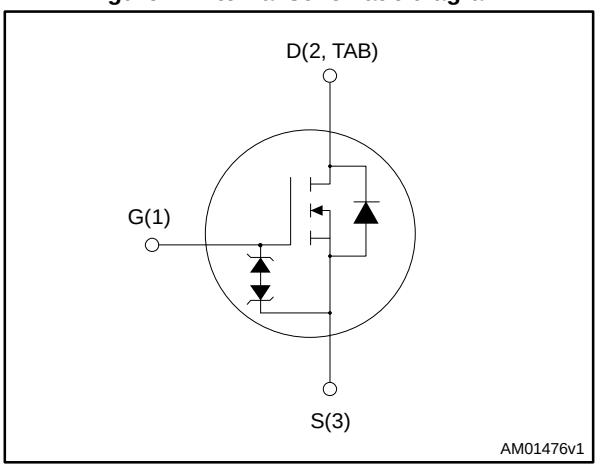
N-channel 950 V, 0.110 Ω typ., 38 A MDmesh™ K5 Power MOSFET in a TO-247 long leads package

Datasheet - production data



TO-247 long leads

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STWA40N95K5	950 V	0.130 Ω	38 A	450 W

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STWA40N95K5	40N95K5	TO-247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	38	A
I_D	Drain current (continuous) at T_C = 100 °C	24	A
I_{DM} (1)	Drain current (pulsed)	152	A
P_{TOT}	Total dissipation at T_C = 25 °C	450	W
I_{AR}	Max current during repetitive or single pulse avalanche	13	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D= 13 A, V_{DD}= 50 V)	700	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 19 A, di/dt ≤ 100 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$.

(3)V_{DS} ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.28	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	50	°C/W

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	950			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 950 V			1	µA
		V_{GS} = 0, V_{DS} = 950 V, T_C=125 °C			50	µA
I_{GSS}	Gate-body leakage current	V_{DS}=0, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 19 A		0.110	0.130	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS}=0, V_{DS} =100 V, f=1 MHz	-	3300	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 760 V	-	398	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	142	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 38 A V_{GS} =10 V (see *Figure 16: "Gate charge test circuit"*)	-	93	-	nC
Q_{gs}	Gate-source charge		-	18.7	-	nC
Q_{gd}	Gate-drain charge		-	63.4	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 19 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15: "Switching times test circuit for resistive load"*)	-	33.5	-	ns
t_r	Rise time		-	51	-	ns
$t_{d(off)}$	Turn-off-delay time		-	91.5	-	ns
t_f	Fall time		-	10	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		38	A
I_{SDM} (1)	Source-drain current (pulsed)		-		152	A
V_{SD} (2)	Forward on voltage	I_{SD} = 38 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 38 A, di/dt = 100 A/µs V_{DD}= 60 V (see *Figure 18: "Unclamped inductive load test circuit"*)	-	706		ns
Q_{rr}	Reverse recovery charge		-	22		µC
I_{RRM}	Reverse recovery current		-	62		A
t_{rr}	Reverse recovery time	I_{SD} = 38 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C (see *Figure 18: "Unclamped inductive load test circuit"*)	-	886		ns
Q_{rr}	Reverse recovery charge		-	28.2		µC
I_{RRM}	Reverse recovery current		-	64		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

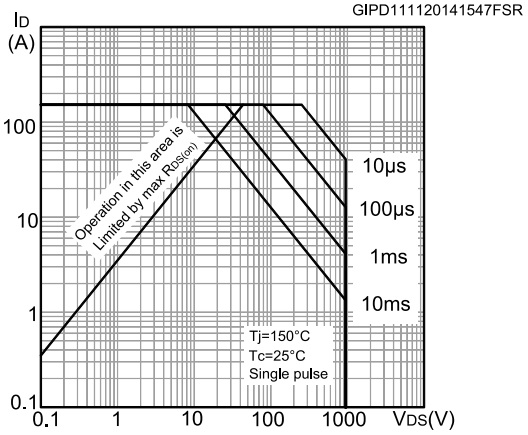


Figure 3: Thermal impedance

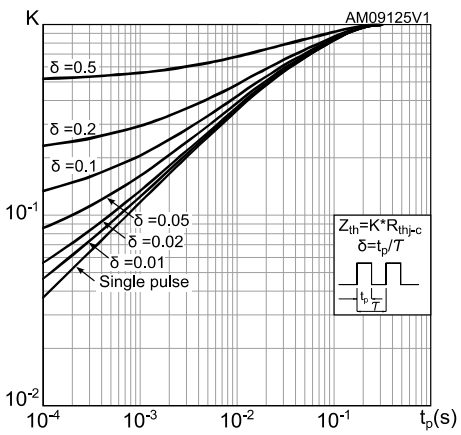


Figure 4: Output characteristics

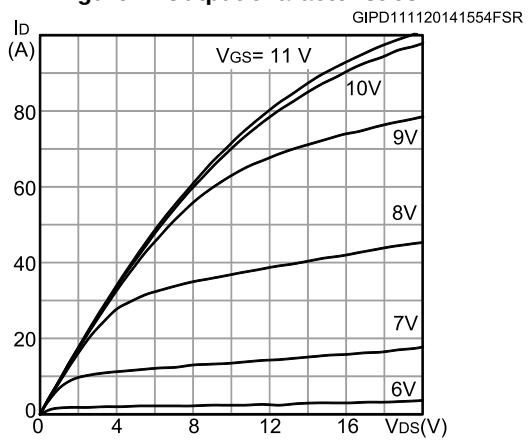


Figure 5: Transfer characteristics

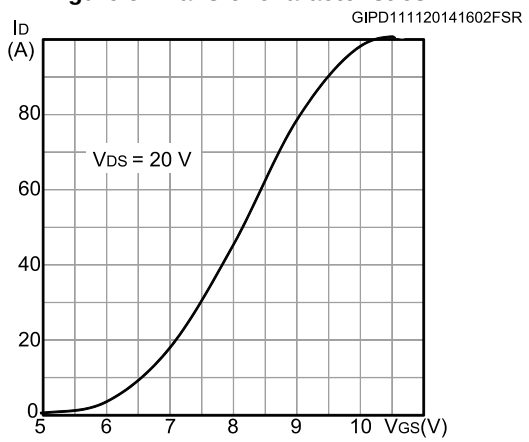


Figure 6: Gate charge vs gate-source voltage

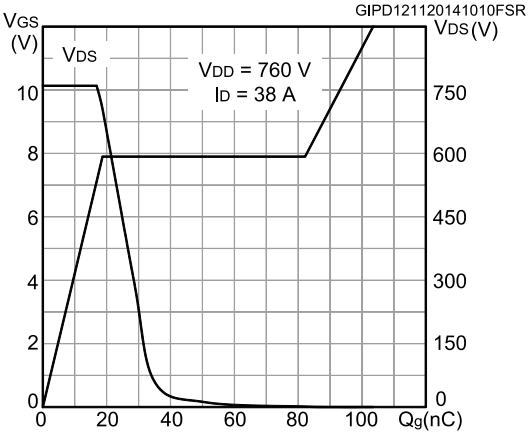


Figure 7: Static drain-source on-resistance

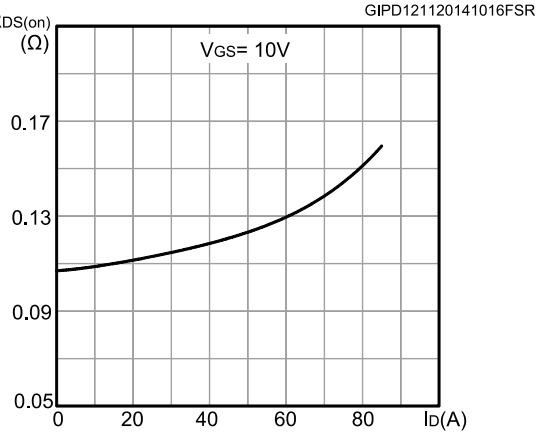


Figure 8: Capacitance variations

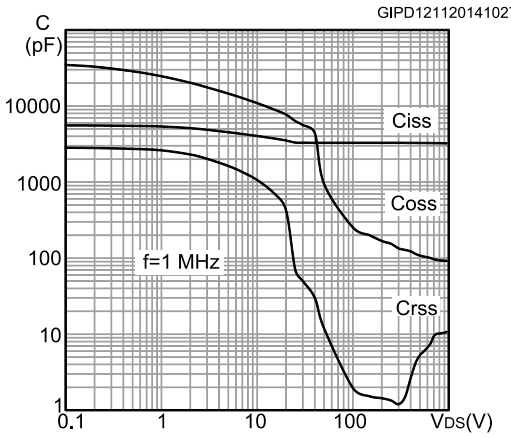


Figure 9: Normalized gate threshold voltage vs temperature

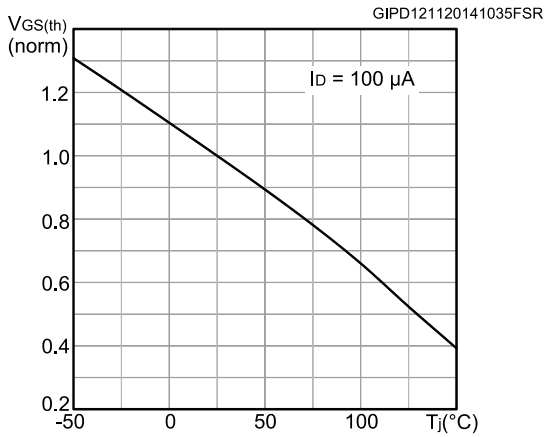


Figure 10: Normalized on-resistance

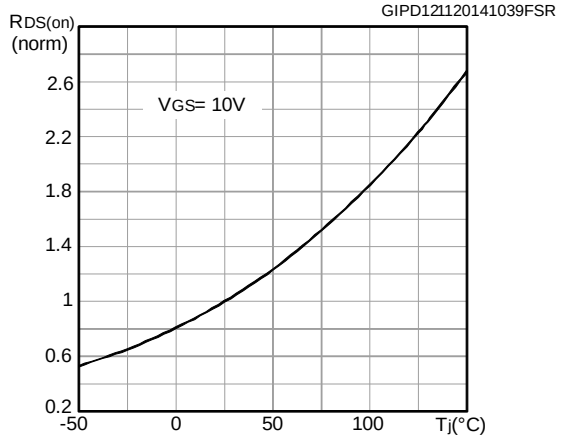


Figure 11: Normalized V(BR)DSS vs temperature

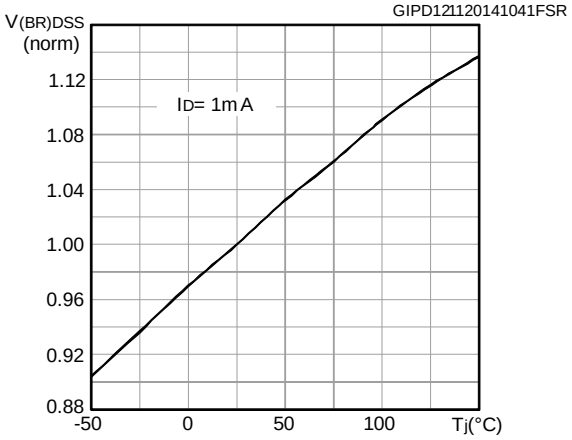


Figure 12: Output capacitance stored energy

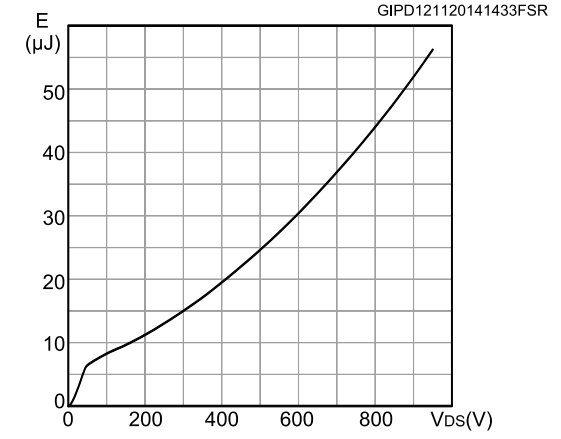


Figure 13: Source-drain diode forward characteristics

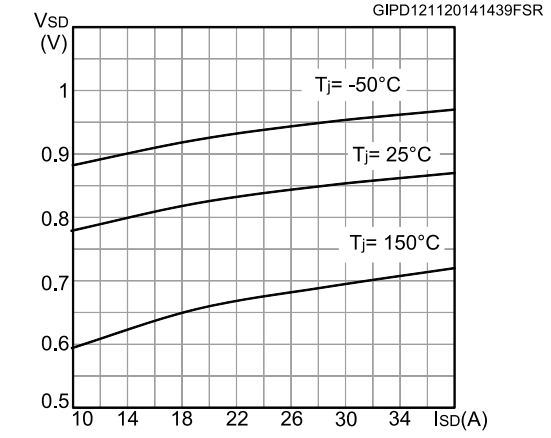
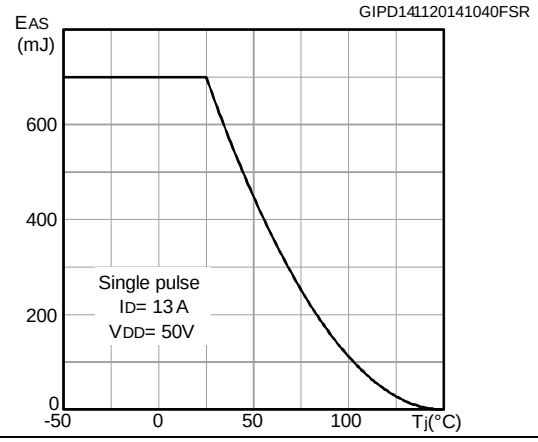


Figure 14: Maximum avalanche energy vs T J



3 Test circuits

Figure 15: Switching times test circuit for resistive load

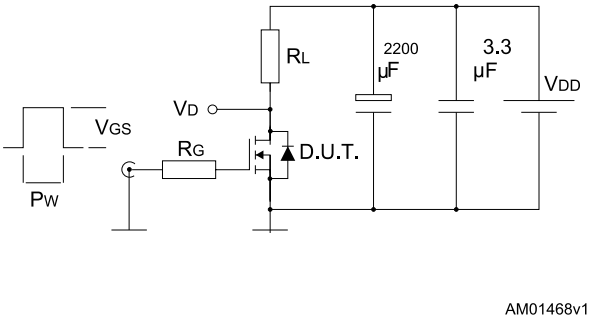


Figure 16: Gate charge test circuit

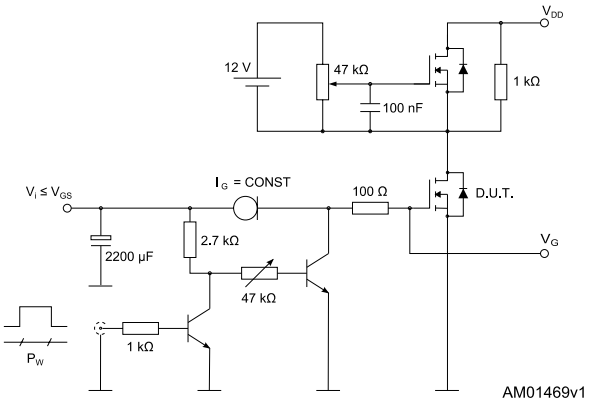


Figure 17: Test circuit for inductive load switching and diode recovery times

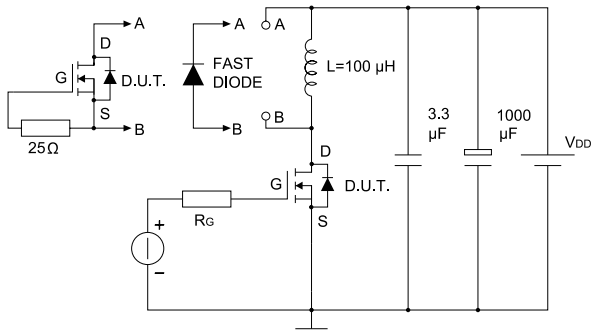


Figure 18: Unclamped inductive load test circuit

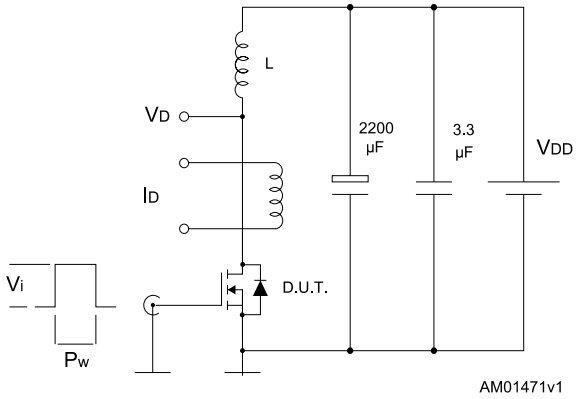


Figure 19: Unclamped inductive waveform

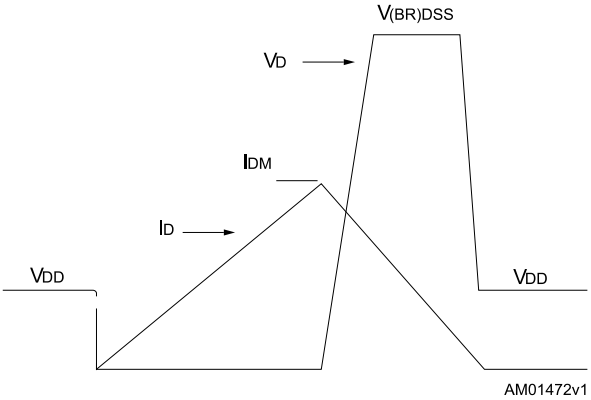
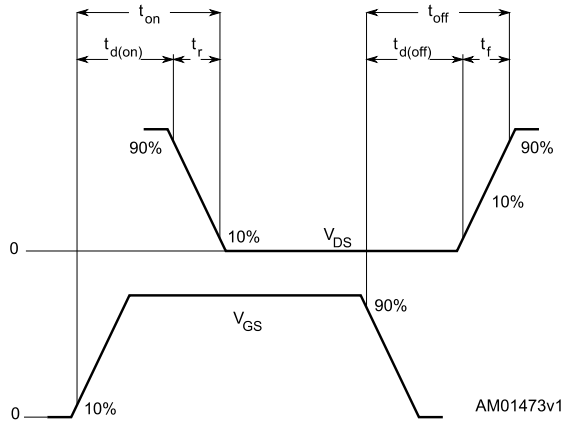


Figure 20: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 21: TO-247 long leads package outline

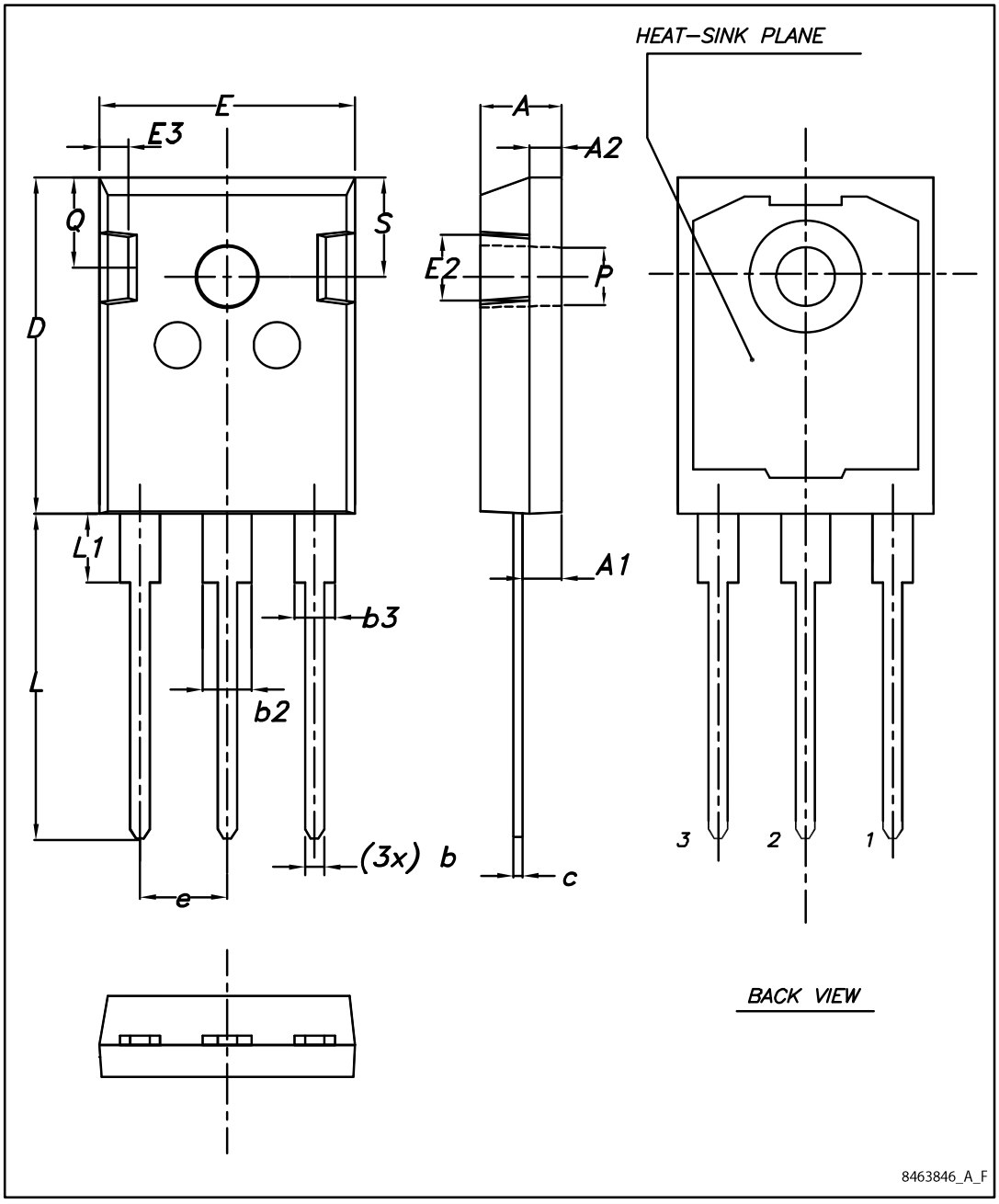


Table 9: TO-247 long leads package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
05-Aug-2015	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.