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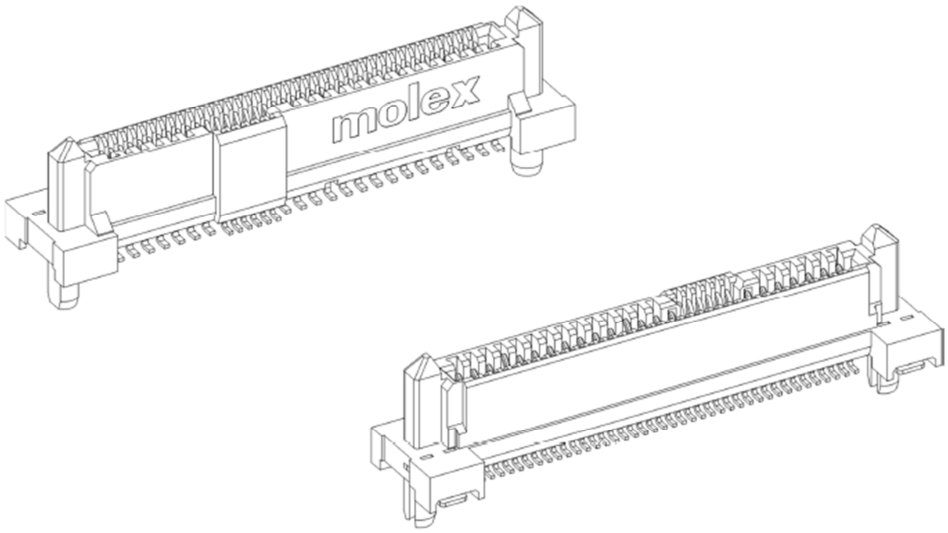
1.0 SCOPE

This board layout and routing guidelines cover the printed circuit board layout that can be used for the evaluation of high-speed signals using microstrip routing for 78757 series connector.

Disclaimer: Molex does not guarantee the performance of the final product to the information provided in this document. All information in this report is considered Molex proprietary and confidential. This guide is not intended as a substitute for engineering analysis where optimization for signal integrity (SI) performance can be critical.



2.0 PC BOARD REQUIREMENTS

2.1 MATERIAL THICKNESS

The recommended PC board thickness shall be 1.60mm. Suitable PC board material shall be glass epoxy (FR-4).

2.2 LAYOUT

The solder pads for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Refer to the applicable Sales Drawing for the recommended solder pad pattern, dimensions and tolerances.

3.0 HIGH SPEED ROUTING

3.1 TRACE TO PAD ATTACHMENT

There are several ways to connect the traces to their corresponding signal pads. Two possible methods are illustrated in Figures 1 and 2.

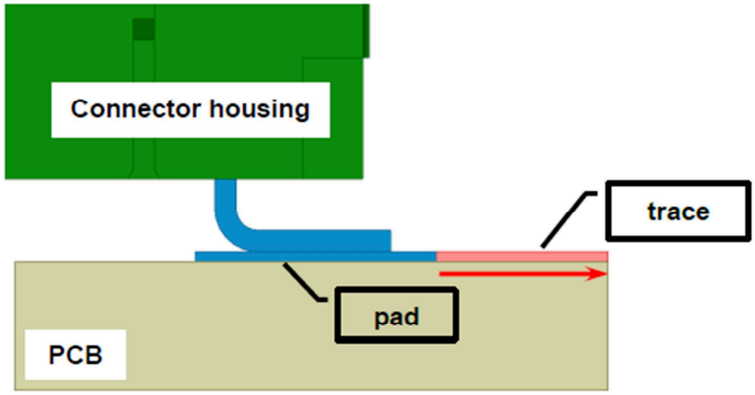


Figure 1

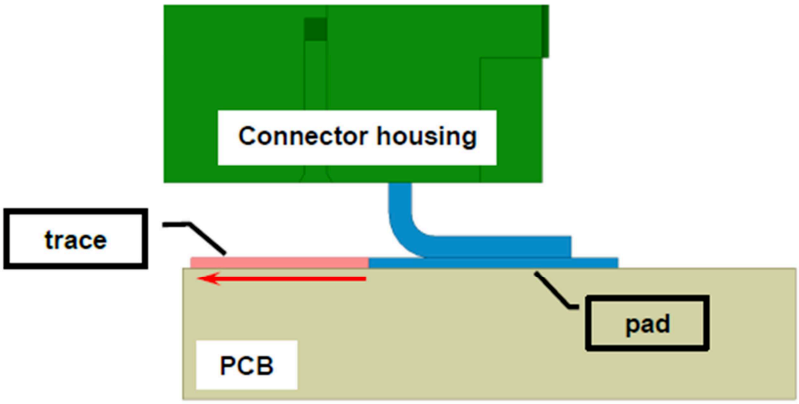


Figure 2

As seen in Figure 1, trace routed outwards from pad of connector will result in minimum pad stub while worst case pad stub occurs when trace is routed inwards as shown in Figure 2.

3.2 GROUND VIA PLACEMENT

There are several ways to connect ground vias to their corresponding ground pads. Two possible methods are illustrated in Figures 3 and 4.

PCB Top View

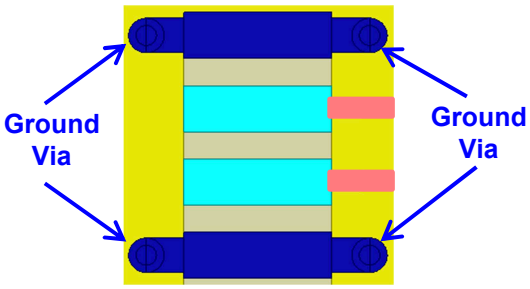


Figure 3

PCB Top View

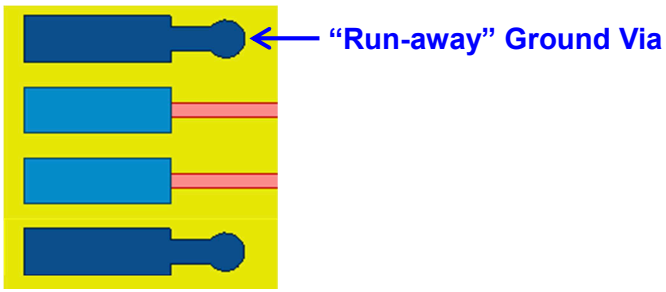


Figure 4

As seen in Figure 3, ground vias can be attached to both ends of ground pad for better signal return path. If this is not possible due to routing constrain, "run-away" ground vias from ground pads should follow the direction where the signal traces were attached to their corresponding signal pads as shown in Figure 4.

3.3 IMPEDANCE MATCHING AT TRACE AND FOOTPRINT/PAD

Impedance matching is critical to improve and optimize SI performance.

All traces and pad should design to the intended system impedance. For SAS application, it should be single-ended 50Ω or differential 100Ω. For PCI-Express application, it should be single-ended 42.5Ω or differential 85Ω.

This could be done by controlling distance between trace (H_{trace}) and pad (H_{pad}) with reference to their ground return. This is illustrated in Figure 5.

When the trace width of pad equals to trace, H_{trace} equals H_{pad}. If pad width is wider than trace, $H_{pad} > H_{trace}$. This is to eliminate excessive capacitive coupling at pad region.

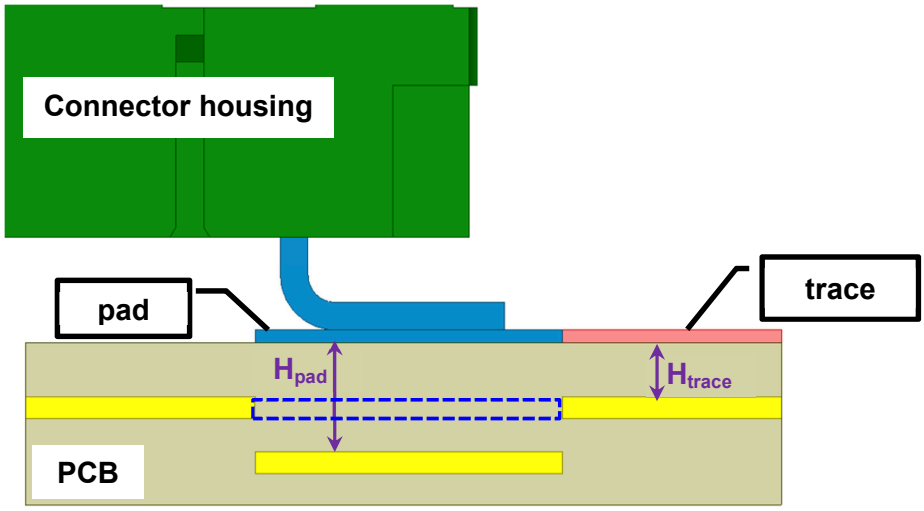


Figure 5

3.4 HIGH SPEED REFERENCE PLANE ANTI-PAD

An antipad or copper cutout region, shown in Figure 6, is needed to obtain desirable H_{pad} for impedance optimization. A table containing suggested values for a TX/RX lane are shown in Table 1.

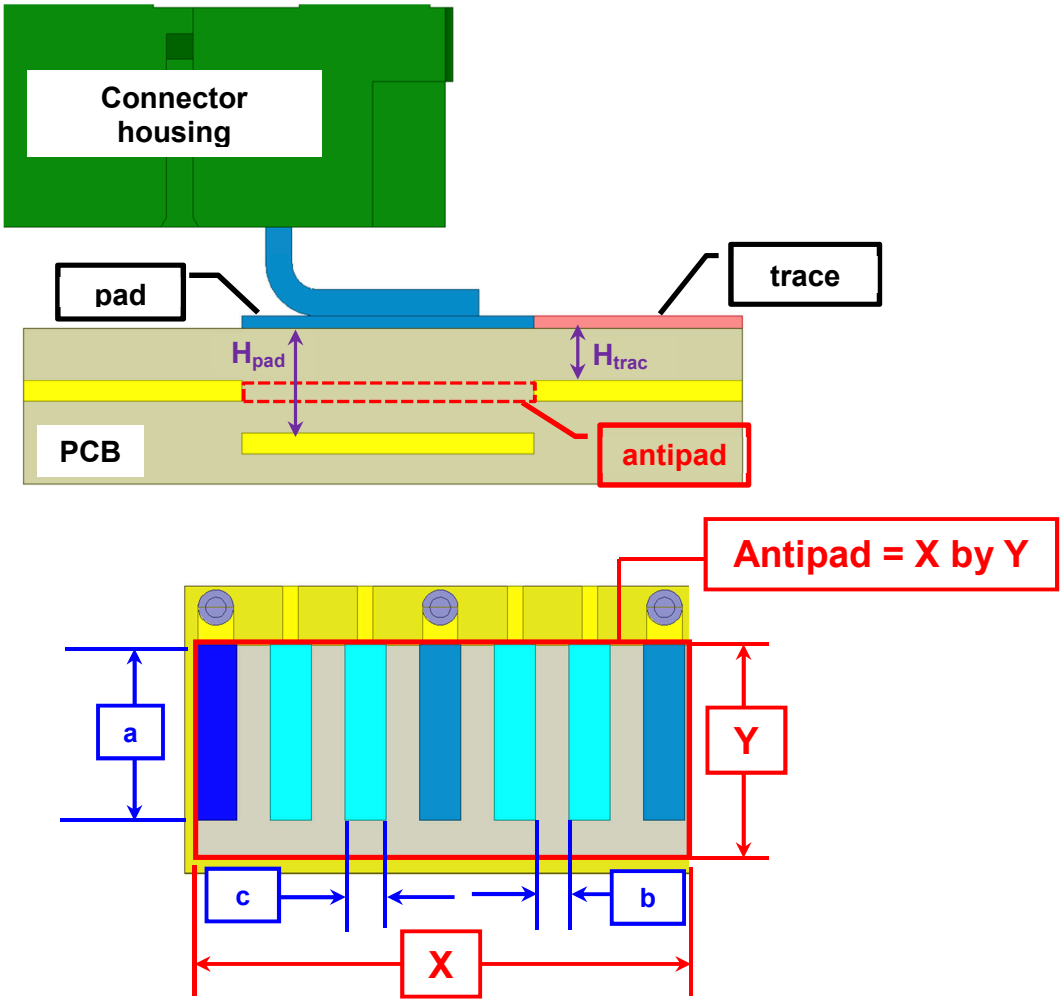


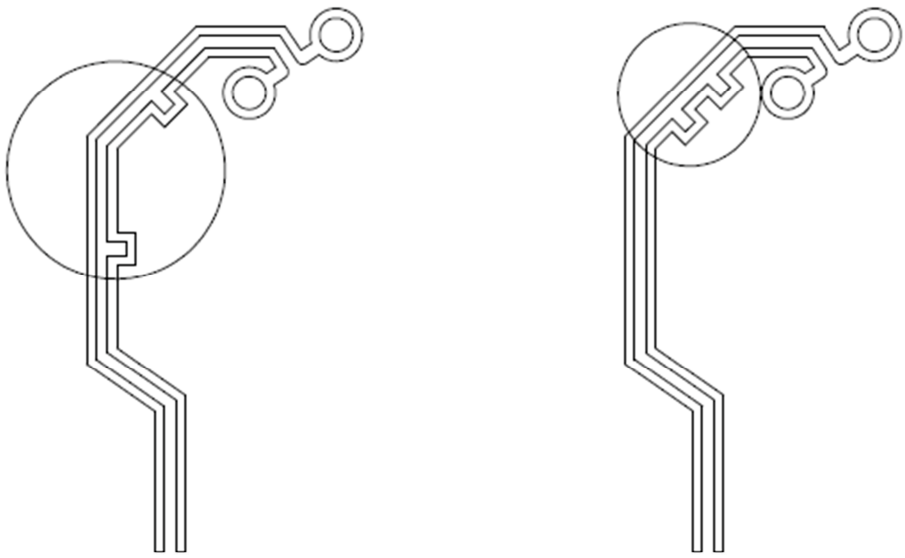
Figure 6 – Port Footprint

Antipad Dimension	**TX/RX Lane**
X	7c + 6b
Y	a + b

Table 1

Note: Anti-pad was implemented for impedance matching. Dimensions can vary from recommendation to meet electrical requirements. For example, the anti-pad can be made larger with a broader keep-out region on non-signal ground planes to minimize parasitic capacitance.

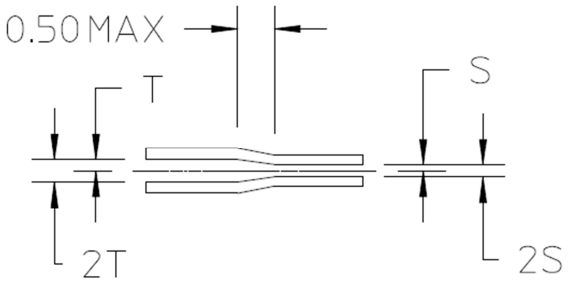
3.5 SKEW COMPENSATION FOR DIFFERENTIAL ROUTING



PREFERRED NOT RECOMMENDED

It is recommended that skew compensation be distributed verses grouped in one or more locations.

3.6 TRACE COMPARISON



TRANSITION SHOULD BE SYMMETRIC