# XA9500XL Automotive CPLD Product Family

DS108-1 (v1.7) April 3, 2007

**Product Specification**

## Features

- AEC-Q100 device qualification and full PPAP support available in both extended temperature Q-grade and I-grade.
- Guaranteed to meet full electrical specifications over $T_A$ = -40° C to +105° C with $T_J$ Maximum = +125° C (Q-grade)
- System frequency up to 64.5 MHz (15.5 ns)
- Available in small footprint packages
- Optimized for high-performance 3.3V systems
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals — ideal for multi-voltage system interfacing and level shifting
  - Technology: 0.35 µm CMOS process
- Advanced system features
  - In-system programmable enabling higher system reliability through reduced handling and reducing production programming times
  - Superior pin-locking and routability with FastCONNECT™ **II** switch matrix allowing for multiple design iterations without board re-spins
  - Input hysteresis on all user and boundary-scan pin inputs to reduce noise on input signals
  - Bus-hold circuitry on all user pin inputs which reduces cost associated with pull-up resistors and reduces bus loading
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) for in-system device testing
    - Fast concurrent programming
- Slew rate control on individual outputs for reducing EMI generation
- Refer to XC9500XL Family data sheet (DS054) for architecture description
- Refer to XA9536XL data sheet (DS598), the XA9572XL data sheet (DS599), and the XA95144XL data sheet (DS600) for pin tables
- Xilinx received ISO/TS 16949 Certification in March 2005.

WARNING: Programming temperature range of $T_A$ = 0° C to +70° C

## Description

The XA9500XL 3.3V CPLD Automotive XA product family is targeted for leading-edge, high-performance automotive applications that require either automotive industrial (–40°C to +85°C ambient) or extended (–40°C to +105°C ambient) temperature reconfigurable devices.

## Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. Each macrocell in an XA9500XL automotive device must be configured for low-power mode (default mode for XA9500XL devices). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of $I_{CC}$, the following equation may be used:

$I_{CC}(mA) = MC(0.052*PT + 0.272) + 0.04 * MC_{TOG}*MC* f$

where:

MC = # macrocells

PT = average number of product terms per macrocell

f = maximum clock frequency

$MC_{TOG}$ = average % of flip-flops toggling per clock (~12%)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual $I_{CC}$ value varies with the design application and should be verified during

*Table 1:* **XA9500XL Device Family**

| Device | Temperature Grade | Macrocells | Usable Gates | Registers | $f_{SYSTEM}$ (MHz) |
|---|---|---|---|---|---|
| XA9536XL | I, Q | 36 | 800 | 36 | 64.5 |
| XA9572XL | I, Q | 72 | 1,600 | 72 | 64.5 |
| XA95144XL | I | 144 | 3,200 | 144 | 64.5 |

*Table 2:* **XA9500XL Packages and User I/O Pins (not including four dedicated JTAG pins)**

| Device | VQG44 | VQG64 | TQG100 | CSG144 |
|---|---|---|---|---|
| XA9536XL | 34 | -- | -- | -- |
| XA9572XL | 34 | 52 | 72 | -- |
| XA95144XL | -- | -- | -- | 117 |

## Absolute Maximum Ratings(1,2)

| Symbol | Description | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND | –0.5 | 4.0 | V |
| $V_{IN}$ | Input voltage relative to GND(3) | –0.5 | 5.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output(3) | –0.5 | 5.5 | V |
| $T_{STG}$ | Storage temperature (ambient)(4) | –65 | +150 | ºC |
| $T_J$ | Junction temperature | - | +125 | ºC |

**Notes:**
1. All automotive customers are required to set the Macrocell Power Setting to low, and set Logic Optimization to density.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
4. For soldering guidelines, see the Package Information on the Xilinx website.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $T_A$ | Ambient temperature | I-Grade | –40 | +85 | °C |
| | | Q-Grade | –40 | +105 | °C |
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | | 3.0 | 3.6 | V |
| $V_{CCIO}$ | Supply voltage for output drivers for 3.3V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers for 2.5V operation | | 2.3 | 2.7 | V |
| $V_{IL}$ | Low-level input voltage | | 0 | 0.80 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |

## Quality and Reliability Characteristics

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{DR}$ | Data Retention | 20 | - | Years |
| $N_{PE}$ | Program/erase cycles (Endurance) @ $T_A$ = 70°C | 10,000 | - | Cycles |

## Component Availability

| Pins | | 44 | 64 | 100 | 144 |
|---|---|---|---|---|---|
| Type | | Quad Flat Pack | Quad Flat Pack | Thin Quad Flat Pack | Chip Scale Package |
| Code | | VQG44 | VQG64 | TQG100 | CSG144 |
| **XA9536XL** | -15 | I,Q | -- | -- | -- |
| **XA9572XL** | -15 | I,Q | I,Q | I,Q | -- |
| **XA95144XL** | -15 | -- | -- | -- | I |

**Notes:**
1. Q = Automotive Extended Temperature ($T_A$ = –40°C to +105°C).
2. I = Automotive Industrial Temperature ($T_A$ = –40°C to +85°C).
3. All packages Pb-free.

## Ordering Information

**Example:** **XA9572XL -15 VQG 44Q**

- XA9572XL — Device Type
- -15 — Speed Grade
- VQG — Package Type
- 44 — Number of Pins
- Q — Temperature Range
- (blank) — Pb-free

### Device Ordering Options

| Device |
|---|
| XA9536XL |
| XA9572XL |
| XA95144XL |

| Speed | |
|---|---|
| -15 | 15.5 ns pin-to-pin delay |

| Package | |
|---|---|
| VQG44 | 44-pin Quad Flat Pack (VQFP) |
| VQG64 | 64-pin Quad Flat Pack (VQFP) |
| TQG100 | 100-pin Thin Quad Flat Pack (TQFP) |
| CSG144 | 144-pin Chip Scale Package (CSP) |

| Temperature | |
|---|---|
| I-Grade | $T_A$ = –40°C to +85°C |
| Q-Grade | $T_A$ = –40°C to +105°C with $T_J$ Maximum = 125°C |

## XA9500XL Automotive Requirements and Recommendations

### Requirements

The following requirements are for all automotive applications:

1. All automotive customers are required to keep the Macrocell Power selection set to low, and the Logic Optimization set to density when designing with ISE software. These are the default settings when XA9500XL devices are selected for design. These settings are found on the Process Properties page for Implement Design. See the ISE Online Help for details on these properties.
2. Use a monotonic, fast ramp power supply to power up XA9500XL . A $V_{CC}$ ramp time of less than 1 ms is required.
3. Do not float I/O pins during device operation. Floating I/O pins can increase $I_{CC}$ as input buffers will draw 1-2 mA per floating input. In addition, when I/O pins are floated, noise can propagate to the center of the CPLD. I/O pins should be appropriately terminated with keeper/bus-hold. Unused I/Os can also be configured as $C_{GND}$ (programmable GND).
4. Do not drive I/O pins without $V_{CC}$/$V_{CCIO}$ powered.
5. Sink current when driving LEDs. Because all Xilinx CPLDs have N-channel pull-down transistors on outputs, it is required that an LED anode is sourced through a resistor externally to $V_{CC}$. Consequently, this will give the brightest solution.
6. Avoid external pull-down resistors. Always use external pull-up resistors if external termination is required. This is because the XA9500XL Automotive CPLD, which includes some I/O driving circuits beyond the input and output buffers, may have contention with external pull-down resistors, and, consequently, the I/O will not switch as expected.

7. Do not drive I/Os pins above the $V_{CCIO}$ assigned to its I/O bank.
   a. The current flow can go into $V_{CCIO}$ and affect a user voltage regulator.
   b. It can also increase undesired leakage current associated with the device.
   c. If done for too long, it can reduce the life of the device.
8. Do not rely on the I/O states before the CPLD configures.
9. Use a voltage regulator which can provide sufficient current during device power up. As a rule of thumb, the regulator needs to provide at least three times the peak current while powering up a CPLD in order to guarantee the CPLD can configure successfully.
10. Ensure external JTAG terminations for TMS, TCK, TDI, TDO comply with IEEE 1149.1. All Xilinx CPLDs have internal weak pull-ups of ~50 kΩ on TDI, TMS, and TCK.
11. Attach all CPLD $V_{CC}$ and GND pins in order to have necessary power and ground supplies around the CPLD.
12. Decouple all $V_{CC}$ and $V_{CCIO}$ pins with capacitors of 0.01 µF and 0.1 µF closest to the pins for each $V_{CC}$/$V_{CCIO}$-GND pair.

## Recommendations

The following recommendations are for all automotive applications.

1. Use strict synchronous design (only one clocking event) if possible. A synchronous system is more robust than an asynchronous one.
2. Include JTAG stakes on the PCB. JTAG stakes can be used to test the part on the PCB. They add benefit in reprogramming part on the PCB, inspecting chip internals with INTEST, identifying stuck pins, and inspecting programming patterns (if not secured).
3. XA9500XL Automotive CPLDs work with any power sequence, but it is preferable to power the $V_{CCI}$ (internal $V_{CC}$) before the $V_{CCIO}$ for the applications in which any glitches from device I/Os are unwanted.
4. Do not disregard report file warnings. Software identifies potential problems when compiling, so the report file is worth inspecting to see exactly how your design is mapped onto the logic.
5. Understand the Timing Report. This report file provides a speed summary along with warnings. Read the timing file (*.tim) carefully. Analyze key signal chains to determine limits to given clock(s) based on logic analysis.
6. Review Fitter Report equations. Equations can be shown in ABEL-like format, or can also be displayed in Verilog or VHDL formats. The Fitter Report also includes switch settings that are very informative of other device behaviors.
7. Let design software define pinouts if possible. Xilinx CPLD software works best when it selects the I/O pins and manages resources for users. It can spread signals around and improve pin-locking. If users must define pins, plan resources in advance.
8. Perform a post-fit simulation for all speeds to identify any possible problems (such as race conditions) that might occur when fast-speed silicon is used instead of slow-speed silicon.
9. Distribute SSOs (Simultaneously Switching Outputs) evenly around the CPLD to reduce switching noise.
10. Terminate high speed outputs to eliminate noise caused by very fast rising/falling edges.

## Warranty Disclaimer

THIS WARRANTY DOES NOT EXTEND TO ANY IMPLEMENTATION IN AN APPLICATION OR ENVIRONMENT THAT IS NOT CONTAINED WITHIN XILINX SPECIFICATIONS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS. FURTHER, PRODUCTS ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF THE VEHICLE UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE AND ALSO A WARNING SIGNAL TO THE OPERATOR OF THE VEHICLE UPON FAILURE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 05/17/02 | 1.0 | Initial Xilinx release. |
| 07/17/02 | 1.1 | Updated $N_{PE}$ Quality and Reliability specification. |
| 02/03/03 | 1.2 | Added reference to XC9500XL, XC9536XL, and XC9572XL data sheets. |
| 05/21/04 | 1.3 | Updated the VQ44 column of Table 2 and the Component Availability table on page 2. |
| 10/18/04 | 1.4 | Extensive edits to update family from IQ to XA. |
| 09/29/05 | 1.5 | Changes to packaging information. |
| 01/12/07 | 1.6 | Updated for introduction of individual device data sheets. $f_{SYSTEM}$ changed to 64.5 MHz. |
| 04/03/07 | 1.7 | Add programming temperature range warning on page 1. |