International IƆR Rectifier

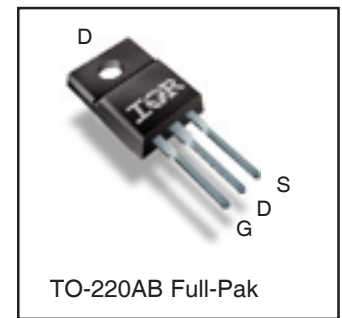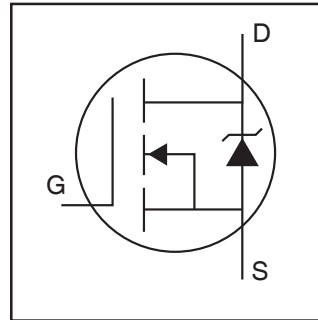# IRFI4410ZGPbF

HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free

V_{DSS}		100V
$R_{DS(on)}$	typ.	7.9mΩ
	max.	9.3mΩ
I_D		43A

TO-220AB Full-Pak

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	43	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	30	
I_{DM}	Pulsed Drain Current ①	170	
P_D @T_C = 25°C	Maximum Power Dissipation	47	W
	Linear Derating Factor	0.3	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	310	mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	——	3.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	——	65	

Static @ T$_J$ = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	–––	V	V$_{GS}$ = 0V, I$_D$ = 250μA
V$_{(BR)DSS}$/ T$_J$	Breakdown Voltage Temp. Coefficient	——	95	–––	mV/°C	Reference to 25°C, I$_D$ = 5mA ③
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	7.9	9.3	m	V$_{GS}$ = 10V, I$_D$ = 26A ③
V$_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 150μA
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	20	μA	V$_{DS}$ = 100V, V$_{GS}$ = 0V
		——	——	250		V$_{DS}$ = 100V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V$_{GS}$ = -20V
R$_{G(int)}$	Internal Gate Resistance	——	0.9	–––		

Dynamic @ T$_J$ = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	80	——	–––	S	V$_{DS}$ = 50V, I$_D$ = 26A
Q$_g$	Total Gate Charge	——	81	110	nC	I$_D$ = 26A
Q$_{gs}$	Gate-to-Source Charge	——	18	–––		V$_{DS}$ = 50V
Q$_{gd}$	Gate-to-Drain ("Miller") Charge	——	23	–––		V$_{GS}$ = 10V ③
t$_{d(on)}$	Turn-On Delay Time	——	15	–––	ns	V$_{DD}$ = 65V
t$_r$	Rise Time	——	27	–––		I$_D$ = 26A
t$_{d(off)}$	Turn-Off Delay Time	——	43	–––		R$_G$ = 2.7
t$_f$	Fall Time	——	30	–––		V$_{GS}$ = 10V ③
C$_{iss}$	Input Capacitance	——	4910	–––	pF	V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	330	–––		V$_{DS}$ = 50V
C$_{rss}$	Reverse Transfer Capacitance	——	150	–––		f = 1.0MHz
C$_{oss}$ eff. (ER)	Effective Output Capacitance (Energy Related)	——	420	–––		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 80V ⑥, See Fig.11
C$_{oss}$ eff. (TR)	Effective Output Capacitance (Time Related)	——	680	–––		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 80V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	43	A	MOSFET symbol showing the
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	170	A	integral reverse p-n junction diode.
V$_{SD}$	Diode Forward Voltage	——	——	1.3	V	T$_J$ = 25°C, I$_S$ = 26A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	47	71	ns	T$_J$ = 25°C, V$_R$ = 85V,
		——	54	81		T$_J$ = 125°C, I$_F$ = 26A
Q$_{rr}$	Reverse Recovery Charge	——	110	160	nC	T$_J$ = 25°C, di/dt = 100A/μs ③
		——	140	210		T$_J$ = 125°C
I$_{RRM}$	Reverse Recovery Current	——	2.5	–––	A	T$_J$ = 25°C
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T$_{Jmax}$, starting T$_J$ = 25°C, L = 0.91mH
R$_G$ = 25Ω, I$_{AS}$ = 26A, V$_{GS}$ =10V. Part not recommended for use above this value.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ R$_θ$ is measured at T$_J$ approximately 90°C

⑤ C$_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{DSS}$.

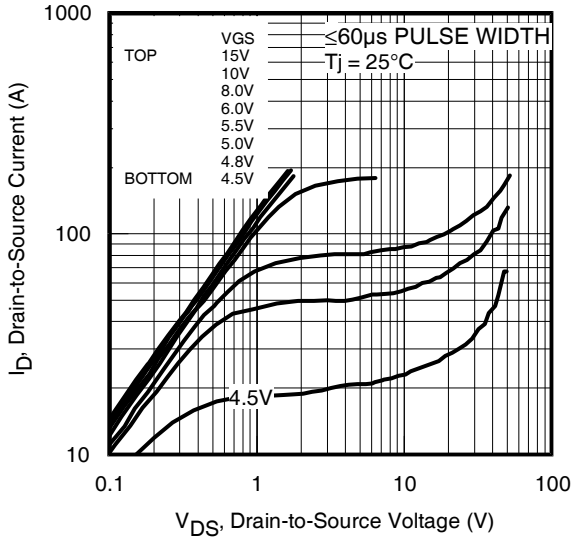⑥ C$_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{DSS}$.

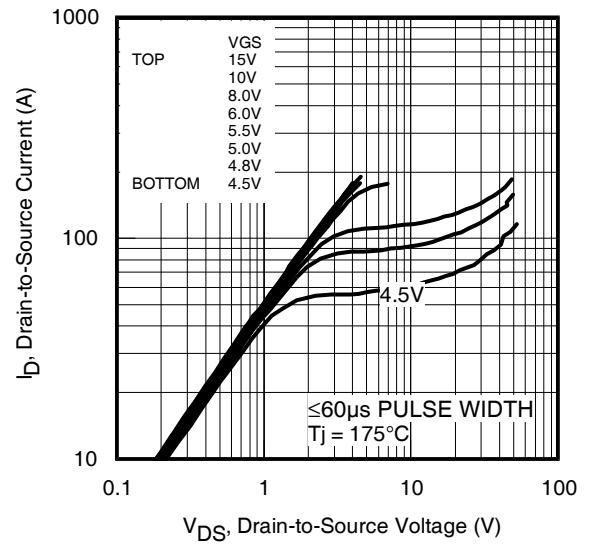**Fig 1.** Typical Output Characteristics
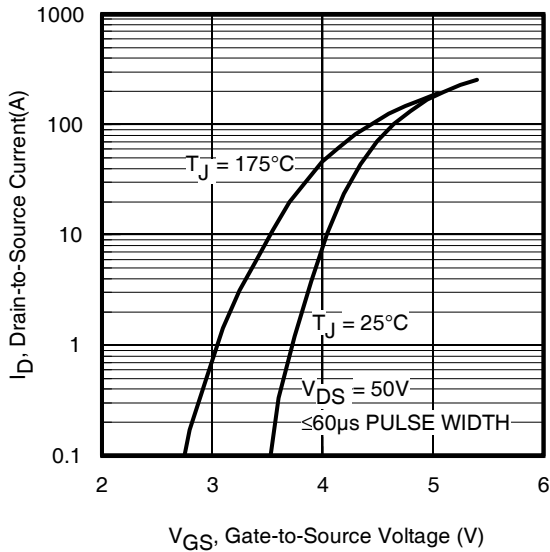
Fig 2. Typical Output Characteristics

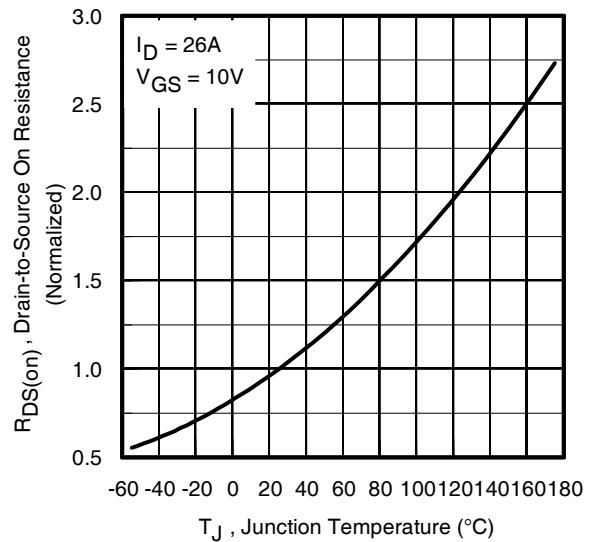**Fig 3.** Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature
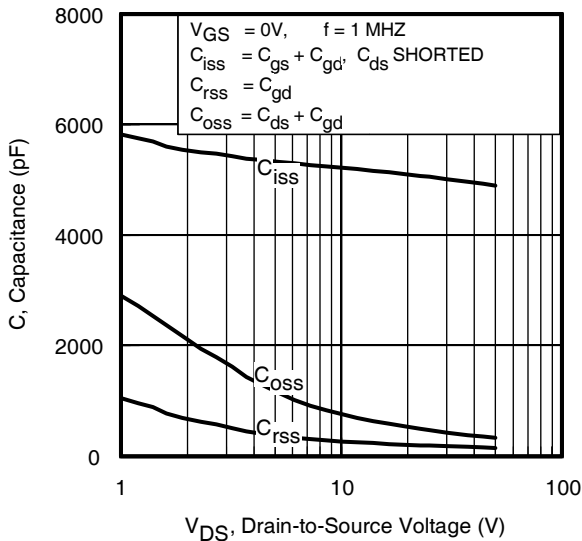
Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
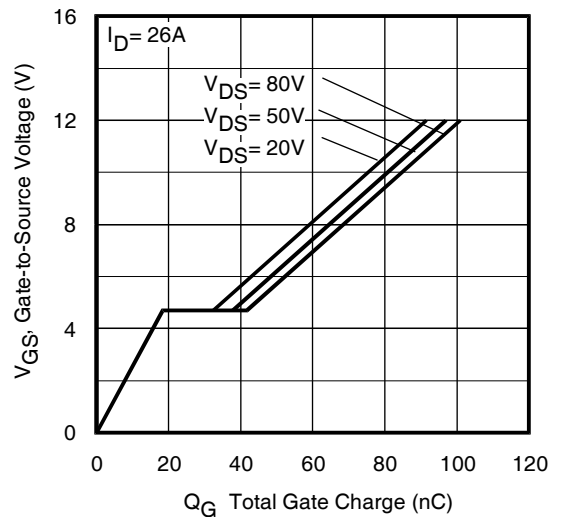
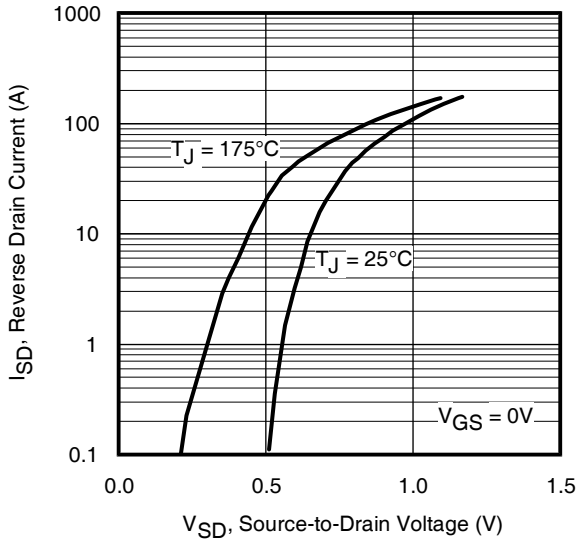**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

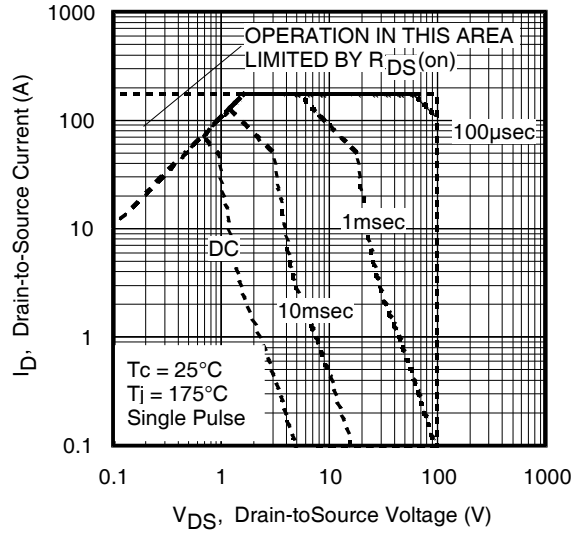**Fig 7.** Typical Source-Drain Diode
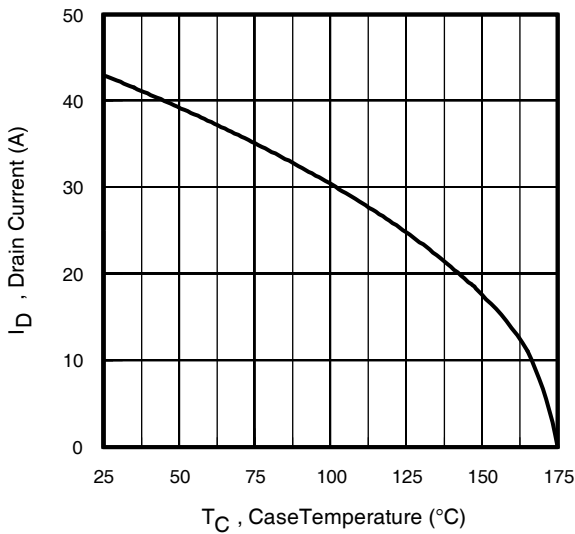Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs.
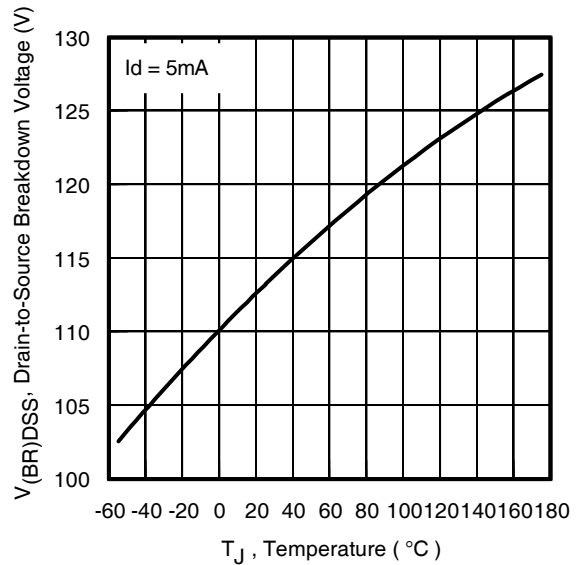Case Temperature

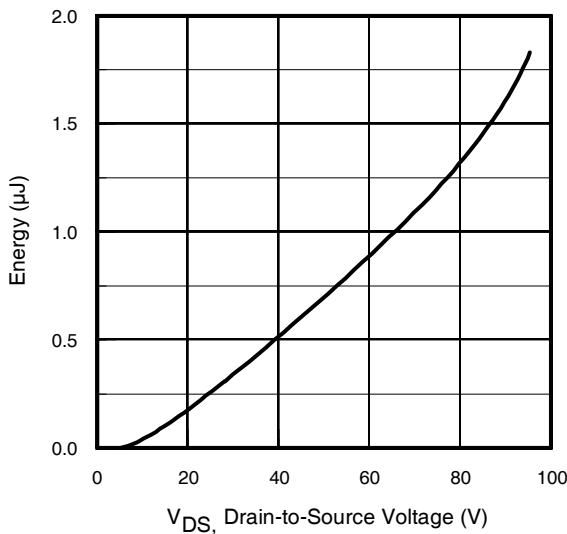**Fig 10.** Drain-to-Source Breakdown Voltage

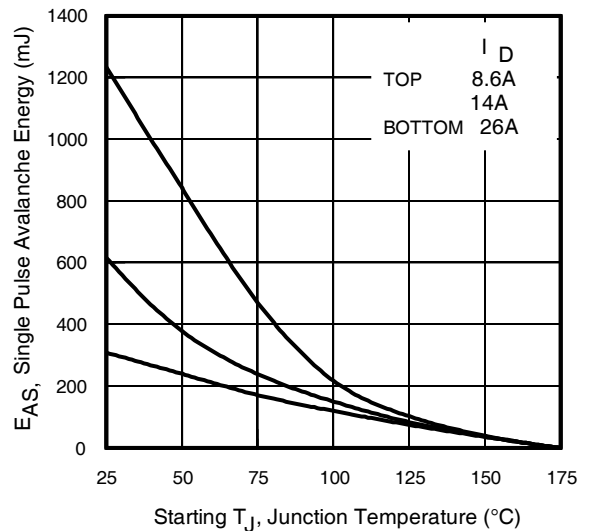**Fig 11.** Typical C_{OSS} Stored Energy

Fig 12. Maximum Avalanche Energy Vs. DrainCurrent
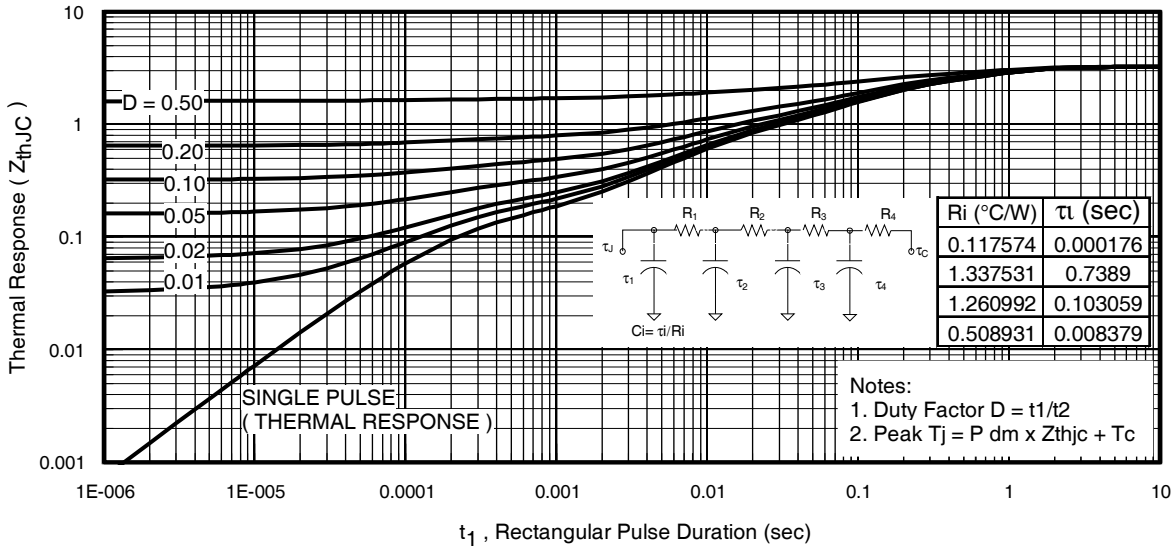
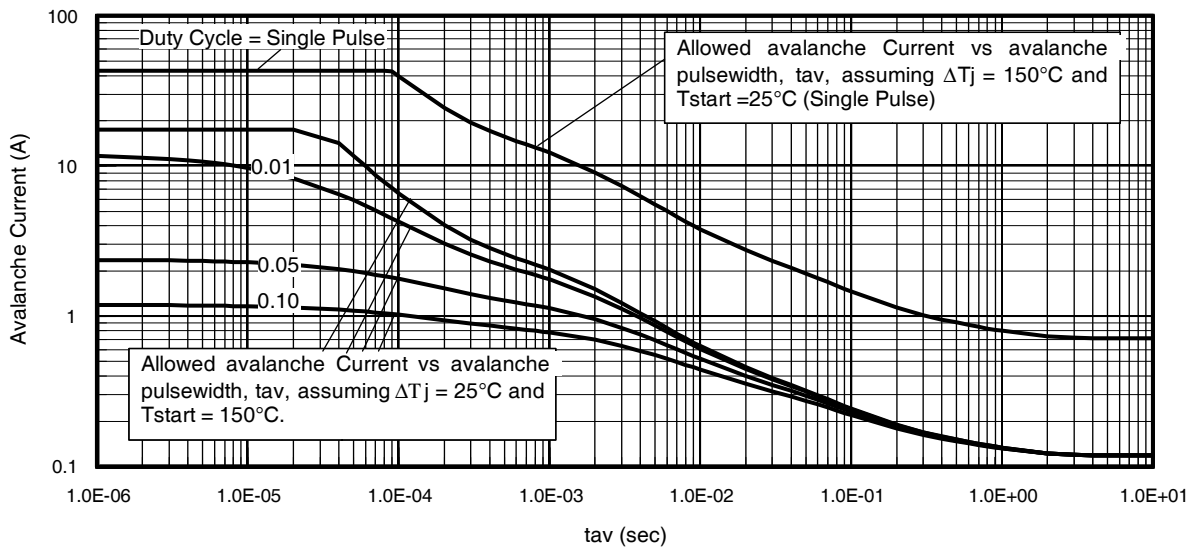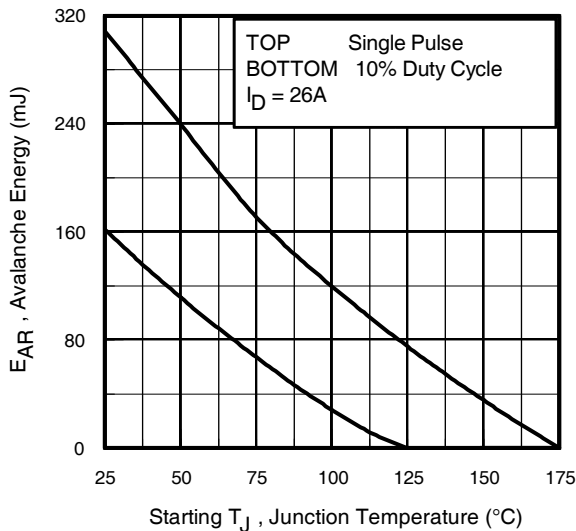**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

In the inset of Fig 13:

Ri (°C/W)	τι (sec)
0.117574	0.000176
1.337531	0.7389
1.260992	0.103059
0.508931	0.008379

$C_i = \tau_i / R_i$

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

Fig 14. Typical Avalanche Current vs.Pulsewidth

Allowed avalanche Current vs avalanche pulsewidth, tav, assuming $\Delta T_j = 150°C$ and Tstart =25°C (Single Pulse)

Allowed avalanche Current vs avalanche pulsewidth, tav, assuming $\Delta T_j = 25°C$ and Tstart = 150°C.

TOP   Single Pulse
BOTTOM   10% Duty Cycle
$I_D = 26A$

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D (ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
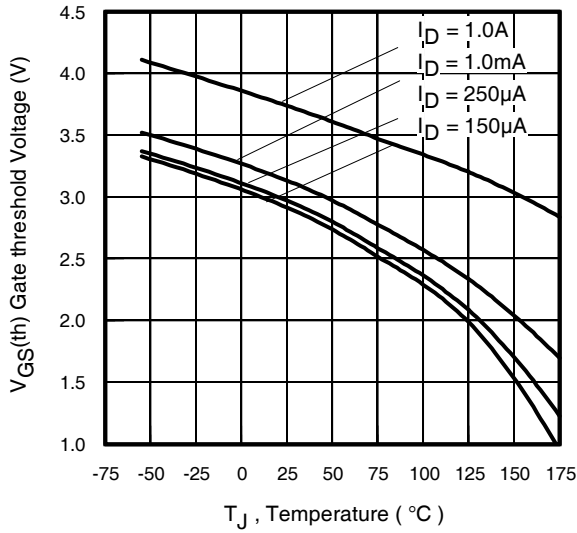$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

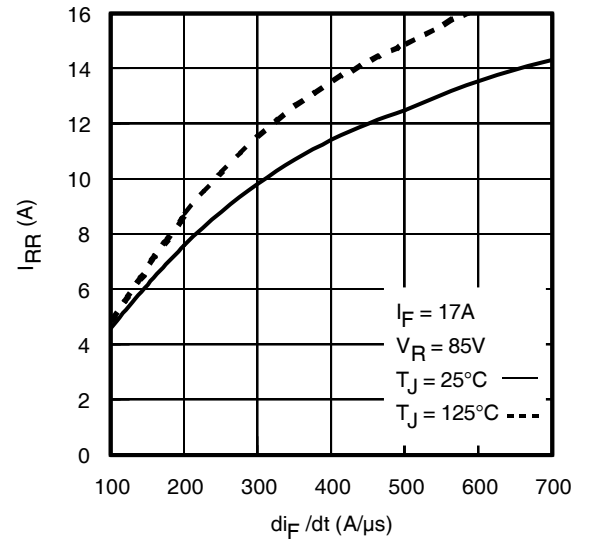**Fig 16.** Threshold Voltage Vs. Temperature

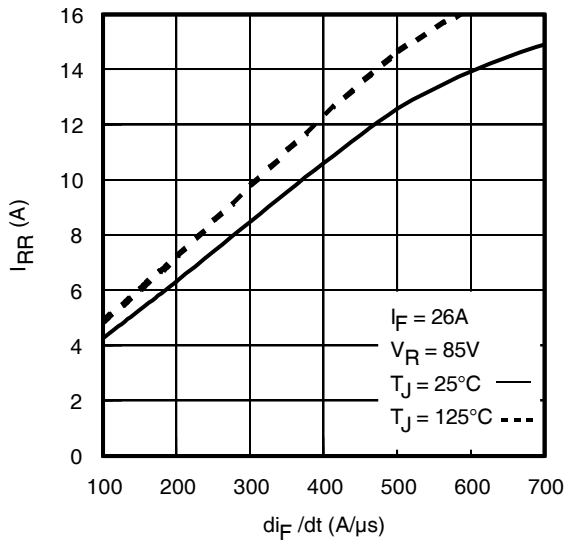**Fig. 17** - Typical Recovery Current vs. di$_f$/dt

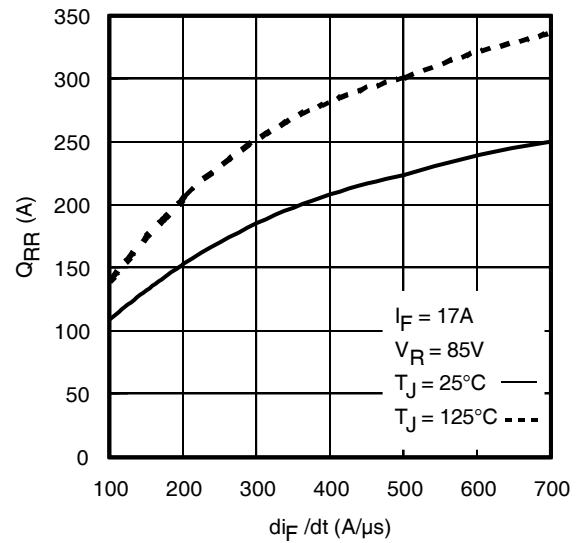**Fig. 18** - Typical Recovery Current vs. di$_f$/dt
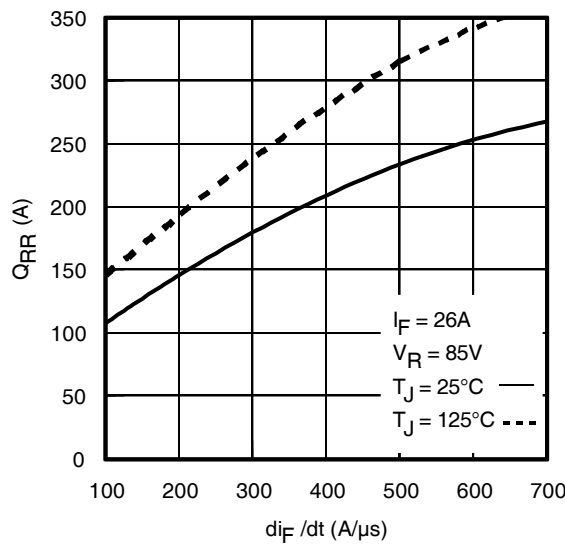

Fig. 19 - Typical Stored Charge vs. di$_f$/dt

Fig. 20 - Typical Stored Charge vs. di$_f$/dt

Circuit Layout Considerations
• Low Stray Inductance
• Ground Plane
• Low Leakage Inductance Current Transformer

• dv/dt controlled by R_G
• Driver same type as D.U.T.
• I_{SD} controlled by Duty Factor "D"
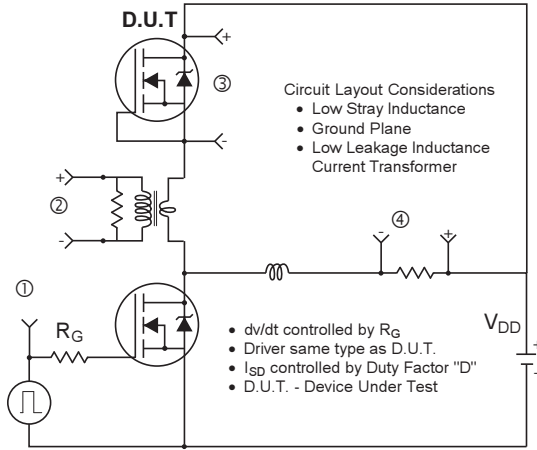• D.U.T. - Device Under Test

* V_{GS} = 5V for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs
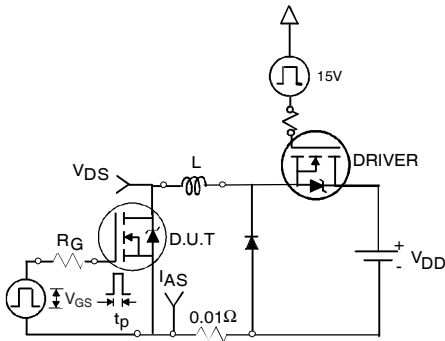

Fig 22a. Unclamped Inductive Test Circuit
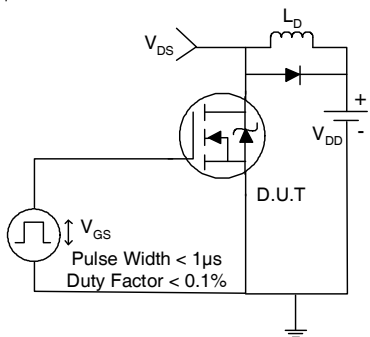

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit
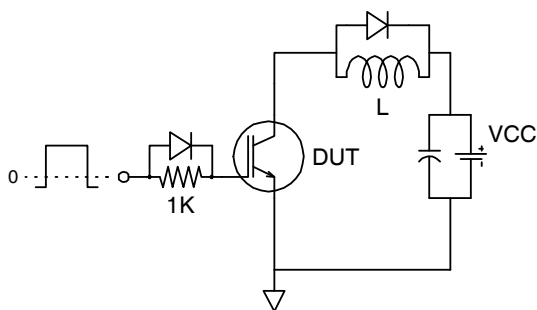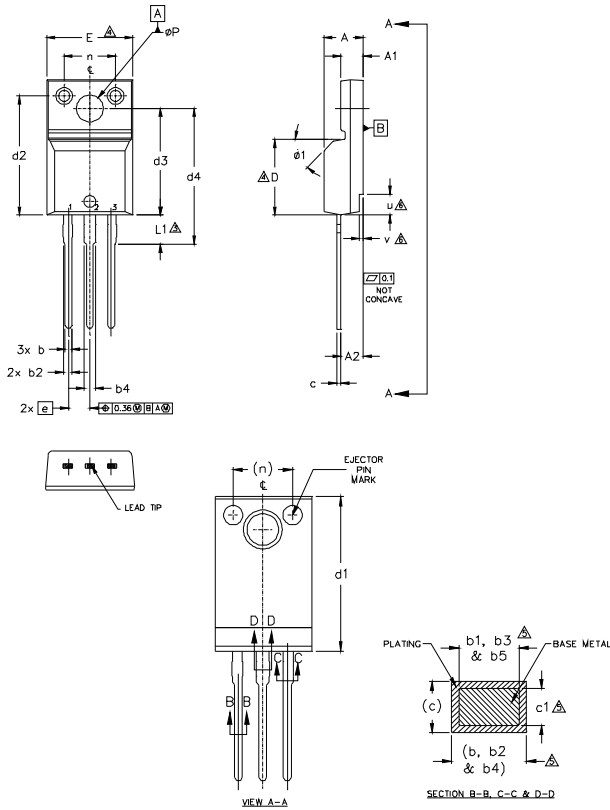

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

TO-220AB Full-Pak Package Outline (Dimensions are shown in millimeters (inches))

NOTES:
1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS | | | | NOTES |
| | MILLIMETERS | | INCHES | | |
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	
A1	2.57	2.83	.101	.111	
A2	2.41	2.92	.095	.115	
b	0.62	.094	0.24	.037	
b1	0.62	0.89	.024	0.35	5
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	5
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	5
c	0.33	0.63	.013	.025	5
c1	0.33	0.58	.013	.023	5
D	8.65	9.80	.341	.386	4
d1	15.80	16.12	.622	.635	
d2	13.97	14.22	.550	.560	
d3	12.30	12.92	.484	.509	
d4	8.64	9.91	.340	.390	
E	9.63	10.63	.379	.419	4
e	2.54 BSC		.100 BSC		
L	13.20	13.72	.520	.540	
L1	3.10	2.31	.122	.138	3
n	6.05	6.15	.238	.242	
øP	3.05	3.45	.120	.136	
u	2.40	2.50	.094	.098	6
v	0.40	0.50	.016	.020	6
ø1	–	45°	–	45°	

LEAD ASSIGNMENTS

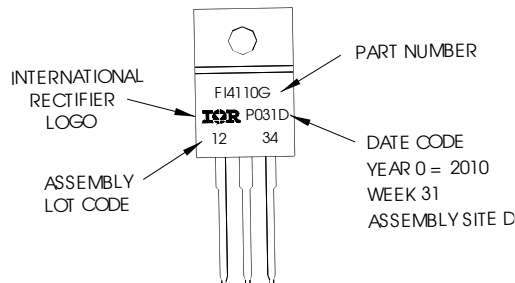HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER

TO-220AB Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI4110G
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 31, 2010

Notes: - "P" in assembly line position indicates "Lead-Free"
- "G" suffix in part number indicates "Halogen-Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

FI4110G
IR P031D
12   34

ASSEMBLY LOT CODE

DATE CODE
YEAR 0 = 2010
WEEK 31
ASSEMBLY SITE D

TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 101N Sepulveda Blvd, El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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8   www.irf.com