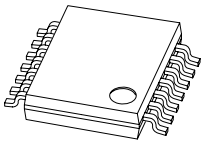


IP4769CZ14

VGA interface ESD protection with integrated termination resistors

Rev. 1 — 17 January 2011 Product data sheet

1. Product profile

1.1 General description

The IP4769CZ14 connects between the Video Graphics Adapter (VGA)/Digital Video Interface (DVI) and the video transmitter like e.g. a PC graphic card or the VGA receiver like e.g. a PC Monitor.

The IP4769CZ14 includes ElectroStatic Discharge (ESD) protection for the Data Display Channel (DDC) signals, DDC level shifting and ESD protection for both SYNChronization (SYNC) lines as well as high-level ESD protection diodes for the Red-Green-Blue (RGB) signal lines.

The DDC level shifting can be used to shift the 5 V DDC bus at the connector side to 3.3 V or 2.5 V on the internal side.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Integrated high-level ESD protection and level shifting
- DDC level shifting from 5 V to 3.3 V or 2.5 V
- IEC 61000-4-2, ±4 kV rail-to-rail clamping for each I/O line
- Channel capacitance C_{ch} < 4 pF

1.3 Applications

- To reduce ElectroMagnetic Interferences (EMI)/Radio Frequency Interferences (RFI) and to provide downstream ESD protection for:
  - VGA interfaces including DDC channels
  - Desktop and notebook PCs
  - Graphics cards
  - Set-top boxes

2. Pinning information

2.1 Pinning

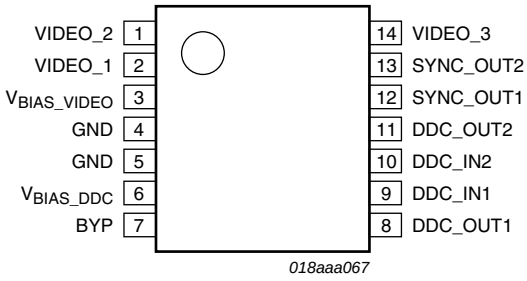


Fig 1. Pin configuration

2.2 Pin description

Table 1. Pin description

Symbol	Pin	Description
VIDEO_2	1	video signal ESD protection channel 2
VIDEO_1	2	video signal ESD protection channel 1
V_{BIAS_VIDEO}	3	ESD bias voltage for VIDEO_1, VIDEO_2 and VIDEO_3 protection circuit
GND	4	ground
GND	5	ground
V_{BIAS_DDC}	6	bias voltage for DDC level shifter N-FET gates
BYP	7	optional external 100 nF bypass capacitor to enhance internal zener performance on SYNC_OUT1, SYNC_OUT2, DDC_OUT1 and DDC_OUT2
DDC_OUT1	8	DDC signal output 1; connector side
DDC_IN1	9	DDC signal input 1; VGA controller side
DDC_IN2	10	DDC signal input 2; VGA controller side
DDC_OUT2	11	DDC signal output 2; connector side
SYNC_OUT1	12	SYNC signal output 1; ESD clamp; connector side
SYNC_OUT2	13	SYNC signal output 2; ESD clamp; connector side
VIDEO_3	14	video signal ESD protection channel 3

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4769CZ14	TSSOP14	plastic shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

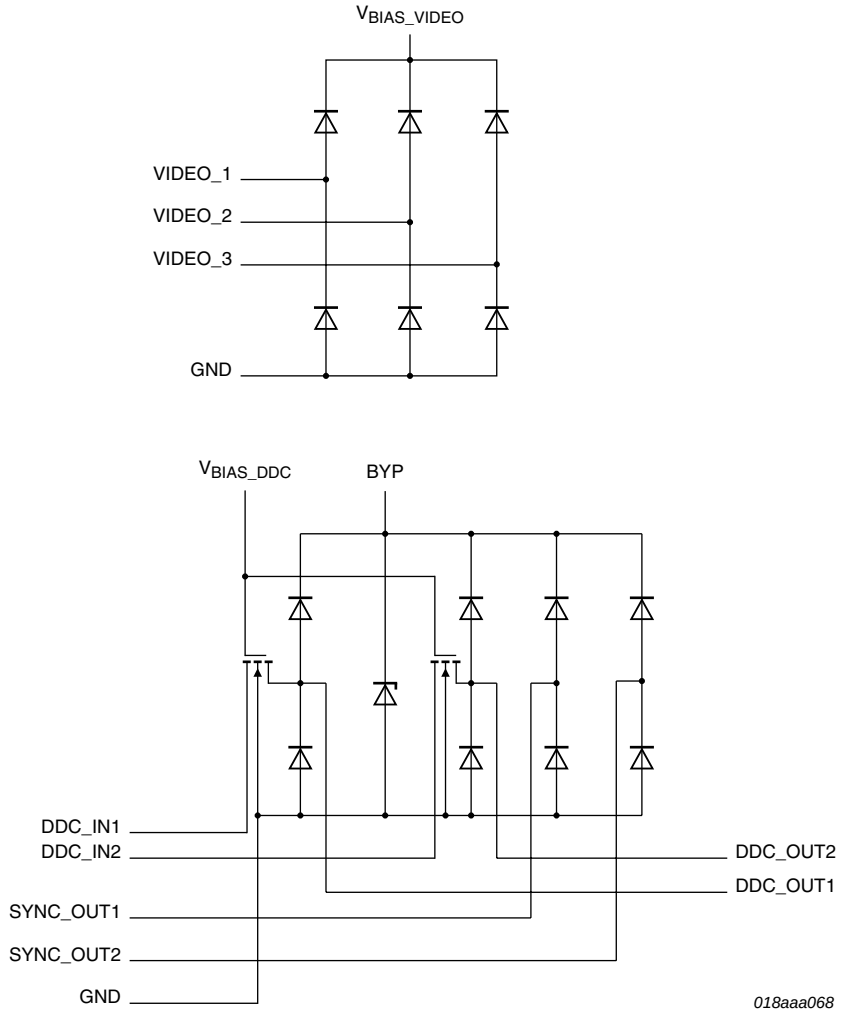


Fig 2. Functional diagram

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	all pins	[1][2]	-	±6	kV
			[3]	-	±200	V
			[4]	-	±2	kV
$V_{CC(VIDEO)}$	video supply voltage			–0.5	5.5	V
$V_{CC(DDC)}$	data display channel supply voltage			–0.5	5.5	V
$V_{I(VIDEO\_2)}$	input voltage on pin VIDEO_2			–0.5	$V_{CC(VIDEO)}$	V
$V_{I(VIDEO\_3)}$	input voltage on pin VIDEO_3			–0.5	$V_{CC(VIDEO)}$	V
$V_{I(DDC\_IN1)}$	input voltage on pin DDC_IN1			–0.5	5.5	V
$V_{I(DDC\_IN2)}$	input voltage on pin DDC_IN2			–0.5	5.5	V
$V_{O(DDC\_OUT1)}$	output voltage on pin DDC_OUT1			–0.5	5.5	V
$V_{O(DDC\_OUT2)}$	output voltage on pin DDC_OUT2			–0.5	5.5	V
T_{stg}	storage temperature			–55	+125	°C

[1] BYP, VCC_VIDEO and VCC_SYNC must be bypassed to GND via a low impedance ground plane with 100 nF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the pins (VIDEO_1; VIDEO_2; VIDEO_3; SYNC_OUT1; SYNC_OUT2; DCC_OUT1; DCC_OUT2) and GND.

[2] According to IEC 61000-4-2, level 3, contact discharge.

[3] Machine model according to ESD22-A115-A.

[4] Human Body Model (HBM) according to JESD22-A-J114D.

6. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature		–40	-	+85	°C

7. Characteristics

Table 5. Analog video (R, G, B) characteristics

$V_{CC(VIDEO)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	static input signals		-	-	10	μA
C_{ch}	channel capacitance	f = 1 MHz; V_I = 2.5 $V_{(p-p)}$; V_{bias} = 2.5 V	[1]	-	-	4	pF
$I_{i(video)}$	video input current	V_{IN} = $V_{CC(VIDEO)}$ or V_{IN} = GND		−1	-	+1	μA
V_F	forward voltage	I_F = 1 mA		-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

Table 6. DDC level shifter characteristics

$V_{CC(DDC)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{ch}	channel capacitance	f = 1 MHz; V_I = 2.5 $V_{(p-p)}$; V_{bias} = 2.5 V	[1]	-	-	4	pF
R_{dyn}	dynamic resistance	I = 1 A	[2]				
		positive transient		-	-	2.4	Ω
		negative transient		-	-	1.3	Ω
V_{CL}	clamping voltage	V_{ESD} = 8 kV; positive transient	[3]	-	8	-	V
ΔV_{on}	on-state voltage drop		[4]	-	85	140	mV
V_F	forward voltage	I_F = 1 mA		-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

[2] According to IEC 61000-4-5 and IEC 61000-4-9.

[3] According to IEC 61000-4-2, contact discharge.

[4] For level shifting N-FET.

Table 7. SYNC protection characteristics

$V_{CC(SYNC)}$ = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{ch}	channel capacitance	f = 1 MHz; $V_{CC(SYNC)}$ = 2.5 $V_{(p-p)}$; V_{bias} = 2.5 V	[1]	-	-	4	pF
V_F	forward voltage	I_F = 1 mA		-	0.7	-	V

[1] This parameter is guaranteed by design and characterization.

8. Application information

To maximize ESD clamping performance, the IP4769CZ14 should be placed as close as possible to the VGA/DVI connector. The ESD protection channels VIDEO_1, VIDEO_2 and VIDEO_3 are identical and can be connected in any order with R, B, G signals to simplify routing, and minimize stubs and vias. The SYNC protection lines are also identical and can be used in any order for HSYNC or VSYNC signals. The DDC level shifter lines are likewise identical in function.

The pull-up resistors on the DDC lines are dictated by the application, depending on the values of the internal pull-ups provided in the Application-Specific Integrated Circuit (ASIC), etc. Weak pull-ups may be required, for example, to pull up the DDC_INx lines to VCC_5V when no monitor is connected, if the local ASIC does not include internal pull-ups. Unexpected backdrive current can flow through these resistors though, when an external monitor is powered and the local VCC_5V is powered down. Backdrive protection should be considered if this is a concern.

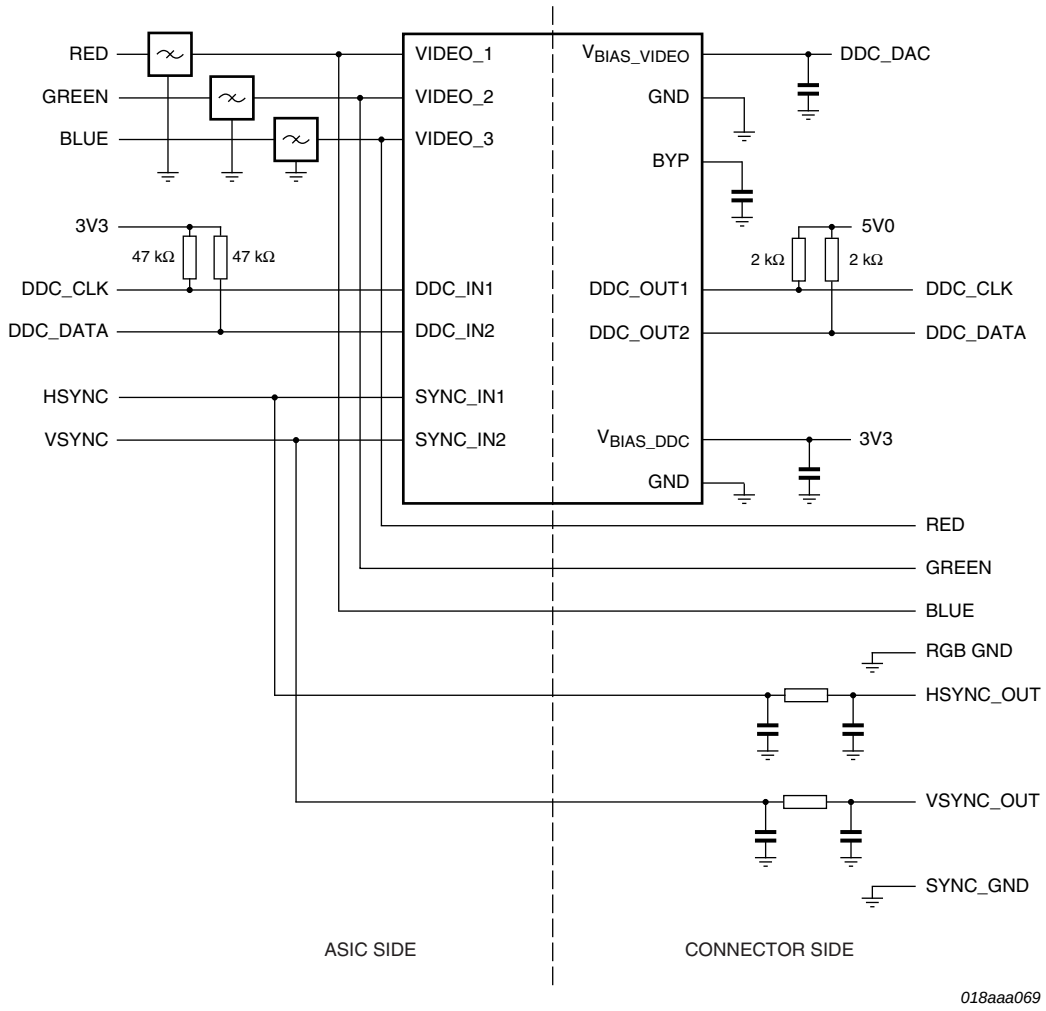
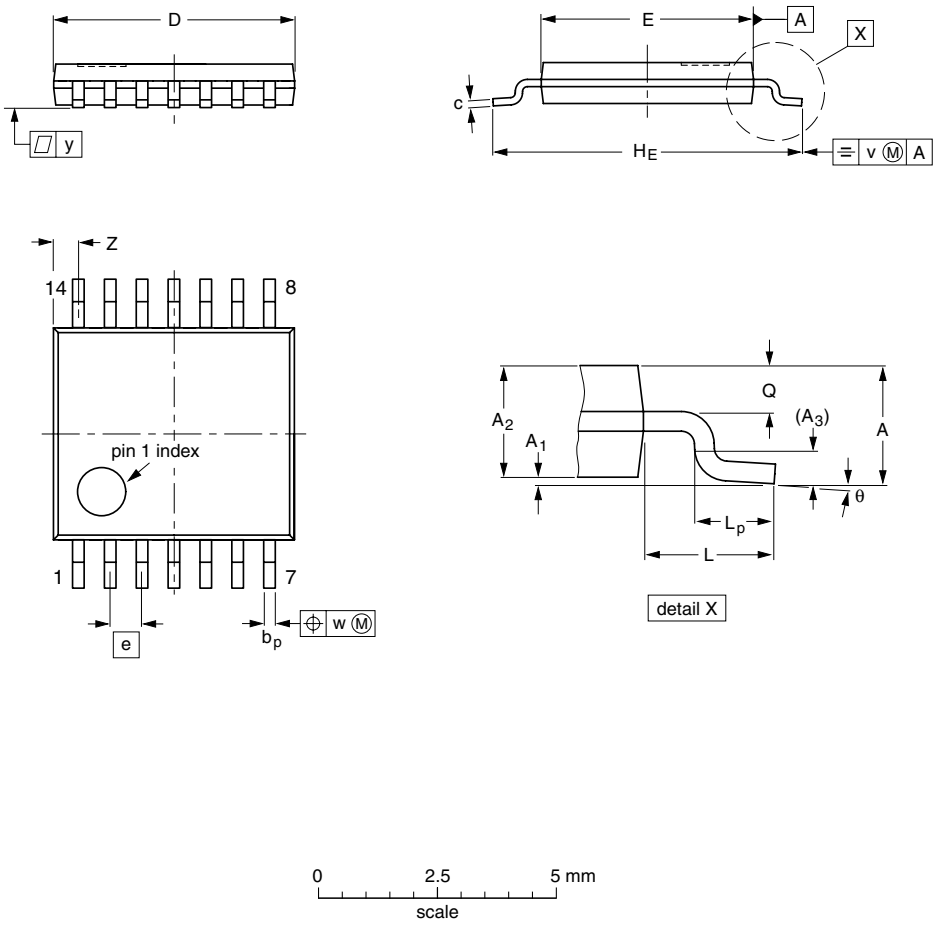


Fig 3. Application diagram

9. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 4. Package outline SOT402-1 (TSSOP14/MO-153)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4769CZ14 v.1	20110117	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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13. Contents

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