AD984X Timing Generator Board User's Manual

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EVAL BOARD USER'S MANUAL

Timing Generator Board Description

This Timing Generator Board is designed to be used as part of a two−board set, used in conjunction with an ON Semiconductor CCD Imager Evaluation Board. ON Semiconductor offers a variety of CCD Imager Boards that have been designed to operate with this Timing Generator Board. For more information on the available Imager Evaluation Boards, see the ON Semiconductor contact information at the end of this document.

The Timing Generator Board generates the timing signals necessary to operate ON Semiconductor area array Imager Boards, and also provides the power required by these Imager Boards via the board interface connector (J5). In addition the Timing Generator Board performs the signal processing and digitization of the analog output of the Imager Board. The analog output of the Imager Board is connected to the Timing Generator Board via coaxial cable.

The Timing Generator Board contains an Altera Programmable Logic Device (PLD) that can be In−System−Programmed (ISP) with code that is imager specific. This provides flexibility to operate many different Imager Boards with the same Timing Generator Board.

The Timing Generator Board has a digital Input interface to the Altera device that can be used to support various modes of operation depending on imager specific Altera code. The digital input interface also includes a serial interface to the delay lines and AFE parts on the Timing Generator Board so that adjustments may be made to their default operating conditions.
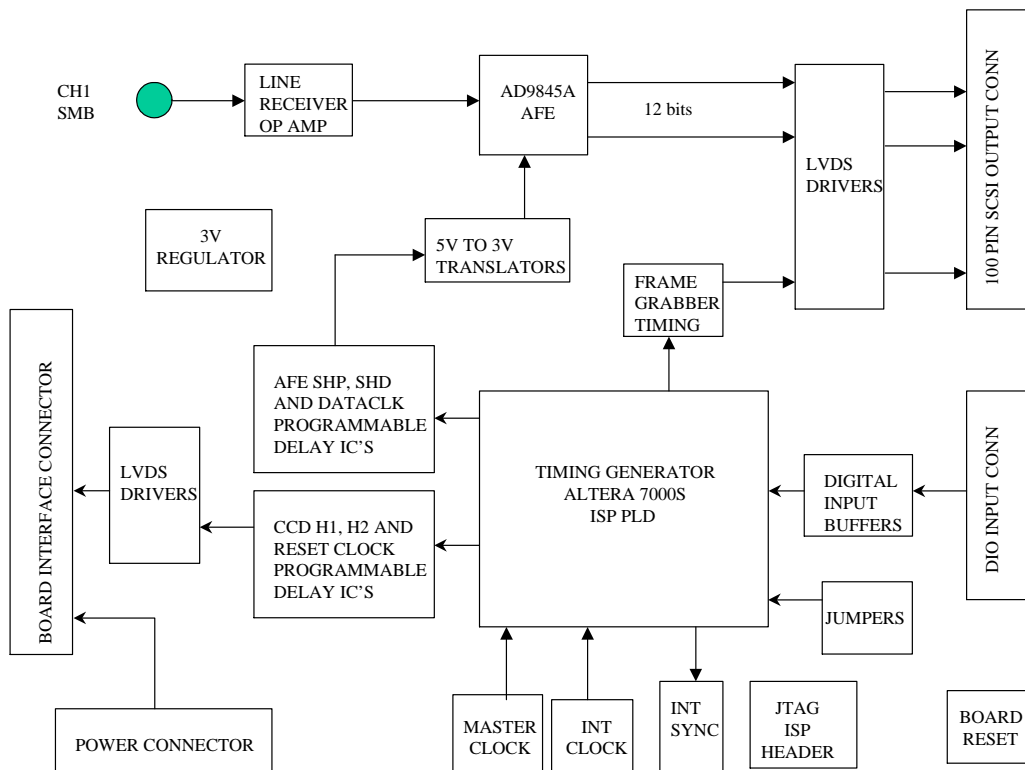

Figure 1. 3E8092 Timing Generator Board Block Diagram

TIMING GENERATOR BOARD INPUT REQUIREMENTS

Table 1. POWER SUPPLY INPUT REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V Supply	4.9	5	5.1	V
		800		mA
−5 V Supply	−5.1	−5	−4.9	V
		50		mA

TIMING GENERATOR BOARD ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the Timing Generator Board (see Figure 1 for a block diagram).

Power Connector

This connector provides the necessary power supply inputs to the Timing Generator Board. The connector also provides the VPLUS and VMINUS power supplies. These supplies are not used by the Timing Generator Board but are needed by the CCD Imager Boards. The Timing Generator Board simply routes these power supplies from the power connector to the board interface connector.

Power Supply Filtering

Power supplied to the board is de−coupled and filtered with ferrite beads and capacitors in order to suppress noise. For best noise performance, linear power supplies should be used to provide power to the boards.

Power−On Clear / Board Reset

The Altera Programmable Logic Device (PLD) resets and initializes the board on power-up, or when the BOARD RESET button in pressed. The ten silicon delay ICs are programmed to their default configuration, and the AFE device registers are programmed to their default configuration. The default configuration is defined separately for each particular CCD Image Sensor, and is detailed in the associated Altera Code Timing Specification.

Master Clock

The master clock is used to generate the pixel rate clocks. The pixel rate timing signals operate at a frequency that is divided down from the master clock frequency. The exact pixel rate frequency is Altera code dependent, but is limited to 1/2 the frequency of the master clock.

Table 2. TIMING BOARD CLOCK RATES

Timing Board PN	Master Clock	Pixel Clock (Max)
3E8090	40 MHz	20 MHz
3E8091	80 MHz	40 MHz
3E8092	56 MHz	28 MHz
3E8180	60 MHz	30 MHz

Unit Integration Clock

The unit integration clock is used for KAF series devices as a means for varying the integration time. This clock is not used for KAI series devices. The clock circuit consists of a 555 timer configured to oscillate at a frequency of 1 kHz. The output of this circuit, the INTEGRATE_CLK, has a 1 ms period, which is used by the Altera PLD as the unit integration time. When the Timing Generator Board is configured to operate in the internal integration mode, the integration time is controlled by the Timing Generator Board and will be a multiple of this unit integration time. The actual integration time is dependent on how the integration control lines on the digital input connector are configured, as well as on how the Altera PLD is programmed.

Digital Input Connector (Remote Digital Input Control)

The digital input connector can be used to input control signals to the evaluation board. These control signals can be used to adjust the operating mode of the evaluation board. The functions of the digital inputs depend on what code the Altera device is programmed with. This is an optional feature. No external digital inputs are required for board operation.

The digital input control lines to the board are buffered. The input pins to the buffer IC's are weakly held low by pull down resistors to GND. Therefore, with no digital inputs, the default level of the Timing Generator Board control lines is all zeros.

A three wire serial interface is also provided on the input connector. This interface really consists of five lines, a serial clock, serial data, and three separate serial load signals. Therefore the delays lines on the Timing Generator Board and each of the two AFE chips can be adjusted independent of one another via the serial interface.

Jumpers

There are four jumpers on the board that can be used to adjust the operating mode of the Timing Generator Board. The functions of the jumpers depend on how the Altera device is programmed, and is detailed in the associated Altera Code Timing Specification.

JTAG Header

This 10-pin header provides the user with the ability to reprogram the Altera PLD in place via Altera's BYTEBLASTER programming hardware.

Timing Generator PLD

The Programmable Logic Device (PLD) is an Altera 7000S series part. This device is In System Programmable (ISP) via a 10-pin JTAG header located on the board. In this way, the Altera device is programmed with imager specific code to operate the Imager Board to which the Timing Generator Board will be connected.

The Timing Generator PLD controls the overall flow of the evaluation board operation. The PLD outputs include the CCD clocks signals, AFE timing signals, and Frame Grabber synchronization signals.

The Timing Generator PLD programs the 10 silicon delay IC's on the AFE Timing Generator Board to their default delay settings via a 3 wire serial interface upon power up, or by depressing the BOARD_RESET button.

The Timing Generator PLD programs the registers of the two AFE chips on the AFE Timing Generator Board to their default settings via a 3 wire serial interface upon power up, or by depressing the BOARD_RESET button.

Programmable Delay IC's

There are 10 silicon delay lines on the Timing Generator Board. They are used to properly align the pixel rate CCD clock signals with respect to one another, as well as properly align the AFE signals timing with respect to the VOUT_CCD signal that is input from the CCD Imager Board.

The Timing Generator PLD programs the 10 delay IC's to their experimentally determined default conditions upon power up, or when the BOARD_RESET button is pressed.
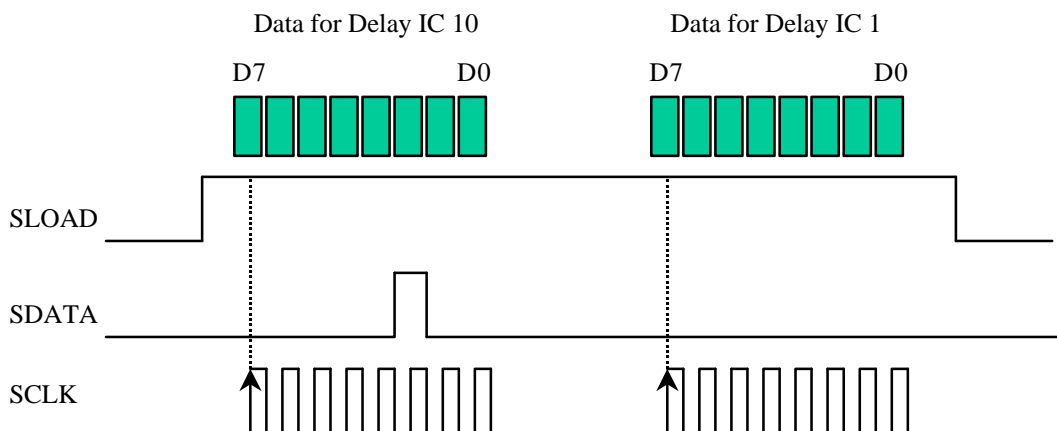
Figure 2. Delay Serial Load Timing

The signal delays can be adjusted by re-programming the delay IC's using the 3 wire serial interface provided on the Digital Input Connector (SLOAD, SDATA, SCLOCK). For programming purposes, the silicon delay lines are daisy-chained together (cascaded), the serial output pin of device 1 is tied to the serial input pin of the device 2 and so on. Therefore when making an adjustment to one or more delay lines, all the delay lines must be reprogrammed. The total number of serial bits must be eight times the number of units daisy−chained and each group of 8 bits must be sent in MSB−to−LSB order (See Reference 3.)

The programming order of the delay line IC's is as follows:

1. AFE DATACLK
2. AFE2 SHP
3. AFE1 SHP
4. AFE2 SHD
5. AFE1 SHD
6. H1A CLOCK
7. H1B CLOCK
8. H2A CLOCK
9. H2B CLOCK
10. RESET CLOCK

Programmable One−Shots

The pulse width of the AFE SHP and SHD clocks are set by programmable One−Shots. The One−Shots can be configured to provide clock signals with pulse widths from 5 ns to 15 ns.

The pulse width of the SHP and SHD clocks is set by configuring P[2..0], the inputs to the programmable one-shots. P2 is always held low. P[1..0] can be tied high or low to achieve the desired pulse width by populating the resistors on the board accordingly.

Table 3. SHP1 PULSEWIDTH

Pulse Width	P0	P1	P2	R48	R49	R54	R55	Notes
15 ns	0	0	0	OUT	OUT	IN	IN	
5 ns	1	0	0	OUT	IN	IN	OUT	
7.5 ns	0	1	0	IN	OUT	OUT	IN	Default
10 ns	1	1	0	IN	IN	OUT	OUT	

Table 4. SHD1 PULSEWIDTH

Pulse Width	P0	P1	P2	R33	R34	R36	R37	Notes
15 ns	0	0	0	OUT	OUT	IN	IN	
5 ns	1	0	0	OUT	IN	IN	OUT	
7.5 ns	0	1	0	IN	OUT	OUT	IN	Default
10 ns	1	1	0	IN	IN	OUT	OUT	

Table 5. SHP2 PULSEWIDTH

Pulse Width	P0	P1	P2	R59	R61	R63	R64	Notes
15 ns	0	0	0	OUT	OUT	IN	IN	
5 ns	1	0	0	OUT	IN	IN	OUT	
7.5 ns	0	1	0	IN	OUT	OUT	IN	Default
10 ns	1	1	0	IN	IN	OUT	OUT	

Table 6. SHD2 PULSEWIDTH

Pulse Width	P0	P1	P2	R39	R40	R42	R43	Notes
15 ns	0	0	0	OUT	OUT	IN	IN	
5 ns	1	0	0	OUT	IN	IN	OUT	
7.5 ns	0	1	0	IN	OUT	OUT	IN	Default
10 ns	1	1	0	IN	IN	OUT	OUT	

LVDS Drivers

Timing signals are sent to the Imager Board via the board interface connector using Low Voltage Differential Signaling (LVDS) drivers. LVDS combines high-speed connectivity with low noise and low power.

Board Interface Connector

This 80-pin connector provides both the timing signals and the necessary power to the CCD Imager Boards from the Timing Generator Board.

AD984X Analog Front End (AFE) Device

The Timing Generator Board has one or two analog input channels, each consisting of an operational amplifier buffer and an Analog Front End (AFE) device. The Timing Generator Board supports the AD984X family of AFE devices offered by Analog Devices Inc.

There are several variants in the AD984X family. The Timing Generator Board is populated differently depending on which AFE device is being used.

Table 7. TIMING BOARD CONFIGURATION OPTIONS

Timing Board PN	Analog Devices PN	Sampling Rate	Bit Depth	Channels
3E8090	AD9844AJST	20 MSPS	12	2
3E8091	AD9840AJST	40 MSPS	10	2
3E8092	AD9845AJST	28 MSPS	12	1
3E8180	AD9845AJST	28 MSPS	12	2

When using the AD9840 (10-bit, 40 MSPS) AFE, R81, R87, R88, and R89 are installed to tie what would be the least significant bits in a 12-bit system to AGND. Otherwise, these components are not installed.

When using a part that does not support Analog Devices PXGA modes, R68, R69, R71 and R72 are installed and R79 and R80 are not installed. By doing so, what would have been the VD and HD inputs to the AFE (for an AFE supporting PXGA) are not connected but instead those AFE pins are connected to AGND.

The AD984X family of parts has three modes of operation with respect to the analog input signal: CCD MODE, AUX1 MODE, and AUX2 MODE. The Timing Generator Board only supports the CCD MODE and the AUX1 MODE. In order to configure the board for AUX1 MODE operation, remove R74 and R75 and instead populate R65 and R66. This will route the VOUT_CCD to the AUX1IN pin of the AFE.

The Timing Generator PLD programs the AFE IC's to the default conditions upon power up, or when the BOARD_RESET button is depressed.

The AFE registers can be adjusted by re-programming the registers using the 3 wire serial interface provided on the Digital Input Connector. Each AFE can be adjusted independently because they each have their own serial load control line. (CH1_SLOAD, CH2_SLOAD)

The Timing Generator PLD programs the AFE IC's to the default conditions upon power up, or when the BOARD_RESET button is depressed.

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Table 8. AFE REGISTERS

Register Address	Register Description	Notes
0	Operation	1
1	VGA gain	1
2	Clamp	1
3	Control	1
4	PXGA 0	1
5	PXGA 1	1
6	PXGA 2	1
7	PXGA 3	1

1. See the AD984X specifications sheet (Reference 2) for details.

R/W A0 A1 A2 Test D0 D1 D2   D3 D4 D5 D6 D7 D8 D9 D10

CHX_SLOAD

SDATA

SCLK
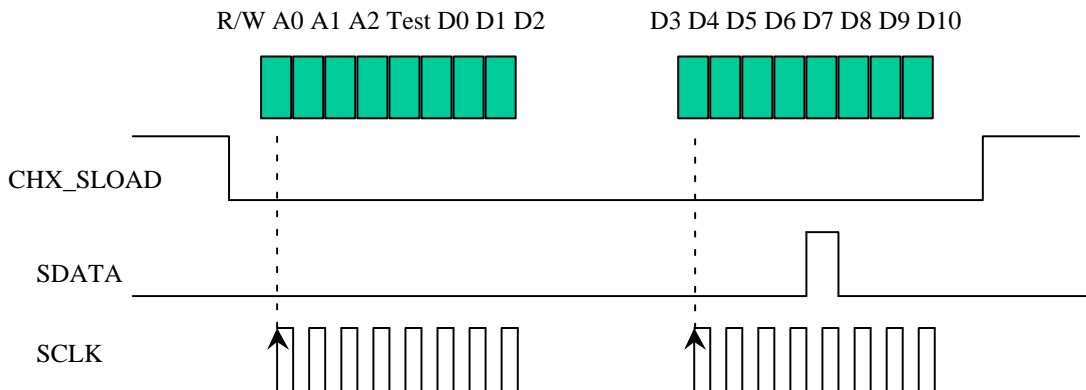
Figure 3. Register Serial Load Timing

VOUT CCD Signal Processing

Each of the two signal processing channels is designed to process a VOUT_CCD signal that is input from a CCD Imager Board in the following way:

The analog input signal from the Imager Board is buffered by an operational amplifier. This amplifier is in a non–inverting configuration with a gain of 1.25. The output of the amplifier is then AC–coupled into the AFE chip. The AFE chip processes the VOUT_CCD signal, then performs the A/D conversion and outputs 12 bits of digital information per pixel. The AFE device operates at 3.3 V and therefore requires the +5 V supply be regulated down to meet this requirement. Also the AFE timing signals are buffered and translated from 5 V levels to 3 V levels before being sent to the device.

Integration Output Connector

This output provides a signal that is high during the integration time period. This signal can be used to synchronize an external shutter or LED light source with the integration time period.

Output Connector

The output connector interfaces directly to the National Instruments PCI-1424 framegrabber. The output connector provides two channels of 12 bit output data in parallel in LVDS differential format. The connector also provides the three necessary PCI-1424 frame grabber synchronization signals in LVDS differential format.

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J1 and J2

J1 and J2 allow connection of VOUT_CCD video signal(s) from the CCD Imager Boards.

Table 9. DIGITAL INPUT CONNECTOR J3

Pin	Assignment	Function	Pin	Assignment
1	SLOAD	SERIAL PORT	2	GND
3	SDATA	SERIAL PORT	4	GND
5	SCLOCK	SERIAL PORT	6	GND
7	CH2_SLOAD	AFE2 SLOAD	8	GND
9	CH1_SLOAD	AFE1 SLOAD	10	GND
11	DIO13	Altera Code Dependent	12	GND
13	DIO12	Altera Code Dependent	14	GND
15	DIO11	Altera Code Dependent	16	GND
17	DIO10	Altera Code Dependent	18	GND
19	DIO9	Altera Code Dependent	20	GND
21	DIO8	Altera Code Dependent	22	GND
23	DIO7	Altera Code Dependent	24	GND
25	DIO6	Altera Code Dependent	26	GND
27	DIO5	Altera Code Dependent	28	GND
29	DIO4	Altera Code Dependent	30	GND
31	DIO3	Altera Code Dependent	32	GND
33	DIO2	Altera Code Dependent	34	GND
35	DIO1	Altera Code Dependent	36	GND
37	DIO0	Altera Code Dependent	38	GND
39	BRD_RESET	BOARD RESET	40	GND

Table 10. JTAG CONNECTOR J4

Pin	Assignment
1	TCK
2	AGND
3	TDO

Table 10. JTAG CONNECTOR J4

Pin	Assignment
4	+5 V_MTR
5	TMS
6	N.C.
7	N.C.
8	N.C.
9	TDI
10	AGND

Table 11. BOARD INTERFACE CONNECTOR J5

Pin	Assignment	Pin	Assignment
1	N.C.	2	N.C.
3	AGND	4	AGND
5	VES+	6	VES–
7	AGND	8	AGND
9	FDG+	10	FDG–
11	AGND	12	AGND
13	V3RD+	14	V3RD–
15	AGND	16	AGND
17	V2B+	18	V2B–
19	AGND	20	AGND
21	V2+	22	V2–
23	AGND	24	AGND
25	V1+	26	V1–
27	AGND	28	AGND
29	R+	30	R–
31	AGND	32	AGND
33	H2B+	34	H2B–
35	AGND	36	AGND
37	H2A+	38	H2A–
39	AGND	40	AGND
41	H1B+	42	H1B–
43	AGND	44	AGND
45	H1A+	46	H1A–
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	N.C.	60	N.C.
61	–5 V_MTR	62	–5 V_MTR
63	N.C.	64	N.C.

Table 11. BOARD INTERFACE CONNECTOR J5

Pin	Assignment	Pin	Assignment
65	AGND	66	AGND
67	N.C.	68	N.C.
69	+5 V_MTR	70	+5 V_MTR
71	N.C.	72	N.C.
73	AGND	74	AGND
75	N.C.	76	N.C.
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Table 12. INTEGRATE SYNC CONNECTOR J6

Pin	Assignment	Function
1	INTEGRATE	Signal is High during Integration Time Period
2	AGND	

Table 13. POWER CONNECTOR J7

Pin	Assignment
1	VMINUS
2	AGND
3	VPLUS
4	AGND
5	−5 V_MTR
6	AGND
7	+5 V_MTR
8	AGND

Table 14. JUMPER SELECTS J8

Jumper	Pin	Assignment	Pin	Assignment	Pin	Assignment	Function
P1	1	AGND	5	JMP3	9	VCC	Altera Code Dependent
P2	2	AGND	6	JMP2	10	VCC	Altera Code Dependent
P3	3	AGND	7	JMP1	11	VCC	Altera Code Dependent
P4	4	AGND	8	JMP0	12	VCC	Altera Code Dependent

Table 15. OUTPUT CONNECTOR J9

Pin	Assignment	Signal Level	Pin	Assignment	Signal Level
1	AOUT0+	LVDS	2	AOUT0−	LVDS
3	AOUT1+	LVDS	4	AOUT1−	LVDS
5	AOUT2+	LVDS	6	AOUT2−	LVDS
7	AOUT3+	LVDS	8	AOUT3−	LVDS
9	AOUT4+	LVDS	10	AOUT4−	LVDS
11	AOUT5+	LVDS	12	AOUT5−	LVDS
13	AOUT6+	LVDS	14	AOUT6−	LVDS
15	AOUT7+	LVDS	16	AOUT7−	LVDS

Table 15. OUTPUT CONNECTOR J9

Pin	Assignment	Signal Level	Pin	Assignment	Signal Level
17	AOUT8+	LVDS	18	AOUT8−	LVDS
19	AOUT9+	LVDS	20	AOUT9−	LVDS
21	AOUT10+	LVDS	22	AOUT10−	LVDS
23	AOUT11+	LVDS	24	AOUT11−	LVDS
25	–		26	–	
27	–		28	–	
29	–		30	–	
31	–		32	–	
33	N.C.		34	N.C.	
35	N.C.		36	N.C.	
37	N.C.		38	N.C.	
39	N.C.		40	N.C.	
41	FRAME+		42	FRAME−	
43	LINE+		44	LINE−	
45	N.C.		46	N.C.	
47	N.C.		48	N.C.	
49	PIXEL+		50	PIXEL−	
51	BOUT0+	LVDS	52	BOUT0−	LVDS
53	BOUT1+	LVDS	54	BOUT1−	LVDS
55	BOUT2+	LVDS	56	BOUT2−	LVDS
57	BOUT3+	LVDS	58	BOUT3−	LVDS
59	BOUT4+	LVDS	60	BOUT4−	LVDS
61	BOUT5+	LVDS	62	BOUT5−	LVDS
63	BOUT6+	LVDS	64	BOUT6−	LVDS
65	BOUT7+	LVDS	66	BOUT7−	LVDS
67	BOUT8+	LVDS	68	BOUT8−	LVDS
69	BOUT9+	LVDS	70	BOUT9−	LVDS
71	BOUT10+	LVDS	72	BOUT10−	LVDS
73	BOUT11+	LVDS	74	BOUT11−	LVDS
75	–		76	–	
77	–		78	–	
79	–		80	–	
81	–		82	–	
83	N.C.		84	N.C.	
85	N.C.		86	N.C.	
87	N.C.		88	N.C.	
89	N.C.		90	N.C.	
91	N.C.		92	N.C.	
93	N.C.		94	N.C.	
95	N.C.		96	N.C.	
97	N.C.		98	N.C.	
99	AGND		100	AGND	

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Timing Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the Truesense Imaging Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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