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Jameco Part Number 768731

Capacitor Array (IPC)

BENEFITS OF USING CAPACITOR ARRAYS

AVX capacitor arrays offer designers the opportunity to lower placement costs, increase assembly line output through lower component count per board and to reduce real estate requirements.

Reduced Costs

Placement costs are greatly reduced by effectively placing one device instead of four or two. This results in increased throughput and translates into savings on machine time. Inventory levels are lowered and further savings are made on solder materials, etc.

Space Saving

Space savings can be quite dramatic when compared to the use of discrete chip capacitors. As an example, the 0508 4-element array offers a space reduction of >40% vs. 4 x 0402 discrete capacitors and of >70% vs. 4 x 0603 discrete capacitors. (This calculation is dependent on the spacing of the discrete components.)

Increased Throughput

Assuming that there are 220 passive components placed in a mobile phone:

A reduction in the passive count to 200 (by replacing discrete components with arrays) results in an increase in throughput of approximately 9%.

A reduction of 40 placements increases throughput by 18%.

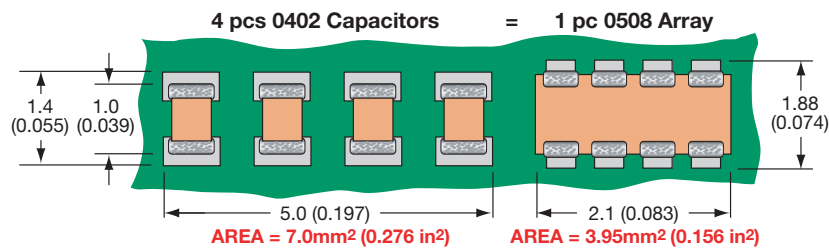
For high volume users of cap arrays using the very latest placement equipment capable of placing 10 components per second, the increase in throughput can be very significant and can have the overall effect of reducing the number of placement machines required to mount components:

If 120 million 2-element arrays or 40 million 4-element arrays were placed in a year, the requirement for placement equipment would be reduced by one machine.

During a 20Hr operational day a machine places 720K components. Over a working year of 167 days the machine can place approximately 120 million. If 2-element arrays are mounted instead of discrete components, then the number of placements is reduced by a factor of two and in the scenario where 120 million 2-element arrays are placed there is a saving of one pick and place machine.

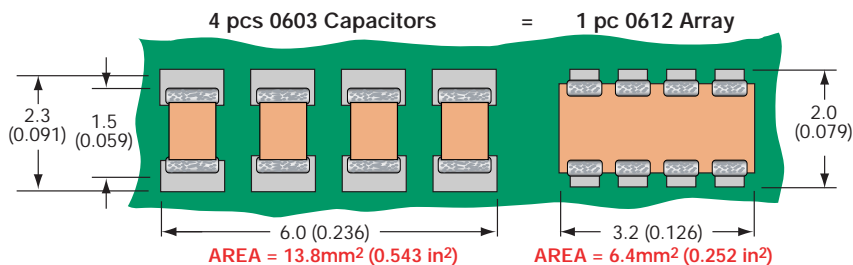
Smaller volume users can also benefit from replacing discrete components with arrays. The total number of placements is reduced thus creating spare capacity on placement machines. This in turn generates the opportunity to increase overall production output without further investment in new equipment.

W2A (0508) Capacitor Arrays



The 0508 4-element capacitor array gives a PCB space saving of over 40% vs four 0402 discretés and over 70% vs four 0603 discrete capacitors.

W3A (0612) Capacitor Arrays



The 0612 4-element capacitor array gives a PCB space saving of over 50% vs four 0603 discretés and over 70% vs four 0805 discrete capacitors.

Capacitor Array



NP0/C0G													X7R/X5R																				
SIZE	0405				0508				0508				0612				SIZE	0405				0508				0508				0612			
# Elements	2				2				4				4				# Elements	2				2				4				4			
Soldering	Reflow Only				Reflow/Wave				Reflow/Wave				Reflow/Wave				Soldering	Reflow Only				Reflow/Wave				Reflow/Wave				Reflow/Wave			
Packaging	All Paper				All Paper				Paper/Embossed				Paper/Embossed				Packaging	All Paper				All Paper				Paper/Embossed				Paper/Embossed			
Length	MM	1.00 ± 0.15 (0.039 ± 0.006)			MM	1.30 ± 0.15 (0.051 ± 0.006)			MM	1.30 ± 0.15 (0.051 ± 0.006)			MM	1.60 ± 0.150 (0.063 ± 0.006)			Length	MM	1.00 ± 0.15 (0.039 ± 0.006)			MM	1.30 ± 0.15 (0.051 ± 0.006)			MM	1.30 ± 0.15 (0.051 ± 0.006)			MM	1.60 ± 0.20 (0.063 ± 0.008)		
Width	MM	1.37 ± 0.15 (0.054 ± 0.006)			MM	2.10 ± 0.15 (0.083 ± 0.006)			MM	2.10 ± 0.15 (0.083 ± 0.006)			MM	3.20 ± 0.20 (0.126 ± 0.008)			Width	MM	1.37 ± 0.15 (0.054 ± 0.006)			MM	2.10 ± 0.15 (0.083 ± 0.006)			MM	2.10 ± 0.15 (0.083 ± 0.006)			MM	3.20 ± 0.20 (0.126 ± 0.008)		
Max. Thickness	MM	0.66 (0.026)			MM	0.94 (0.037)			MM	0.94 (0.037)			MM	1.35 (0.053)			Max. Thickness	MM	0.66 (0.026)			MM	0.94 (0.037)			MM	0.94 (0.037)			MM	1.35 (0.053)		
WVDC	16	25	50	16	25	50	100	16	25	50	100	16	25	50	100	WVDC	10	16	25	50	10	16	25	50	100	16	25	50	100	16	25	50	100
Cap (pF)	1.0															100																	
	1.2															120																	
	1.5															150																	
	1.8															180																	
	2.2															220																	
	2.7															270																	
	3.3															330																	
	3.9															390																	
	4.7															470																	
	5.6															560																	
	6.8															680																	
	8.2															820																	
	10															1000																	
	12															1200																	
	15															1500																	
	18															1800																	
	22															2200																	
	27															2700																	
	33															3300																	
	39															3900																	
	47															4700																	
	56															5600																	
	68															6800																	
	82															8200																	
	100															Cap 0.010 μF																	
	120															0.012																	
	150															0.015																	
	180															0.018																	
	220															0.022																	
	270															0.027																	
	330															0.033																	
	390															0.039																	
	470															0.047																	
	560															0.056																	
	680															0.068																	
	820															0.082																	
	1000															0.10																	
	1200															0.12																	
	1500															0.15																	
	1800															0.18																	
	2200															0.22																	
	2700															0.27																	
	3300															0.33																	
	3900															0.47																	
	4700															0.56																	
	5600															0.68																	
	6800															0.82																	
	8200															1.0																	
	Cap 0.010 (μF)															1.2																	
																1.5																	
																1.8																	
																2.2																	
																3.3																	
																4.7																	
																10																	
																22																	
																47																	
																100																	

= NP0/C0G

= X7R

= X5R

Capacitor Array

Multi-Value Capacitor Array (IPC)

GENERAL DESCRIPTION

A recent addition to the array product range is the Multi-Value Capacitor Array. These devices combine two different capacitance values in standard 'Cap Array' packages and are available with a maximum ratio between the two capacitance values of 100:1. The multi-value array is currently available in the 0405 and 0508 2-element styles and also in the 0612 4-element style.

Whereas to date AVX capacitor arrays have been suited to applications where multiple capacitors of the same value are used, the multi-value array introduces a new flexibility to the range. The multi-value array can replace discrete capacitors of different values and can be used for broadband decoupling applications. The 0508 x 2 element multi-value array would be particularly recommended in this application. Another application is filtering the 900/1800 or 1900MHz noise in mobile phones. The 0405 2-element, low capacitance value NPO, (COG) device would be suited to this application, in view of the space saving requirements of mobile phone manufacturers.

ADVANTAGES OF THE MULTI-VALUE CAPACITOR ARRAYS

Enhanced Performance Due to Reduced Parasitic Inductance

When connected in parallel, not only do discrete capacitors of different values give the desired self-resonance, but an additional unwanted parallel resonance also results. This parallel resonance is induced between each capacitor's self-resonant frequencies and produces a peak in impedance response. For decoupling and bypassing applications this peak will result in a frequency band of reduced decoupling and in filtering applications reduced attenuation.

The multi-value capacitor array, combining capacitors in one unit, virtually eliminates the problematic parallel resonance, by minimizing parasitic inductance between the capacitors, thus enhancing the broadband decoupling/filtering performance of the part.

Reduced ESR

An advantage of connecting two capacitors in parallel is a significant reduction in ESR. However, as stated above, using discrete components brings with it the unwanted side effect of parallel resonance. The multi-value cap array is an excellent alternative as not only does it perform the same function as parallel capacitors but also it reduces the uncertainty of the frequency response.

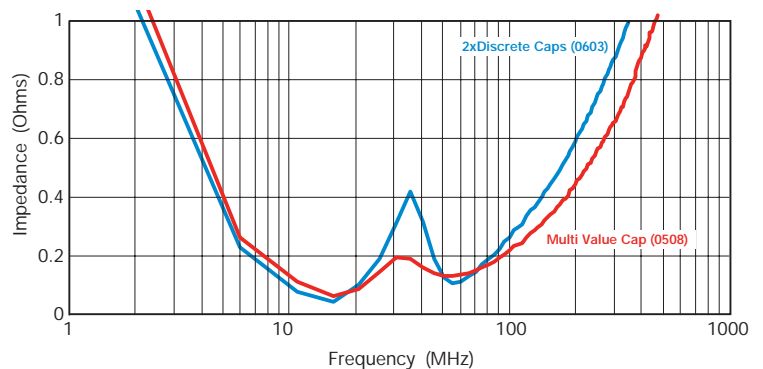
HOW TO ORDER

W	2	A	2	Y	C	102M	104M	A	T	2A
Style	Case Size	Array	Number of Caps	Voltage	Dielectric	1st Value	2nd Value	Failure Rate	Termination Code	Packaging & Quantity Code
	1 = 0405 2 = 0508 3 = 0612			6 = 6.3V Z = 10V Y = 16V 3 = 25V 5 = 50V 1 = 100V	A = NPO C = X7R D = X5R	Capacitance Code (In pF) 2 Sig. Digits + Number of Zeros	Capacitance Tolerance K = ±10% M = ±20%		T = Plated Ni and Sn	2A = 7" Reel (4000) 4A = 13" Reel (10000) 2F = 7" Reel (1000)

	Cap (Min/Max)	
	NPO	X5R/X7R
0612 4-element	100/471	221/104
0508 2-element	100/471	221/104
0405 2-element	100/101	101/103

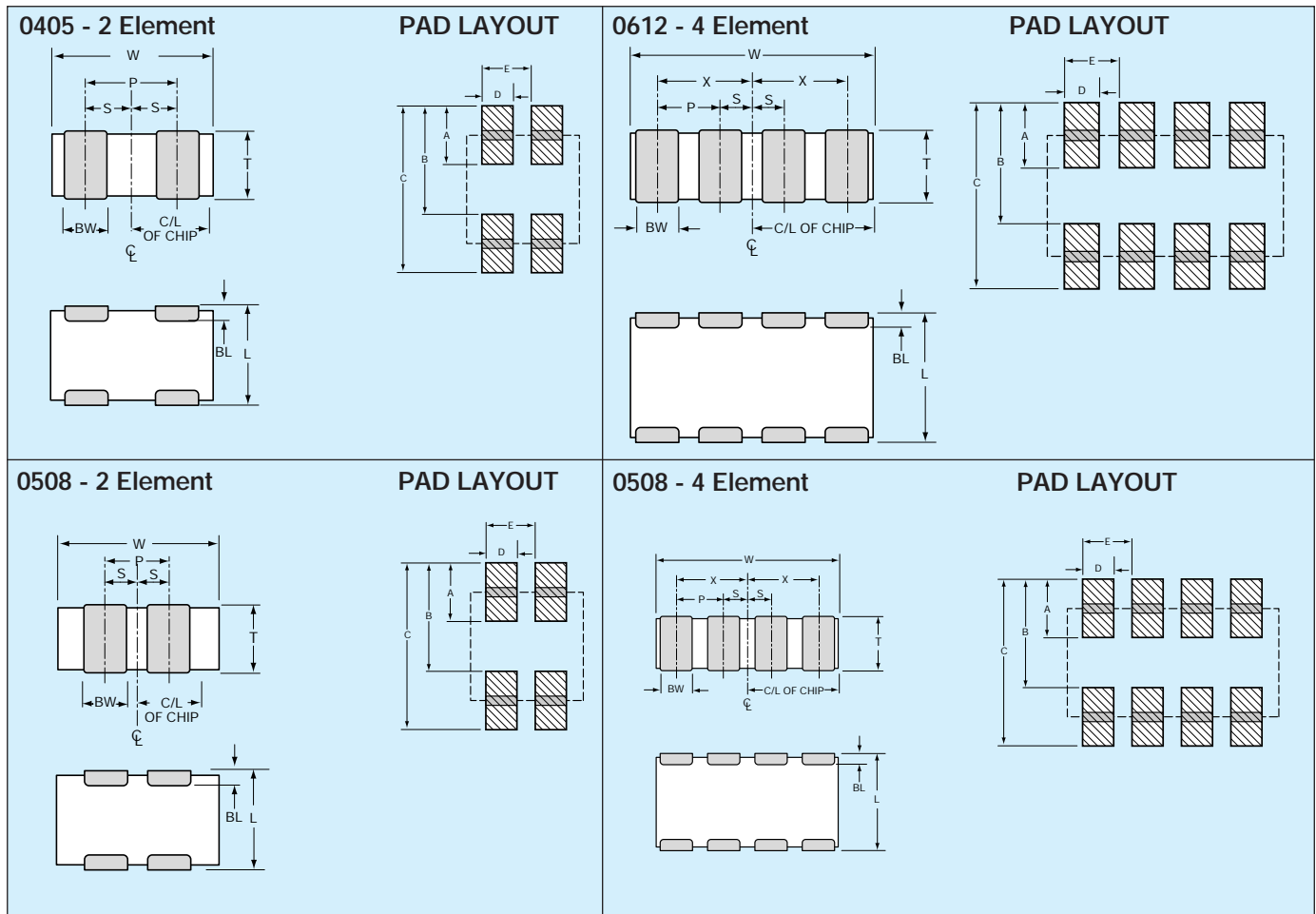
- Max. ratio between the two cap values is 1:100.
- The voltage of the higher capacitance value dictates the voltage of the multi-value part.
- Only combinations of values within a specific dielectric range are possible.

IMPEDANCE VS FREQUENCY



PART & PAD LAYOUT DIMENSIONS

millimeters (inches)



PART DIMENSIONS

0405 - 2 Element

L	W	T	BW	BL	P	S
1.00 ± 0.15 (0.039 ± 0.006)	1.37 ± 0.15 (0.054 ± 0.006)	0.66 MAX (0.026 MAX)	0.36 ± 0.10 (0.014 ± 0.004)	0.20 ± 0.10 (0.008 ± 0.004)	0.64 REF (0.025 REF)	0.32 ± 0.10 (0.013 ± 0.004)

0508 - 2 Element

L	W	T	BW	BL	P	S
1.30 ± 0.15 (0.051 ± 0.006)	2.10 ± 0.15 (0.083 ± 0.006)	0.94 MAX (0.037 MAX)	0.43 ± 0.10 (0.017 ± 0.004)	0.33 ± 0.08 (0.013 ± 0.003)	1.00 REF (0.039 REF)	0.50 ± 0.10 (0.020 ± 0.004)

0508 - 4 Element

L	W	T	BW	BL	P	X	S
1.30 ± 0.15 (0.051 ± 0.006)	2.10 ± 0.15 (0.083 ± 0.006)	0.94 MAX (0.037 MAX)	0.25 ± 0.06 (0.010 ± 0.003)	0.20 ± 0.08 (0.008 ± 0.003)	0.50 REF (0.020 REF)	0.75 ± 0.10 (0.030 ± 0.004)	0.25 ± 0.10 (0.010 ± 0.004)

0612 - 4 Element

L	W	T	BW	BL	P	X	S
1.60 ± 0.20 (0.063 ± 0.008)	3.20 ± 0.20 (0.126 ± 0.008)	1.35 MAX (0.053 MAX)	0.41 ± 0.10 (0.016 ± 0.004)	0.18 ± 0.08 (0.007 ± 0.003)	0.76 REF (0.030 REF)	1.14 ± 0.10 (0.045 ± 0.004)	0.38 ± 0.10 (0.015 ± 0.004)

PAD LAYOUT DIMENSIONS

0405 - 2 Element

A	B	C	D	E
0.46 (0.018)	0.74 (0.029)	1.20 (0.047)	0.30 (0.012)	0.64 (0.025)

0508 - 2 Element

A	B	C	D	E
0.68 (0.027)	1.32 (0.052)	2.00 (0.079)	0.46 (0.018)	1.00 (0.039)

0508 - 4 Element

A	B	C	D	E
0.56 (0.022)	1.32 (0.052)	1.88 (0.074)	0.30 (0.012)	0.50 (0.020)

0612 - 4 Element

A	B	C	D	E
0.89 (0.035)	1.65 (0.065)	2.54 (0.100)	0.46 (0.018)	0.79 (0.031)

Packaging of Chip Components



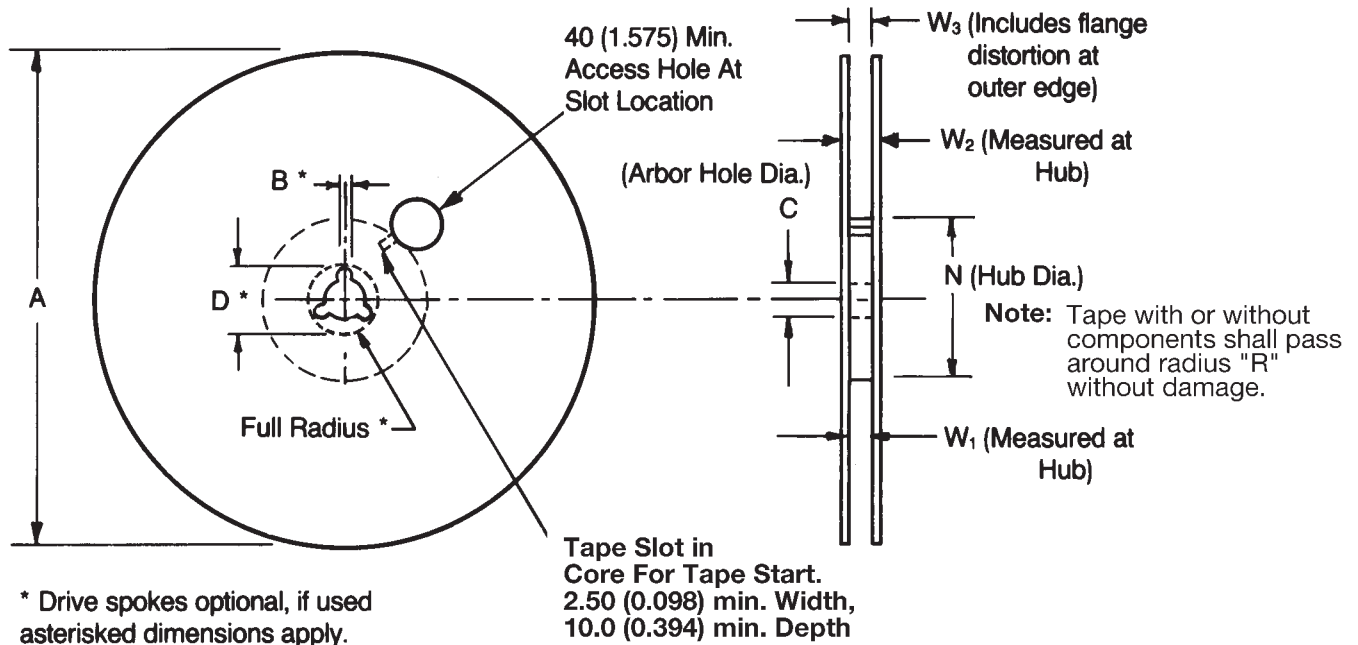
Automatic Insertion Packaging

TAPE & REEL QUANTITIES

All tape and reel specifications are in compliance with RS481.

	8mm	12mm	
Paper or Embossed Carrier	0612, 0508, 0805, 1206, 1210		
Embossed Only		1808	1812, 1825 2220, 2225
Paper Only	0201, 0306, 0402, 0603		
Qty. per Reel/7" Reel	2,000, 3,000 or 4,000, 10,000, 15,000 Contact factory for exact quantity	3,000	500, 1,000 Contact factory for exact quantity
Qty. per Reel/13" Reel	5,000, 10,000, 50,000 Contact factory for exact quantity	10,000	4,000

REEL DIMENSIONS



Tape Size ⁽¹⁾	A Max.	B* Min.	C	D* Min.	N Min.	W ₁	W ₂ Max.	W ₃
8mm	330 (12.992)	1.5 (0.059)	13.0 ^{+0.50} _{-0.20} (0.512 ^{+0.020} _{-0.008})	20.2 (0.795)	50.0 (1.969)	8.40 ^{+1.5} _{-0.6} (0.331 ^{+0.059} _{-0.0})	14.4 (0.567)	7.90 Min. (0.311) 10.9 Max. (0.429)
12mm						12.4 ^{+2.0} _{-0.6} (0.488 ^{+0.079} _{-0.0})	18.4 (0.724)	11.9 Min. (0.469) 15.4 Max. (0.607)

Metric dimensions will govern.

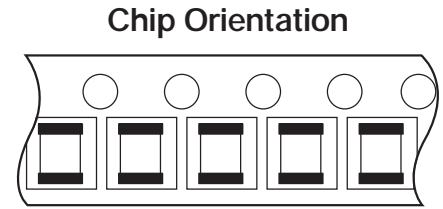
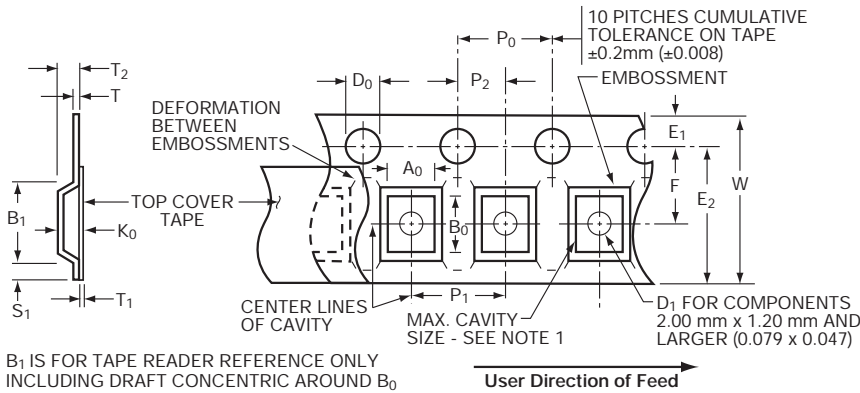
English measurements rounded and for reference only.

(1) For tape sizes 16mm and 24mm (used with chip size 3640) consult EIA RS-481 latest revision.

Embossed Carrier Configuration



8 & 12mm Tape Only



8 & 12mm Embossed Tape Metric Dimensions Will Govern

CONSTANT DIMENSIONS

Tape Size	D ₀	E	P ₀	P ₂	S ₁ Min.	T Max.	T ₁
8mm and 12mm	1.50 ^{+0.10} / _{0.0} (0.059 ^{+0.004} / _{0.0})	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	2.0 ± 0.05 (0.079 ± 0.002)	0.60 (0.024)	0.60 (0.024)	0.10 (0.004) Max.

VARIABLE DIMENSIONS

Tape Size	B ₁ Max.	D ₁ Min.	E ₂ Min.	F	P ₁ See Note 5	R Min. See Note 2	T ₂	W Max.	A ₀ B ₀ K ₀
8mm	4.35 (0.171)	1.00 (0.039)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	4.00 ± 0.10 (0.157 ± 0.004)	25.0 (0.984)	2.50 Max. (0.098)	8.30 (0.327)	See Note 1
12mm	8.20 (0.323)	1.50 (0.059)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	4.00 ± 0.10 (0.157 ± 0.004)	30.0 (1.181)	6.50 Max. (0.256)	12.3 (0.484)	See Note 1
8mm 1/2 Pitch	4.35 (0.171)	1.00 (0.039)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	2.00 ± 0.10 (0.079 ± 0.004)	25.0 (0.984)	2.50 Max. (0.098)	8.30 (0.327)	See Note 1
12mm Double Pitch	8.20 (0.323)	1.50 (0.059)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	8.00 ± 0.10 (0.315 ± 0.004)	30.0 (1.181)	6.50 Max. (0.256)	12.3 (0.484)	See Note 1

NOTES:

1. The cavity defined by A₀, B₀, and K₀ shall be configured to provide the following:

Surround the component with sufficient clearance such that:

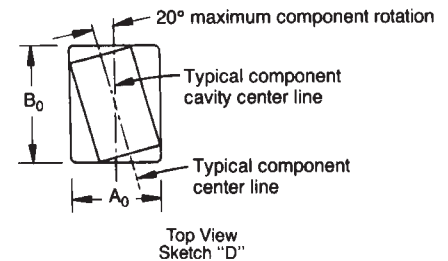
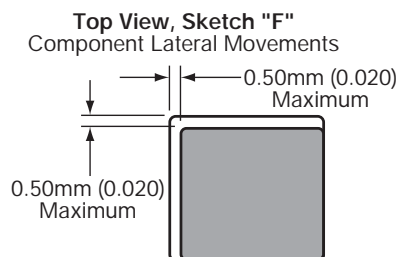
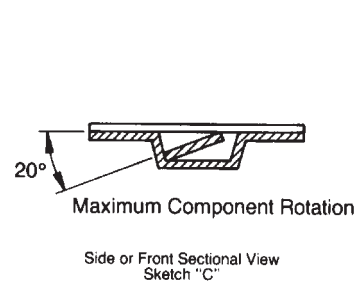
- the component does not protrude beyond the sealing plane of the cover tape.
- the component can be removed from the cavity in a vertical direction without mechanical restriction, after the cover tape has been removed.
- rotation of the component is limited to 20° maximum (see Sketches D & E).
- lateral movement of the component is restricted to 0.5mm maximum (see Sketch F).

2. Tape with or without components shall pass around radius "R" without damage.

3. Bar code labeling (if required) shall be on the side of the reel opposite the round sprocket holes. Refer to EIA-556.

4. B₁ dimension is a reference dimension for tape feeder clearance only.

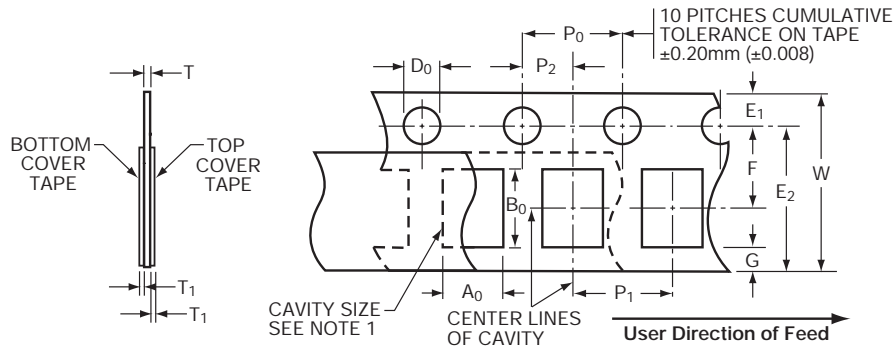
5. If P₁ = 2.0mm, the tape may not properly index in all tape feeders.



Paper Carrier Configuration



8 & 12mm Tape Only



8 & 12mm Paper Tape Metric Dimensions Will Govern

CONSTANT DIMENSIONS

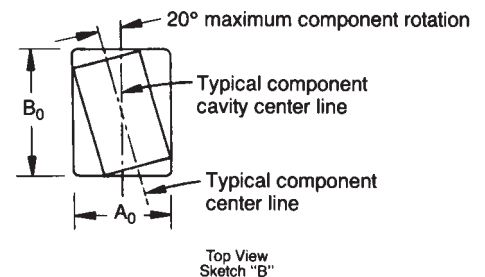
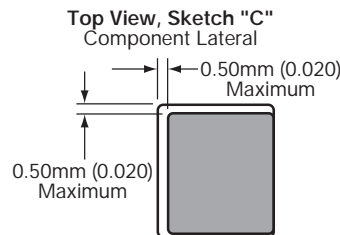
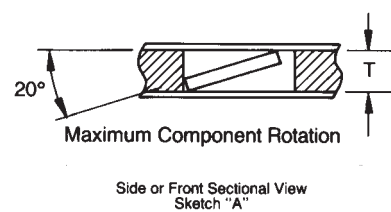
Tape Size	D ₀	E	P ₀	P ₂	T ₁	G. Min.	R Min.
8mm and 12mm	1.50 ^{+0.10} _{-0.004} (0.059 ^{+0.004} _{-0.004})	1.75 ± 0.10 (0.069 ± 0.004)	4.00 ± 0.10 (0.157 ± 0.004)	2.00 ± 0.05 (0.079 ± 0.002)	0.10 (0.004) Max.	0.75 (0.030) Min.	25.0 (0.984) See Note 2 Min.

VARIABLE DIMENSIONS

Tape Size	P ₁ See Note 4	E ₂ Min.	F	W	A ₀ B ₀	T
8mm	4.00 ± 0.10 (0.157 ± 0.004)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	8.00 ^{+0.30} _{-0.10} (0.315 ^{+0.012} _{-0.004})	See Note 1	1.10mm (0.043) Max. for Paper Base Tape and 1.60mm (0.063) Max. for Non-Paper Base Compositions
12mm	4.00 ± 0.010 (0.157 ± 0.004)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	12.0 ± 0.30 (0.472 ± 0.012)		
8mm 1/2 Pitch	2.00 ± 0.05 (0.079 ± 0.002)	6.25 (0.246)	3.50 ± 0.05 (0.138 ± 0.002)	8.00 ^{+0.30} _{-0.10} (0.315 ^{+0.012} _{-0.004})		
12mm Double Pitch	8.00 ± 0.10 (0.315 ± 0.004)	10.25 (0.404)	5.50 ± 0.05 (0.217 ± 0.002)	12.0 ± 0.30 (0.472 ± 0.012)		

NOTES:

- The cavity defined by A₀, B₀, and T shall be configured to provide sufficient clearance surrounding the component so that:
 - the component does not protrude beyond either surface of the carrier tape;
 - the component can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed;
 - rotation of the component is limited to 20° maximum (see Sketches A & B);
 - lateral movement of the component is restricted to 0.5mm maximum (see Sketch C).
- Tape with or without components shall pass around radius "R" without damage.
- Bar code labeling (if required) shall be on the side of the reel opposite the sprocket holes. Refer to EIA-556.
- If P₁ = 2.0mm, the tape may not properly index in all tape feeders.



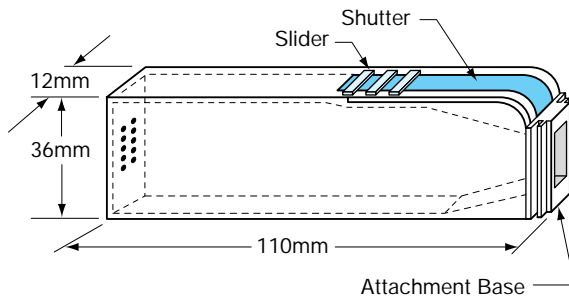
Bar Code Labeling Standard

AVX bar code labeling is available and follows latest version of EIA-556

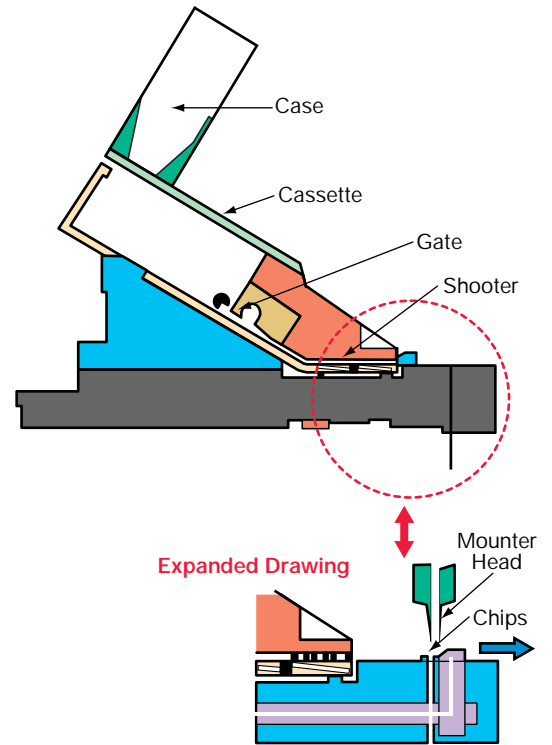
BENEFITS

- Easier handling
- Smaller packaging volume
(1/20 of T/R packaging)
- Easier inventory control
- Flexibility
- Recyclable

CASE DIMENSIONS



BULK FEEDER



CASE QUANTITIES

Part Size	0402	0603	0805	1206
Qty. (pcs / cassette)	80,000	15,000	10,000 (T=.023") 8,000 (T=.031") 6,000 (T=.043")	5,000 (T=.023") 4,000 (T=.032") 3,000 (T=.044")

I. Capacitance (farads)

English: $C = \frac{.224 \text{ K A}}{T_D}$

Metric: $C = \frac{.0884 \text{ K A}}{T_D}$

II. Energy stored in capacitors (Joules, watt - sec)

$$E = \frac{1}{2} CV^2$$

III. Linear charge of a capacitor (Amperes)

$$I = C \frac{dV}{dt}$$

IV. Total Impedance of a capacitor (ohms)

$$Z = \sqrt{R_s^2 + (X_C - X_L)^2}$$

V. Capacitive Reactance (ohms)

$$X_C = \frac{1}{2 \pi fC}$$

VI. Inductive Reactance (ohms)

$$X_L = 2 \pi fL$$

VII. Phase Angles:

Ideal Capacitors: Current leads voltage 90°

Ideal Inductors: Current lags voltage 90°

Ideal Resistors: Current in phase with voltage

VIII. Dissipation Factor (%)

$$\text{D.F.} = \tan \delta \text{ (loss angle)} = \frac{\text{E.S.R.}}{X_C} = (2 \pi fC) (\text{E.S.R.})$$

IX. Power Factor (%)

P.F. = Sine δ (loss angle) = Cos ϕ (phase angle)

P.F. = (when less than 10%) = DF

X. Quality Factor (dimensionless)

$$Q = \text{Cotan } \delta \text{ (loss angle)} = \frac{1}{\text{D.F.}}$$

XI. Equivalent Series Resistance (ohms)

$$\text{E.S.R.} = (\text{D.F.}) (X_C) = (\text{D.F.}) / (2 \pi fC)$$

XII. Power Loss (watts)

$$\text{Power Loss} = (2 \pi fCV^2) (\text{D.F.})$$

XIII. KVA (Kilowatts)

$$\text{KVA} = 2 \pi fCV^2 \times 10^{-3}$$

XIV. Temperature Characteristic (ppm/°C)

$$\text{T.C.} = \frac{C_t - C_{25}}{C_{25} (T_t - 25)} \times 10^6$$

XV. Cap Drift (%)

$$\text{C.D.} = \frac{C_1 - C_2}{C_1} \times 100$$

XVI. Reliability of Ceramic Capacitors

$$\frac{L_0}{L_t} = \left(\frac{V_t}{V_0} \right)^X \left(\frac{T_t}{T_0} \right)^Y$$

XVII. Capacitors in Series (current the same)

$$\text{Any Number: } \frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \dots \frac{1}{C_N}$$

$$\text{Two: } C_T = \frac{C_1 C_2}{C_1 + C_2}$$

XVIII. Capacitors in Parallel (voltage the same)

$$C_T = C_1 + C_2 \dots + C_N$$

XIX. Aging Rate

A.R. = % Δ C/decade of time

XX. Decibels

$$\text{db} = 20 \log \frac{V_1}{V_2}$$

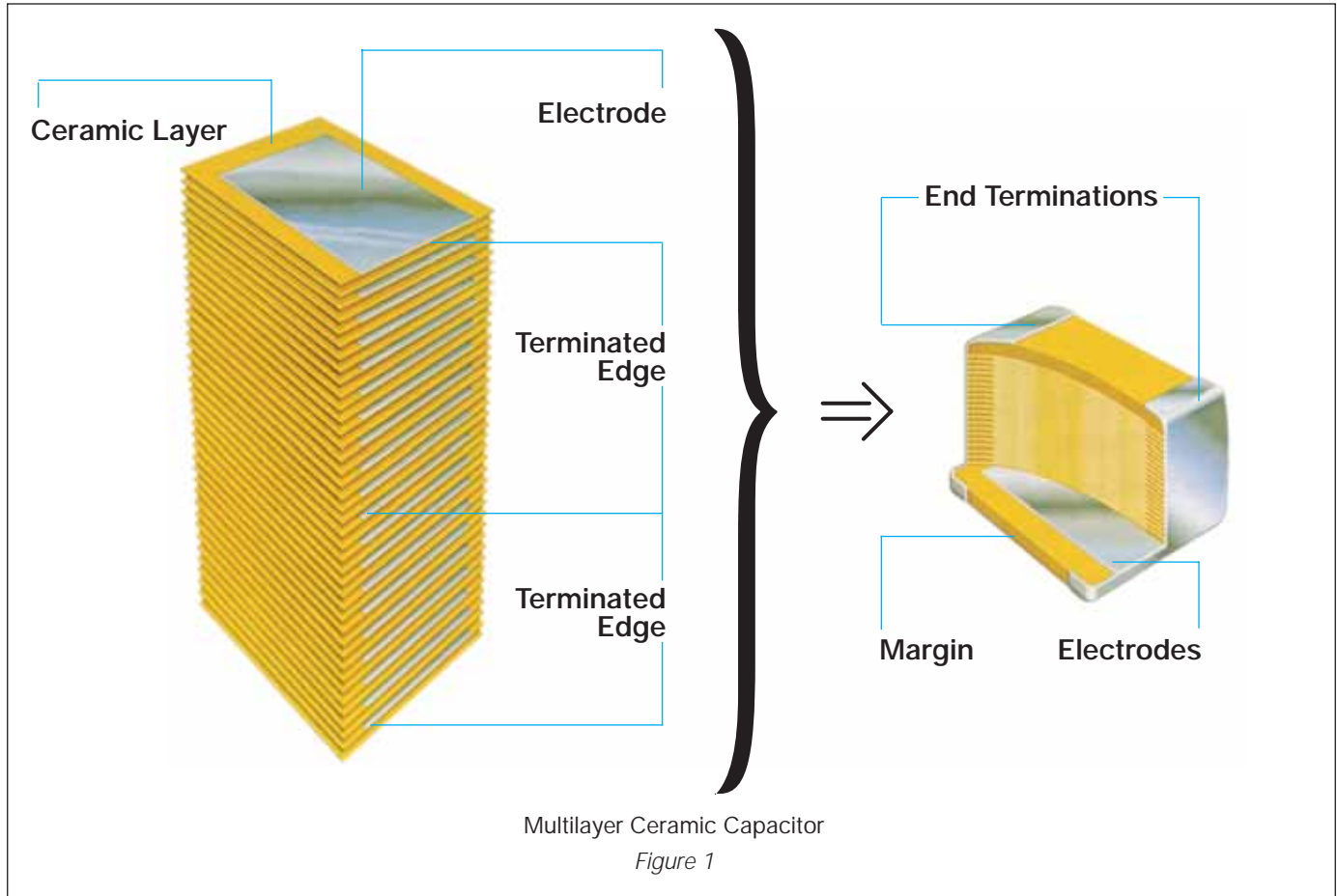
METRIC PREFIXES

SYMBOLS

Pico	X 10 ⁻¹²	K	= Dielectric Constant	f	= frequency	L _t	= Test life
Nano	X 10 ⁻⁹	A	= Area	L	= Inductance	V _t	= Test voltage
Micro	X 10 ⁻⁶	T _D	= Dielectric thickness	δ	= Loss angle	V ₀	= Operating voltage
Milli	X 10 ⁻³	V	= Voltage	ϕ	= Phase angle	T _t	= Test temperature
Deci	X 10 ⁻¹	t	= time	X & Y	= exponent effect of voltage and temp.	T ₀	= Operating temperature
Deca	X 10 ⁺¹	R _S	= Series Resistance	L ₀	= Operating life		
Deca	X 10 ⁺¹						
Kilo	X 10 ⁺³						
Mega	X 10 ⁺⁶						
Giga	X 10 ⁺⁹						
Tera	X 10 ⁺¹²						

Basic Construction – A multilayer ceramic (MLC) capacitor is a monolithic block of ceramic containing two sets of offset, interleaved planar electrodes that extend to two opposite surfaces of the ceramic dielectric. This simple

structure requires a considerable amount of sophistication, both in material and manufacture, to produce it in the quality and quantities needed in today's electronic equipment.



Formulations – Multilayer ceramic capacitors are available in both Class 1 and Class 2 formulations. Temperature compensating formulations are Class 1 and temperature stable and general application formulations are classified as Class 2.

Class 1 – Class 1 capacitors or temperature compensating capacitors are usually made from mixtures of titanates where barium titanate is normally not a major part of the mix. They have predictable temperature coefficients and in general, do not have an aging characteristic. Thus they are the most stable capacitor available. The most popular Class 1 multilayer ceramic capacitors are COG (NP0) temperature compensating capacitors (negative-positive 0 ppm/°C).

Class 2 – EIA Class 2 capacitors typically are based on the chemistry of barium titanate and provide a wide range of capacitance values and temperature stability. The most commonly used Class 2 dielectrics are X7R and Y5V. The X7R provides intermediate capacitance values which vary only $\pm 15\%$ over the temperature range of -55°C to 125°C . It finds applications where stability over a wide temperature range is required.

The Y5V provides the highest capacitance values and is used in applications where limited temperature changes are expected. The capacitance value for Y5V can vary from 22% to -82% over the -30°C to 85°C temperature range.

All Class 2 capacitors vary in capacitance value under the influence of temperature, operating voltage (both AC and DC), and frequency. For additional information on performance changes with operating conditions, consult AVX's software, SpiCap.

Table 1: EIA and MIL Temperature Stable and General Application Codes

<i>EIA CODE</i>	
<i>Percent Capacity Change Over Temperature Range</i>	
RS198	Temperature Range
X7	-55°C to +125°C
X6	-55°C to +105°C
X5	-55°C to +85°C
Y5	-30°C to +85°C
Z5	+10°C to +85°C
Code	Percent Capacity Change
D	±3.3%
E	±4.7%
F	±7.5%
P	±10%
R	±15%
S	±22%
T	+22%, -33%
U	+22%, -56%
V	+22%, -82%

EXAMPLE – A capacitor is desired with the capacitance value at 25°C to increase no more than 7.5% or decrease no more than 7.5% from -30°C to +85°C. EIA Code will be Y5F.

<i>MIL CODE</i>		
Symbol	Temperature Range	
A	-55°C to +85°C	
B	-55°C to +125°C	
C	-55°C to +150°C	
Symbol	Cap. Change Zero Volts	Cap. Change Rated Volts
R	+15%, -15%	+15%, -40%
S	+22%, -22%	+22%, -56%
W	+22%, -56%	+22%, -66%
X	+15%, -15%	+15%, -25%
Y	+30%, -70%	+30%, -80%
Z	+20%, -20%	+20%, -30%

Temperature characteristic is specified by combining range and change symbols, for example BR or AW. Specification slash sheets indicate the characteristic applicable to a given style of capacitor.

In specifying capacitance change with temperature for Class 2 materials, EIA expresses the capacitance change over an operating temperature range by a 3 symbol code. The first symbol represents the cold temperature end of the temperature range, the second represents the upper limit of the operating temperature range and the third symbol represents the capacitance change allowed over the operating temperature range. Table 1 provides a detailed explanation of the EIA system.

Effects of Voltage – Variations in voltage have little effect on Class 1 dielectric but does affect the capacitance and dissipation factor of Class 2 dielectrics. The application of DC voltage reduces both the capacitance and dissipation factor while the application of an AC voltage within a reasonable range tends to increase both capacitance and dissipation factor readings. If a high enough AC voltage is applied, eventually it will reduce capacitance just as a DC voltage will. Figure 2 shows the effects of AC voltage.

**Cap. Change vs. A.C. Volts
X7R**

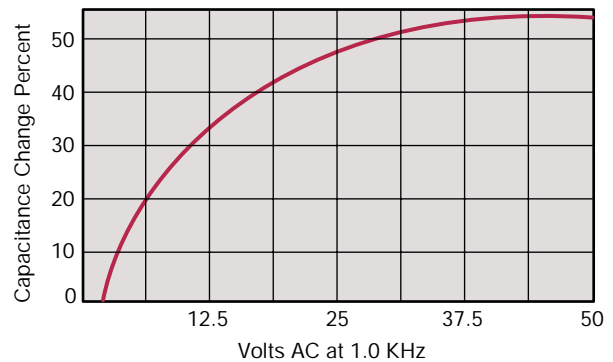


Figure 2

Capacitor specifications specify the AC voltage at which to measure (normally 0.5 or 1 VAC) and application of the wrong voltage can cause spurious readings. Figure 3 gives the voltage coefficient of dissipation factor for various AC voltages at 1 kilohertz. Applications of different frequencies will affect the percentage changes versus voltages.

**D.F. vs. A.C. Measurement Volts
X7R**

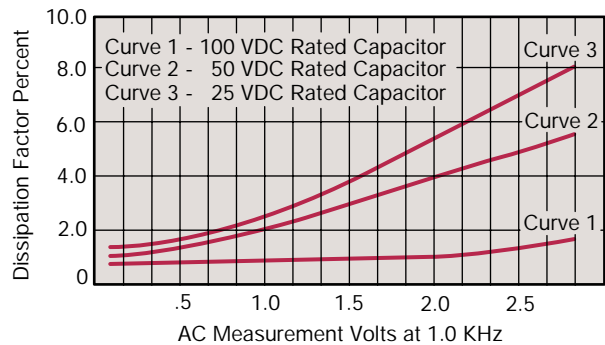


Figure 3

Typical effect of the application of DC voltage is shown in Figure 4. The voltage coefficient is more pronounced for higher K dielectrics. These figures are shown for room temperature conditions. The combination characteristic known as voltage temperature limits which shows the effects of rated voltage over the operating temperature range is shown in Figure 5 for the military BX characteristic.

**Typical Cap. Change vs. D.C. Volts
X7R**

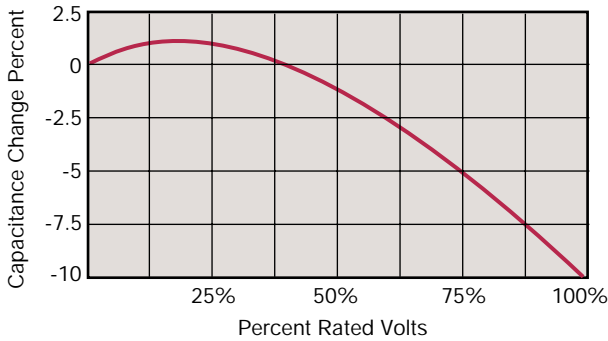


Figure 4

**Typical Cap. Change vs. Temperature
X7R**

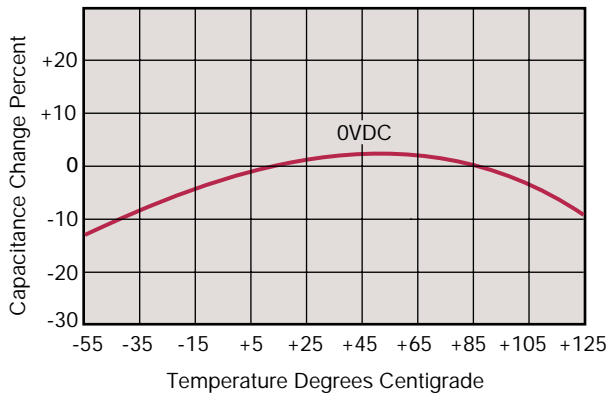


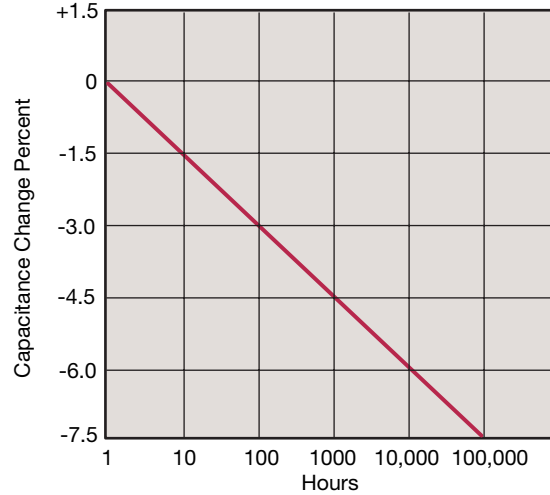
Figure 5

Effects of Time – Class 2 ceramic capacitors change capacitance and dissipation factor with time as well as temperature, voltage and frequency. This change with time is known as aging. Aging is caused by a gradual re-alignment of the crystalline structure of the ceramic and produces an exponential loss in capacitance and decrease in dissipation factor versus time. A typical curve of aging rate for semi-stable ceramics is shown in Figure 6.

If a Class 2 ceramic capacitor that has been sitting on the shelf for a period of time, is heated above its curie point, (125°C for 4 hours or 150°C for ½ hour will suffice) the part will de-age and return to its initial capacitance and dissipation factor readings. Because the capacitance changes rapidly, immediately after de-aging, the basic capacitance measurements are normally referred to a time period sometime after the de-aging process. Various manufacturers use different time bases but the most popular one is one day or twenty-four hours after “last heat.” Change in the aging curve can be caused by the application of voltage and other stresses. The possible changes in capacitance due to de-aging by heating the unit explain why capacitance changes are allowed after test, such as temperature cycling, moisture resistance, etc., in MIL specs. The application of high voltages such as dielectric withstanding voltages also

tends to de-age capacitors and is why re-reading of capacitance after 12 or 24 hours is allowed in military specifications after dielectric strength tests have been performed.

**Typical Curve of Aging Rate
X7R**



Characteristic	Max. Aging Rate %/Decade
C0G (NP0)	None
X7R, X5R	2
Y5V	7

Figure 6

Effects of Frequency – Frequency affects capacitance and impedance characteristics of capacitors. This effect is much more pronounced in high dielectric constant ceramic formulation than in low K formulations. AVX’s SpiCap software generates impedance, ESR, series inductance, series resonant frequency and capacitance all as functions of frequency, temperature and DC bias for standard chip sizes and styles. It is available free from AVX and can be downloaded for free from AVX website: www.avx.com.



Effects of Mechanical Stress – High “K” dielectric ceramic capacitors exhibit some low level piezoelectric reactions under mechanical stress. As a general statement, the piezoelectric output is higher, the higher the dielectric constant of the ceramic. It is desirable to investigate this effect before using high “K” dielectrics as coupling capacitors in extremely low level applications.

Reliability – Historically ceramic capacitors have been one of the most reliable types of capacitors in use today. The approximate formula for the reliability of a ceramic capacitor is:

$$\frac{L_o}{L_t} = \left(\frac{V_t}{V_o}\right)^X \left(\frac{T_t}{T_o}\right)^Y$$

where

L_o = operating life T_t = test temperature and
 L_t = test life T_o = operating temperature
 V_t = test voltage in °C
 V_o = operating voltage X, Y = see text

Historically for ceramic capacitors exponent X has been considered as 3. The exponent Y for temperature effects typically tends to run about 8.

A capacitor is a component which is capable of storing electrical energy. It consists of two conductive plates (electrodes) separated by insulating material which is called the dielectric. A typical formula for determining capacitance is:

$$C = \frac{.224 KA}{t}$$

C = capacitance (picofarads)
 K = dielectric constant (Vacuum = 1)
 A = area in square inches
 t = separation between the plates in inches
 (thickness of dielectric)
 .224 = conversion constant
 (.0884 for metric system in cm)

Capacitance – The standard unit of capacitance is the farad. A capacitor has a capacitance of 1 farad when 1 coulomb charges it to 1 volt. One farad is a very large unit and most capacitors have values in the micro (10^{-6}), nano (10^{-9}) or pico (10^{-12}) farad level.

Dielectric Constant – In the formula for capacitance given above the dielectric constant of a vacuum is arbitrarily chosen as the number 1. Dielectric constants of other materials are then compared to the dielectric constant of a vacuum.

Dielectric Thickness – Capacitance is indirectly proportional to the separation between electrodes. Lower voltage requirements mean thinner dielectrics and greater capacitance per volume.

Area – Capacitance is directly proportional to the area of the electrodes. Since the other variables in the equation are usually set by the performance desired, area is the easiest parameter to modify to obtain a specific capacitance within a material group.

Energy Stored – The energy which can be stored in a capacitor is given by the formula:

$$E = \frac{1}{2}CV^2$$

E = energy in joules (watts-sec)
 V = applied voltage
 C = capacitance in farads

Potential Change – A capacitor is a reactive component which reacts against a change in potential across it. This is shown by the equation for the linear charge of a capacitor:

$$I_{ideal} = C \frac{dV}{dt}$$

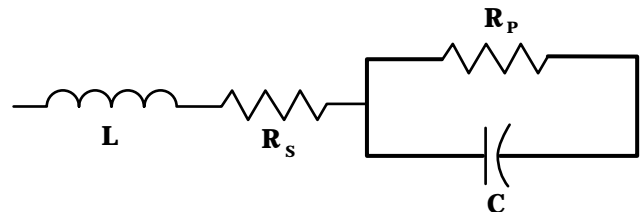
where

I = Current
 C = Capacitance
 dV/dt = Slope of voltage transition across capacitor

Thus an infinite current would be required to instantly change the potential across a capacitor. The amount of current a capacitor can “sink” is determined by the above equation.

Equivalent Circuit – A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is:

C = Capacitance L = Inductance
 R_s = Series Resistance R_p = Parallel Resistance



Reactance – Since the insulation resistance (R_p) is normally very high, the total impedance of a capacitor is:

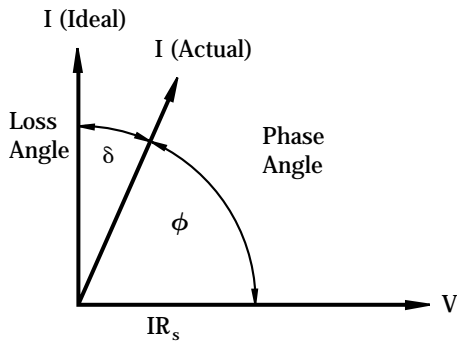
$$Z = \sqrt{R_s^2 + (X_c - X_L)^2}$$

where

Z = Total Impedance
 R_s = Series Resistance
 X_c = Capacitive Reactance = $\frac{1}{2\pi fC}$
 X_L = Inductive Reactance = $2\pi fL$

The variation of a capacitor’s impedance with frequency determines its effectiveness in many applications.

Phase Angle – Power Factor and Dissipation Factor are often confused since they are both measures of the loss in a capacitor under AC application and are often almost identical in value. In a “perfect” capacitor the current in the capacitor will lead the voltage by 90°.



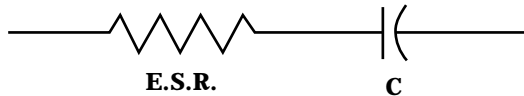
In practice the current leads the voltage by some other phase angle due to the series resistance R_s . The complement of this angle is called the loss angle and:

$$\text{Power Factor (P.F.)} = \cos \phi \text{ or } \sin \delta$$

$$\text{Dissipation Factor (D.F.)} = \tan \delta$$

for small values of δ the tan and sine are essentially equal which has led to the common interchangeability of the two terms in the industry.

Equivalent Series Resistance – The term E.S.R. or Equivalent Series Resistance combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection.



Dissipation Factor – The DF/PF of a capacitor tells what percent of the apparent power input will turn to heat in the capacitor.

$$\text{Dissipation Factor} = \frac{\text{E.S.R.}}{X_c} = (2 \pi fC) (\text{E.S.R.})$$

The watts loss are:

$$\text{Watts loss} = (2 \pi fCV^2) (\text{D.F.})$$

Very low values of dissipation factor are expressed as their reciprocal for convenience. These are called the “Q” or Quality factor of capacitors.

Parasitic Inductance – The parasitic inductance of capacitors is becoming more and more important in the decoupling of today’s high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$V = L \frac{di}{dt}$$

The $\frac{di}{dt}$ seen in current microprocessors can be as high as 0.3 A/ns, and up to 10A/ns. At 0.3 A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the V_{cc} for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, bypass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

Insulation Resistance – Insulation Resistance is the resistance measured across the terminals of a capacitor and consists principally of the parallel resistance R_P shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the I.R. decreases and hence the product ($C \times IR$ or RC) is often specified in ohm farads or more commonly megohm-microfarads. Leakage current is determined by dividing the rated voltage by IR (Ohm’s Law).

Dielectric Strength – Dielectric Strength is an expression of the ability of a material to withstand an electrical stress. Although dielectric strength is ordinarily expressed in volts, it is actually dependent on the thickness of the dielectric and thus is also more generically a function of volts/mil.

Dielectric Absorption – A capacitor does not discharge instantaneously upon application of a short circuit, but drains gradually after the capacitance proper has been discharged. It is common practice to measure the dielectric absorption by determining the “reappearing voltage” which appears across a capacitor at some point in time after it has been fully discharged under short circuit conditions.

Corona – Corona is the ionization of air or other vapors which causes them to conduct current. It is especially prevalent in high voltage units but can occur with low voltages as well where high voltage gradients occur. The energy discharged degrades the performance of the capacitor and can in time cause catastrophic failures.

REFLOW SOLDERING

Case Size	D1	D2	D3	D4	D5
0402	1.70 (0.07)	0.60 (0.02)	0.50 (0.02)	0.60 (0.02)	0.50 (0.02)
0603	2.30 (0.09)	0.80 (0.03)	0.70 (0.03)	0.80 (0.03)	0.75 (0.03)
0805	3.00 (0.12)	1.00 (0.04)	1.00 (0.04)	1.00 (0.04)	1.25 (0.05)
1206	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	1.60 (0.06)
1210	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	2.50 (0.10)
1808	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	2.00 (0.08)
1812	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	3.00 (0.12)
1825	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	6.35 (0.25)
2220	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	5.00 (0.20)
2225	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	6.35 (0.25)

Dimensions in millimeters (inches)

Component Pad Design

Component pads should be designed to achieve good solder fillets and minimize component movement during reflow soldering. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

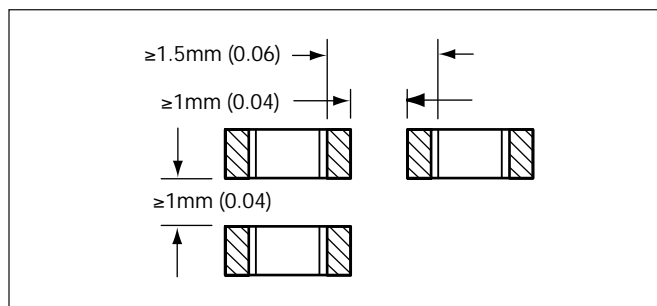
WAVE SOLDERING

Case Size	D1	D2	D3	D4	D5
0603	3.10 (0.12)	1.20 (0.05)	0.70 (0.03)	1.20 (0.05)	0.75 (0.03)
0805	4.00 (0.15)	1.50 (0.06)	1.00 (0.04)	1.50 (0.06)	1.25 (0.05)
1206	5.00 (0.19)	1.50 (0.06)	2.00 (0.09)	1.50 (0.06)	1.60 (0.06)

Dimensions in millimeters (inches)

Component Spacing

For wave soldering components, must be spaced sufficiently far apart to avoid bridging or shadowing (inability of solder to penetrate properly into small spaces). This is less important for reflow soldering but sufficient space must be allowed to enable rework should it be required.



Preheat & Soldering

The rate of preheat should not exceed 4°C/second to prevent thermal shock. A better maximum figure is about 2°C/second.

For capacitors size 1206 and below, with a maximum thickness of 1.25mm, it is generally permissible to allow a temperature differential from preheat to soldering of 150°C. In all other cases this differential should not exceed 100°C.

For further specific application or process advice, please consult AVX.

Cleaning

Care should be taken to ensure that the capacitors are thoroughly cleaned of flux residues especially the space beneath the capacitor. Such residues may otherwise become conductive and effectively offer a low resistance bypass to the capacitor.

Ultrasonic cleaning is permissible, the recommended conditions being 8 Watts/litre at 20-45 kHz, with a process cycle of 2 minutes vapor rinse, 2 minutes immersion in the ultrasonic solvent bath and finally 2 minutes vapor rinse.

Surface Mounting Guide



MLC Chip Capacitors

APPLICATION NOTES

Storage

Good solderability is maintained for at least twelve months, provided the components are stored in their "as received" packaging at less than 40°C and 70% RH.

Solderability

Terminations to be well soldered after immersion in a 60/40 tin/lead solder bath at $235 \pm 5^\circ\text{C}$ for 2 ± 1 seconds.

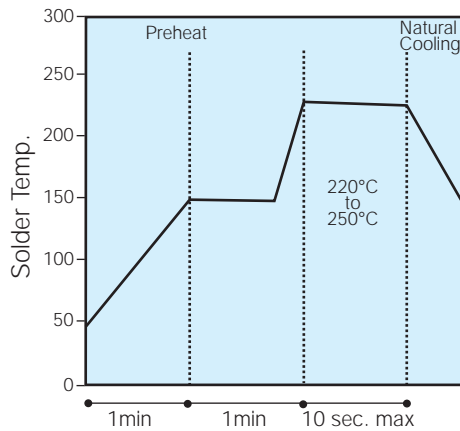
Leaching

Terminations will resist leaching for at least the immersion times and conditions shown below.

Termination Type	Solder Tin/Lead/Silver	Solder Temp. °C	Immersion Time Seconds
Nickel Barrier	60/40/0	260 ± 5	30 ± 1

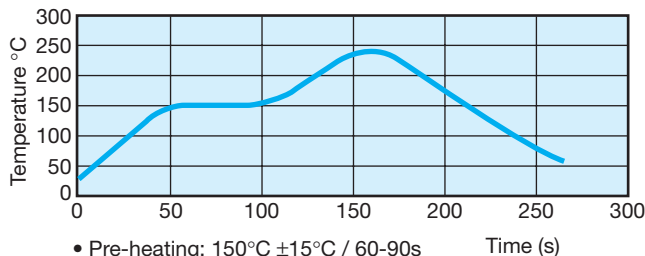
Recommended Soldering Profiles

Reflow



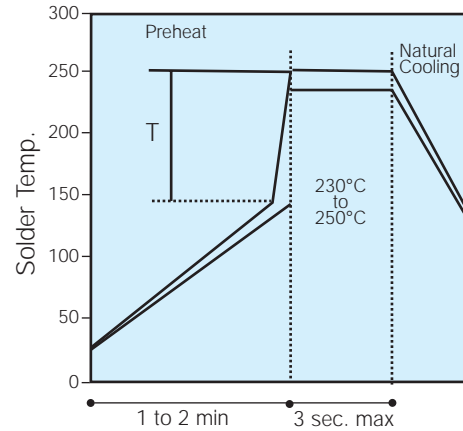
(Minimize soldering time)

Lead-Free Reflow Profile



- Pre-heating: $150^\circ\text{C} \pm 15^\circ\text{C}$ / 60-90s
- Max. Peak Gradient 2.5°C/s
- Peak Temperature: $245^\circ\text{C} \pm 5^\circ\text{C}$
- Time at $>230^\circ\text{C}$: 40s Max.

Wave



(Preheat chips before soldering)
T/maximum 150°C

Lead-Free Wave Soldering

The recommended peak temperature for lead-free wave soldering is 250°C - 260°C for 3-5 seconds. The other parameters of the profile remains the same as above.

The following should be noted by customers changing from lead based systems to the new lead free pastes.

- The visual standards used for evaluation of solder joints will need to be modified as lead free joints are not as bright as with tin-lead pastes and the fillet may not be as large.
- Resin color may darken slightly due to the increase in temperature required for the new pastes.
- Lead-free solder pastes do not allow the same self alignment as lead containing systems. Standard mounting pads are acceptable, but machine set up may need to be modified.

General

Surface mounting chip multilayer ceramic capacitors are designed for soldering to printed circuit boards or other substrates. The construction of the components is such that they will withstand the time/temperature profiles used in both wave and reflow soldering methods.

Handling

Chip multilayer ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers or vacuum pick ups is strongly recommended for individual components. Bulk handling should ensure that abrasion and mechanical shock are minimized. Taped and reeled components provides the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling chip multilayer ceramic capacitors.

Preheat

It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4°C/second

MLC Chip Capacitors

and a target figure 2°C/second is recommended. Although an 80°C to 120°C temperature differential is preferred, recent developments allow a temperature differential between the component surface and the soldering temperature of 150°C (Maximum) for capacitors of 1210 size and below with a maximum thickness of 1.25mm. The user is cautioned that the risk of thermal shock increases as chip size or temperature differential increases.

Soldering

Mildly activated rosin fluxes are preferred. The minimum amount of solder to give a good joint should be used. Excessive solder can lead to damage from the stresses caused by the difference in coefficients of expansion between solder, chip and substrate. AVX terminations are suitable for all wave and reflow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

Cooling

Natural cooling in air is preferred, as this minimizes stresses within the soldered joint. When forced air cooling is used, cooling rate should not exceed 4°C/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

Cleaning

Flux residues may be hygroscopic or acidic and must be removed. AVX MLC capacitors are acceptable for use with all of the solvents described in the specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.

POST SOLDER HANDLING

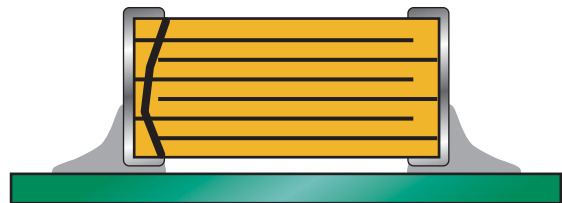
Once SMP components are soldered to the board, any bending or flexure of the PCB applies stresses to the soldered joints of the components. For leaded devices, the stresses are absorbed by the compliancy of the metal leads and generally don't result in problems unless the stress is large enough to fracture the soldered connection.

Ceramic capacitors are more susceptible to such stress because they don't have compliant leads and are brittle in nature. The most frequent failure mode is low DC resistance or short circuit. The second failure mode is significant loss of capacitance due to severing of contact between sets of the internal electrodes.

Cracks caused by mechanical flexure are very easily identified and generally take one of the following two general forms:



Type A:
Angled crack between bottom of device to top of solder joint.



Type B:
Fracture from top of device to bottom of device.

Mechanical cracks are often hidden underneath the termination and are difficult to see externally. However, if one end termination falls off during the removal process from PCB, this is one indication that the cause of failure was excessive mechanical stress due to board warping.

COMMON CAUSES OF MECHANICAL CRACKING

The most common source for mechanical stress is board depanelization equipment, such as manual breakapart, v-cutters and shear presses. Improperly aligned or dull cutters may cause torqueing of the PCB resulting in flex stresses being transmitted to components near the board edge. Another common source of flexural stress is contact during parametric testing when test points are probed. If the PCB is allowed to flex during the test cycle, nearby ceramic capacitors may be broken.

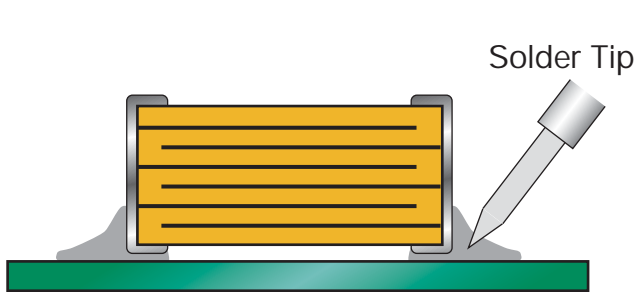
A third common source is board to board connections at vertical connectors where cables or other PCBs are connected to the PCB. If the board is not supported during the plug/unplug cycle, it may flex and cause damage to nearby components.

Special care should also be taken when handling large (>6" on a side) PCBs since they more easily flex or warp than smaller boards.

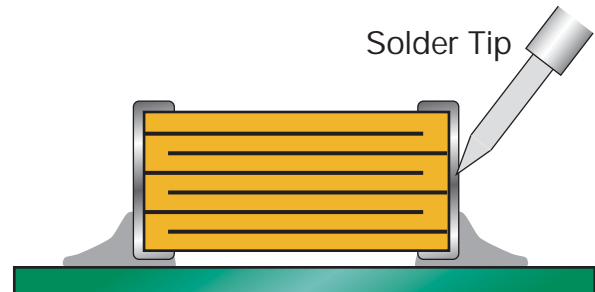
REWORKING OF MLCs

Thermal shock is common in MLCs that are manually attached or reworked with a soldering iron. *AVX strongly recommends that any reworking of MLCs be done with hot air reflow rather than soldering irons.* It is practically impossible to cause any thermal shock in ceramic capacitors when using hot air reflow.

However direct contact by the soldering iron tip often causes thermal cracks that may fail at a later date. If rework by soldering iron is absolutely necessary, it is recommended that the wattage of the iron be less than 30 watts and the tip temperature be <math><300^{\circ}\text{C}</math>. *Rework should be performed by applying the solder iron tip to the pad and not directly contacting any part of the ceramic capacitor.*



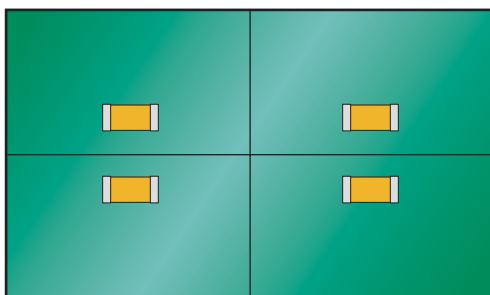
Preferred Method - No Direct Part Contact



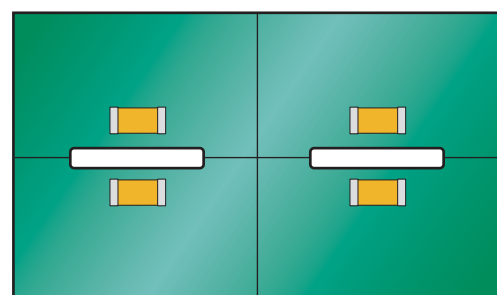
Poor Method - Direct Contact with Part

PCB BOARD DESIGN

To avoid many of the handling problems, AVX recommends that MLCs be located at least .2" away from nearest edge of board. However when this is not possible, AVX recommends that the panel be routed along the cut line, adjacent to where the MLC is located.



No Stress Relief for MLCs



Routed Cut Line Relieves Stress on MLC